8XC51RX
SPECIFICATION UPDATE

Release Date: July, 1996

Order Number: 272885-001

The 8XC51RX may contain design defects or errors known as errata. Characterized errata that may cause the 8XC51RX's behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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or call in North America 1-800-879-4683, Europe 44-0-1793-431-155, France 44-0-1793-421-777,

Germany 44-0-1793-421-333 other Countries 708-296-9333

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REVISION HISTORY

Date of Revision	Version	Description
07/01/96	001	This is the new Specification Update document. It contains all errata published prior to this date.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the first release of the 8XC51RX Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published.

Affected Documents/Related Documents

Title	Order
Embedded Microcontrollers	270646-007
MCS® 51 Microcontroller Family User's Manual	272383-001

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 8XC51RX product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	A#	#	#			
	--					None for this revision of this specification update.

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
	#	#	#			
						None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	A#	#	#			
001	X			8		Program Memory
002	X			8		Data Memory
003	X			8		Upgrading Considerations
004	X			10		Hardware Watchdog (One-time Enabled with Reset-Out)
005	X			10		Using the WDT
006	X			10		WDT During Power Down and Idle
007	X			11		Interrupts

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
				None for this revision of this specification update.

IDENTIFICATION INFORMATION

Markings

No special identifier but standard C51RX product marking.

ERRATA

None for this revision of this specification update.

SPECIFICATION CHANGES

None for this revision of this specification update.

SPECIFICATION CLARIFICATIONS

001. Program Memory

PROBLEM: If the EA# pin is connected to V_{CC}, all program fetches are directed to external memory. On the 83C51RA (or 87C51RA), if the EA# pin is connected to V_{CC}, then program fetches to address 0000H through 1FFFH are directed to internal ROM and fetches to address 2000H through FFFFH are to external memory.

On the 83C51RB (or 87C51RB) if EA# is connected to V_{CC}, program fetches to address 0000H through 3FFFH are directed to internal ROM, and fetches to addresses 4000H through FFFFH are to external memory.

On the 83C51RC (or 87C51RC) if EA# is connected to V_{CC}, program fetches to address 8000H through FFFFH are to external memory.

002. Data Memory

PROBLEM: The 8XC51RX has internal data memory that is mapped into four separate segments:

1. The lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
2. The upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
3. The Special Function Registers (SFRs, 80H to FFH) are directly addressable only.
4. The 256 bytes of expanded RAM (ERAM, 00H-FFH) are indirectly accessed by move external instruction, MOVX, and with the EXTRAM bit cleared.

003. Upgrading Considerations

PROBLEM: The default value of EXTRAM bit is 0. To use external memory, customers will need to set the EXTRAM bit to 1.

Table 1 shows the Auxiliary (AUXR) register. This register contains the control bits for external or EXTRAM access.

AUXR			Address = 8EH				Reset Value = xxxx xx00B
Not Bit Addressable							
---	---	---	---	---	---	EXTRAM	DISALE
Bit 7	6	5	4	3	2	1	0

DISALE	Disable/Enable ALE	
	DISALE Operating Mode	
	0	ALE is emitted at a constant rate of 1/6 the oscillator frequency
	1	ALE is active only during a MOVX or MOVC instruction
EXTRAM	Internal/External RAM (00H-FFH) access using MOVX @Ri/@DPTR	
	Reserved for future expansion	
	EXTRAM Operating Mode	
	0	Internal ERAM (00H-FFH) access using MOVX @Ri/@DPTR
	1	External data memory access
---	Reserved, do not write 1s into it	

Table 1. AUXR: Auxiliary Register

Figure 1 contains the internal and external memory address space with EXTRAM = 0. This condition accesses the 256 bytes of extended RAM and disables external memory access.

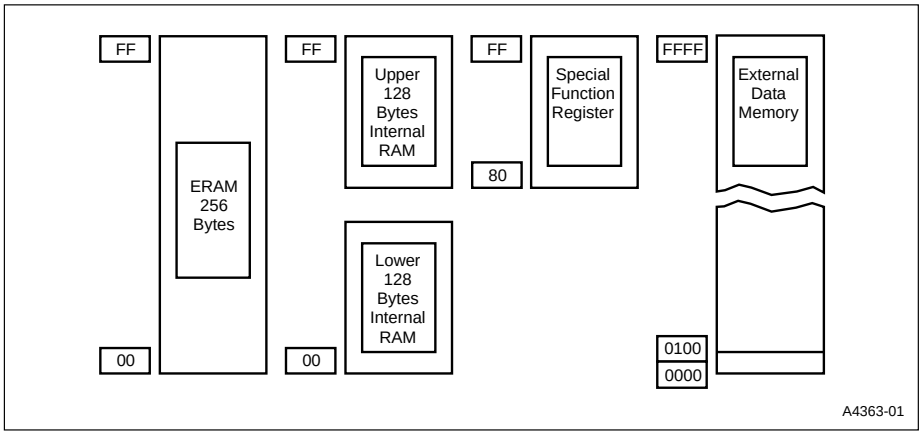

Figure 1. Internal and External Data Memory Address Space with EXTRAM = 0

004. Hardware Watchdog Timer (One-time Enabled with Reset-Out)

PROBLEM: The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the watchdog timer reset (WDTRST) SFR. The WDT defaults to disabled when exiting reset. To enable the WDT, customers must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

005. Using the WDT

PROBLEM: To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET x T_{OSC}, where $T_{OSC} = 1/F_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will be periodically be executed within the time required to prevent a WDT reset.

006. WDT During Power Down and Idle

PROBLEM: In Power Down mode the oscillator stops, which means the WDT also stops. While in Power Down mode the user does not need to service the WDT. There are 2 methods of exiting Power Down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power Down mode. When Power Down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the C51RX is reset. Exiting Power Down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power Down.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is best to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the C51RX while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and reenter Idle mode.

007. Interrupts

PROBLEM: In the 8XC51RA/RB/RC, a second Interrupt Priority register (IPH) has been added, increasing the number of priority levels to four. Table 2 shows this second register. The added register becomes the MSB of the priority select bits and the existing IP register acts as the LSB. This scheme maintains compatibility with the rest of the MCS® 51 family (8XC51FX, 8XC52/8XC54/8XC58, 8XC51GB).

IPH Address = 0B7H Reset Value = XX00 0000B

Not Bit Addressable

---	---	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
Bit 7	6	5	4	3	2	1	0

Symbol	Function
---	Not implemented, reserved for future use.
PT2H	Timer 2 interrupt priority high bit.
PSH	Serial Port interrupt priority high bit.
PT1H	Timer 1 interrupt priority high bit.
PX1H	External interrupt 1 priority high bit.
PT0H	Timer 0 interrupt priority high bit.
PX0H	External interrupt priority high bit.

Table 2. IPH: Interrupt Priority Register

DOCUMENTATION CHANGES

None for this revision of this specification update.