8XC51SL
SPECIFICATION UPDATE

Release Date: July 1996

Order Number: 272877-001

The 8XC51SL may contain design defects or errors known as errata. Characterized errata that may cause the 8XC51SL's behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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Mt. Prospect, IL 60056-7641

or call in North America 1-800-879-4683, Europe 44-0-1793-431-155, France 44-0-1793-421-777,

Germany 44-0-1793-421-333 other Countries 708-296-9333

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REVISION HISTORY

Date of Revision	Version	Description
07/01/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the first release of the 8XC51SL Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published.

Affected Documents/Related Documents

Title	Order
Embedded Microcontrollers	270646-007
MCS® 51 Microcontroller Family User's Manual	272383-001

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 8XC51SL product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	8XC51SL -BG All #s	8XC51SL -AH/AL CA#	8XC51SL -AH/AL DA#			
9600001	X			7	Fixed	Gate A20, RCL Hardware Speed-up Processing
9600002	X			7	Fixed	MEMCSL, P27/LED4 Sink Current
9600003	X			8	Fixed	Port 3 Power Down Wakeup
9600004	X			9	Fixed	8XC51SL-BG Power Down Current Stabilization
9600005	X			10	Fixed	Port 2 Address Mux
9600006	X			10	Fixed	KSI Power Down Wakeup Interrupt
9600007	X			11	Fixed	8XC51SL-BG Reset Errata
9600008		X		13	Fixed	8XC51SL-AH/AL Power Down Current Stabilization Errata
9600009		X		14	Fix	Power Management Date and Status Registers
96000010		X	X	15	Fix	8XC51SL-AH/AL Interrupt Priority Erratum

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
	#	#	#			
						None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
				None for this revision of this specification update.

IDENTIFICATION INFORMATION

Markings

8XC51SL-BG products are identified as follows. The change indicator is located in the ninth character position of the FPO number. The FPO number is the second line on the top side mark of the device.

Top Side Marking	Stepping	Change Indicator
KU80C51SLBG, SV984	B0	A
KU80C51SLBG, SV985	B1	B
KU80C51SLBG, SV994	B2	C
KU80C51SLBG, SW008	B2	C
KU80C51SLBG, SW011	B3	D

ERRATA

9600001. Gate A20, RCL Hardware Speed-up Processing

PROBLEM: The hardware speed-up option on pin 57 gate A20, and pin 64 RCL causes spurious false interrupts on the PCIBF interrupt. This is caused by a timing marginality in the silicon.

IMPLICATION : It is unlikely to cause serious problems.

WORKAROUND: Before processing a PCIBF interrupt first check the status of the PCIBF register (address 7FF2H, bit 1). If the PCIBF register is consecutively read active twice, continue to process the interrupt subroutine, otherwise do not service the subroutine.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: All BG steppings.

9600002. MEMCSL, P27/LED4 Sink Current

PROBLEM: Pin 28 (MEMCSL) and pin 55 (P27/LED4) do not sink any current (Iol = 0mA) while specified at 8mA and 12mA respectively.

IMPLICATION : It is unlikely to cause serious problems.

WORKAROUND: B-0 samples (ceramic pkgs on QDF# 0185, and plastic pkgs on QDF# 0187) can be used with the following external workarounds:

a. Include external 40k ohm (or less) pull down resistor on MEMCSL.
b. Only use P27/LED4 as input port pin (since it is already defined as open-drain output, i.e., no source current capability).

This problem is fixed in the B-1 stepping of the 80C51SL-BG and any future steppings.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: All BG steppings.

9600003. Port 3 Power Down Wakeup

PROBLEM: The 80C51SL-BG may not exit from power down mode using a port 3 external interrupt. Active external interrupts on either P30/SIF00, P32/INT0, P33/SIF10, or P37/RDL are specified to terminate power down mode (used during suspend/off modes). Power down mode is actually exited when a high to low transition occurs on either P30, P32, P33, or P37 with EXTINTEN bit enabled (configuration register 0, bit 4) and the three remaining pins high.

IMPLICATION: If P30, P32, P33, and P37 are not all high prior to entering power down mode, a low transition on any of the four pins will NOT wake up the 80C51SL-BG from power down mode. Enabling or disabling the interrupts corresponding to these four pins (registers IE at address A8H, and IE1 at address E8H) has no effect on exiting power down mode.

WORKAROUND: Three possible workarounds exist dependent upon how the 80C51SL-BG is configured in the system:

a. Ensure that P30, P32, P33, and P37 are all high prior to entering power down mode. With EXTINTEN set, the first low edge on P30, P32, P33, or P37 will wake up the 80C51SL-BG from power down mode. Note: If these pins cannot be set high prior to entering power down mode, the port 3 wakeup sources must be disabled by clearing the EXTINTEN bit and an alternate wakeup source used.

b. Alternatively, instead of using port 3 pins for wakeup, the P10-16 wakeup feature can be used. However, it can only be enabled/disabled as a group via configuration register 0, bit 2. P10-16 pins must all be high when entering power down mode in order for one or more of the P10-16 inputs to detect a wakeup (low edge).

c. If neither of the above methods are possible, then one of the possible wakeup sources, the suspend/resume or off button (typically connected to P32 or P37) can be connected to an unused key matrix position with software definition as a suspend/resume or off button.

The problem is addressed in the B-3 80C51SL-BG stepping and any future steppings.

NOTE: This fix will reduce the number of specified port 3 wakeup sources from four to one (only P32 is supported). EXTINTEN enables/disables this feature, while the INT0 interrupt enable/disable has no affect.

Typically, P30 and P33 are used for keyboard clock and mouse clock respectively. Since the external keyboard and mouse are generally power off during suspend or off modes to conserve battery life, resume would not be allowed from an external keyboard or mouse. Thus P30 and P33 are not used for power down wakeup.

Actual battery life impact will vary dependent upon how often/long power down mode is used (during system suspend/off modes) along with storage temperature of the notebook.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

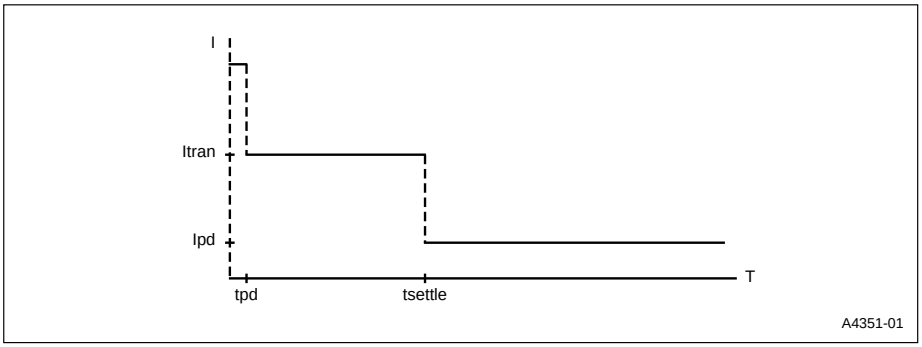
AFFECTED PRODUCTS: All BG steppings.

9600004. 8XC51SL-BG Power Down Current Stabilization

PROBLEM: Power down current (Ipd) transitions from Icc typical to the low mA range before settling into the low µA range. Ipd is also higher than estimated in the product preview data sheet. The 80C51SL-BG must also have power applied at least one minute prior to entering power down mode.

IMPLICATION : This problem will only slightly affect battery life.

WORKAROUND: No work around currently available. Limited characterization data was taken (three different lots, three units per lot) to estimate Ipd. The following data is not guaranteed, but should be characteristic of Ipd.



Symbol	Parameter	Typical (25°C)	Typical (0°C)
Itran	Transition current between Icc typical and Ipd	2 mA	3 mA
Ipd	Power down current	50 μA	800 μA
tsettle - tpd	Time for current to transition from Icc to Ipd	80 seconds	18 minutes

Actual battery life impact will vary dependent upon how often/long power down mode is used (during system suspend/off modes) along with storage temperature of the notebook.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: All BG steppings.

9600005. Port 2 Address Mux

PROBLEM: MOVX @Ri instructions will not output port 2 SFR contents when EAL is low.

IMPLICATION: It is unlikely to cause serious problems.

WORKAROUND: When accessing external data RAM, always use the MOVX @DPTR instructions. Do not use MOVX @Ri.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600006. KSI Power Down Wakeup Interrupt

PROBLEM: When using the KSI to bring the device out of power down mode, a KDINTL interrupt is generated and left pending on wakeup. The reset generated by the KSI interrupt should clear the interrupt latch, but does not.

IMPLICATION: Varies.

WORKAROUND: Before going into power down mode the software can set the PDFLAG bit in configuration register 0. This bit will be cleared on an external or software generated reset, but not on the reset generated when using Port 1, Port 3, or KSI to wakeup from power down mode. When the KDINTL is detected the interrupt routine can check the PDFLAG status and use this to determine whether to process the keyboard interrupt or to ignore it.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: All BG steppings.

9600007. 8XC51SL-BG Reset Errata

PROBLEM: Intel has confirmed that there is an intermittent reset problem with the 8XC51SL-BG. Abnormal ALE, PSENL, and Address have been observed after reset, and in some systems several of the Port 3 pins have toggled during reset.

The 8XC51SL-BG can be reset in the following ways:

1. RST, pin 68, pulled high for greater than 2 8XC51SL-BG machine cycles.

2. Software initiated reset (write to location 7FF0H).

3. Exiting powerdown mode via:

  a. A host data/command Write sequence to the Host interface.

  b. An input key depression sensed via KSI0-7 or P10-6.

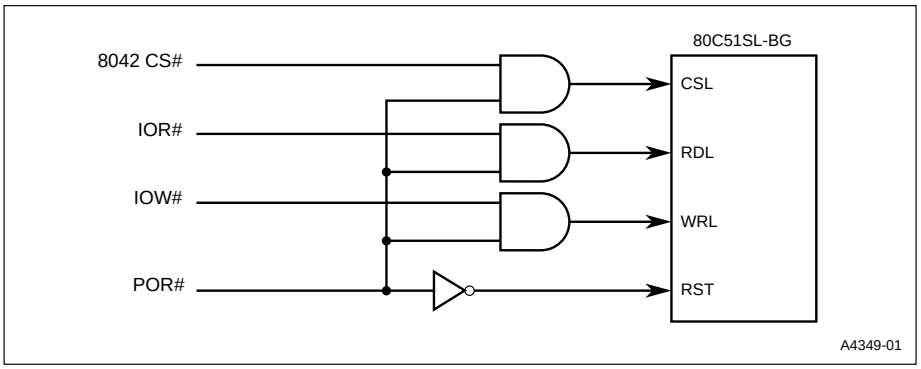
  c. A high to low transition on P32 while EXTINTEN (config. reg. 0, bit 4) is set, with P32 high before entering powerdown mode.

IMPLICATION : During any of the 8XC51SL-BG resets listed, a floating node within the 8XC51SL-BG may cause internal clock signals to be killed thus not allowing a valid reset.

WORKAROUND: Workaround #1 (external logic: 3 gates). This is Intel's recommended workaround.

Drive the 8XC51SL-BG CSL, RDL, and WRL pins low during RST to guarantee a valid RST reset (typically used for power-on reset [POR]). Driving these 8XC51SL-BG pins low during reset drives the floating node to a proper state which allows reset to occur. During the time CSL, RDL, and WRL are driven low, LED0, LED2, and PCOB0-7 will be driven low from the 8XC51SL-BG.

Driving CSL, RDL, and WRL low during RST ensures that a valid RST reset (POR) occurs. It is possible for the problem node to float during non-RST resets after it has been initially set during a RST reset with the workaround in place. It this occurs the system user will have to issue one or more additional resets if the first non-RST reset fails. However, bench test experimentation has shown no reset failures after a valid PD. was applied to RST with the workaround in place. The tests were conducted at room, hot, and cold temperatures for over 8 hours with several million software resets issued. Your system should be verified to confirm that no quality issue exists on the non-RST resets after implementing this workaround. The following figure shows a typical implementation of this work around.

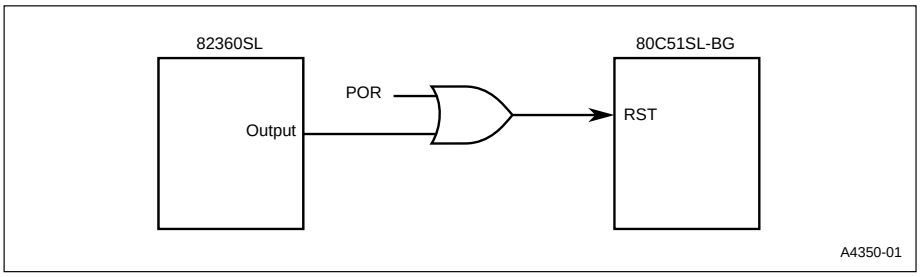


Workaround #2 (System BIOS modification, blue-wire, plus potential OR-gate). This is an alternative workaround.

Drive the 8XC51SL-BG RST input with a presently unused 82360SL output (blue-wire). If a valid 8XC51SL-BG reset is not detected (POST code error), the 82360SL will issue another reset to RST. Each system should be tested to ensure that having the 8XC51SL-BG powered before properly being reset does not cause any system problems. It may be beneficial to OR the present POR reset (if applicable) with the 82360SL system BIOS controlled reset signal to minimize this occurrence.

As with workaround #1, this workaround only directly addresses the RST reset and Intel recommends that each system model be tested to ensure that no quality issue exists with the additional reset sources.

The following figure shows a typical implementation of this workaround.



STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

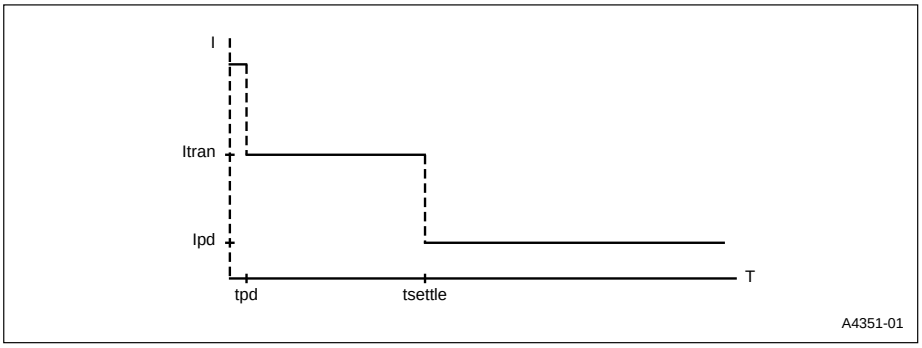
AFFECTED PRODUCTS: All BG steppings.

9600008. 8XC51SL-AH/AL Power Down Current Stabilization Errata

PROBLEM: Power down current (Ipd) transitions from Icc typical to the low mA range before settling into the low micro-amp range. Ipd is also higher than estimated in the product preview data sheet. The 80C51SL-AH/AL must have power applied at least 1 minute prior to entering power down mode.

IMPLICATION : This problem will only slightly affect battery life.

WORKAROUND: No work around currently available. Limited characterization data was taken (three different lots, three units per lot) to estimate Ipd. The following data is not guaranteed, but should be characteristic of Ipd.



SYMBOL	PARAMETER	TYP (25°C)	TYP (0°C)
Itran	Transition current between Icc typical and Ipd	0.6 mA (5V) 0.175 mA (3V)	0.6 mA (5V) 0.175 mA (3V)
Ipd	Power down current	200 µA (5V) 50 µA (5V)	200 µA (3V) 50 µA (5V)
tsettle - tpd	Time for current to transition from Icc typical to Ipd	6 minutes (5V) 6 minutes (3V)	45 minutes (5V) 45 minutes (3V)

Actual battery life impact will vary dependent upon how often/long power down mode is used (during system suspend/off modes) along with storage temperature of the notebook.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: 8XC51SL-AH/AL CA stepping.

9600009. Power Management Data and Status Registers

PROBLEM: Power Management Data Register (address 7FEEh) and Power Management Status Register (address 7FEFh) can only be accessed when address pin A1 is in logic high state. Since the C51SL CPU has no control over the address pin A1, the C51SL CPU cannot access these registers as needed. However, the host CPU can still access these registers by setting address pin A1 to logic high.

IMPLICATION : Power Management Data and Status Registers are used for SYSTEM power management only. These registers do not impact the function of C51SL as a keyboard controller. The erratum does not affect “read” or “write” to other C51SL registers like the Keyboard Data Register (address 7FF1h) and Keyboard Status Register (address 7FF2h). It has no impact to existing software running on 8XC51SL-BG steppings (process P645) as these are new registers added to 8XC51SL-AH/AL.

WORKAROUND: No work around currently available. To configure the chip for use of all functions except the Power Management Register set, keep bit 6 (PMIFEN) of configuration Register 1 to a “0”, regardless of the value input to pin A1. The addresses 7FEEh and 7FEFh will then access external memory space rather than the internal Power Management Register set.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: 8XC51SL-AH/AL CA stepping.

96000010. 8XC51SL-AH/AL Interrupt Priority Erratum

PROBLEM: In 8XC51SL-BG devices, a low priority interrupt can itself be interrupted by a high priority interrupt, but not by another low priority interrupt. A high priority interrupt can not be interrupted by any other interrupt source. 8XC51SL-AH/AL is not fully compatible with 8XC51SL-BG on this. In 8XC51SL-AH/AL, group 1 interrupts are always have higher priority than group 0 interrupts when both groups are programmed with same interrupt priority level. In another words, group 0 interrupts can be interrupted by group 1 interrupts when both groups are programmed with same interrupt priority level as illustrated below:

Group 0 Interrupt Priority Bit, IP.x	Group 1 Interrupt Priority Bit, IP1.x	Comments
0	0	Group 0 interrupted by Group 1, errata
0	1	Group 0 interrupted by Group 1, normal
1	0	Group 1 interrupted by Group 0, normal
1	1	Group 0 interrupted by Group 1, errata

IMPLICATION: All the 8XC51SL-AH/AL devices (process P629) are affected, including CA (or A-2) stepping, DA (or A-3) stepping.

WORKAROUND: To prevent group 0 interrupts being interrupted by group 1 interrupts when both are programmed with same interrupt priority level because of the errata, a software work around can be implemented in group 0 interrupt service routine below:

```
GROUP0_ISR
        PUSH   IE1
        MOV    IE1,#00H        ;Mask out group 1 interrupts
          **********
        (execute service routine)
          **********
        POP    IE1
        RETI
```

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: 8XC51SL-AH/AL CA stepping, DA stepping.

SPECIFICATION CHANGES

None for this revision of this specification update.

SPECIFICATION CLARIFICATIONS

None for this revision of this specification update.

DOCUMENTATION CHANGES

None for this revision of this specification update.