Intel 430HX PCIset
82439HX (TXC)
Specification Update

February 1998

Order Number 297652-003

The Intel 82439HX (TXC) may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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REVISION HISTORY

Date of Revision	Version	Description
July 1996	-001	Initial Release.
October 1997	-002	Removed Specification Changes 1-8 and Errata 1-3. These are now documented in the public datasheet (290551-002) Added Documentation Change #1. Conversion to new template..
February	-003	Added Specification Clarification #1

PREFACE

This document is an update to the specifications contained in the Intel 82439HX (TXC), Intel 430HX PCIset 82439HX System Controller (TXC) Datasheet (290551), Intel 430HX PCIset 82439HX System Controller (TXC) Timing Specification, Datasheet Addendum (272945).

It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It contains Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the 82439HX (TXC) PCIset's, behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The 82439HX (TXC) may be identified by the following register contents:

82439HX Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A-1	8086h	1250h	01h
A-2	8086h	1250h	02h
A-3	8086h	1250h	03h

NOTES:

1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space.
3. The Revision Number correspond to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Specification Update for 82439HX (TXC)

GENERAL INFORMATION

This section covers the 82439HX (TXC).

Component Markings

82439HX (TXC)

Stepping	S-Spec	Top Marking	Freq.	Notes
A-3	S U115	82439HX S U115	66	Production
A-2	S U102	82439HX S U102	66	Production
A-1	S U087	82439HX S U087	66	Production

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed 82439HX (TXC).steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

82439HX TXC

NO.	A1	A2	A3	PLANS	SPECIFICATION CHANGES
					Specification Changes 1-8 have been incorporated into the Intel 430HX Datasheet. There are currently no additional known 82439HX (TXC) Specification Changes.
NO.	**A1**	**A2**	**A3**	**PLANS**	**ERRATA**
					Errata 1-3 have been incorporated into the Intel 430HX Datasheet. There are currently no additional known 82439HX (TXC) Errata.
NO.	**A1**	**A2**	**A3**	**PLANS**	**SPECIFICATION CLARIFICATIONS**
1	X	X	X	Doc	A[26:3] Strapping
NO.	**A1**	**A2**	**A3**	**PLANS**	**DOCUMENTATION CHANGES**
1	X	X	X	Doc	TIO[10] Use

82439HX (TXC) SPECIFICATION CHANGES

Specification Changes 1-8 have been incorporated into the Intel 430HX Datasheet. There are currently no additional known 82439HX (TXC) Specification Changes.

82439HX (TXC) ERRATA

Errata 1-3 have been incorporated into the Intel 430HX Datasheet. There are currently no additional known 82439HX (TXC) Errata.

82439HX (TXC) SPECIFICATION CLARIFICATIONS

1. A[26:3] Strapping

Section 2.1 of the datasheet, Host Interface, Identifies strapping options for A[31:28] and A[27]. No external strapping resistors, either external pull-up or pull-down resistors should be connected to A[26:3]. Incorrect system behavior may result.

82439HX (TXC) DOCUMENTATION CHANGES

1. TIO[10] Use

The TIO[10:8] group of section 2.3, Secondary Cache Interface of the Signal Description section incorrectly states when in 64MB cacheability mode, that TIO[10:8] are all unused and tied internally low to prevent them from floating. This only applies to TIO[9:8]. In this mode, TIO[10] is an I/O pin, meant for potential DRAM cache use, and it has no internal pull-up or pull-down resistor.

This section, described above will be replaced by the following text:

Extended Tag Address: For extended 512MB cacheability mode, these are inputs during CPU accesses and outputs during second level cache line fills and second level cache line invalidates due to inquire cycles. In this mode, TIO[10:8] contain the extension tag address to increase the cacheability limit to 512MB. This mode is enabled via the ECE bit of the CC register and an external pull-down resistor on TIO[10].

For 64MB cacheability mode, TIO[10] requires an external pull-up resistor and configuration of the CC register. In this mode, TIO[9:8] are unused. When TIO[10] is sampled HI at reset, this pin is an I/O pin, meant for potential DRAM cache use. TIO[9:8] have an internal pull-down resistor, TIO[10] does not have an internal pull-up or pull-down resistor.