Intel® 440BX AGPset: 82443BX Host Bridge/Controller

Specification Update

April 1999

Notice: The Intel® 82443BX may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Order Number: 290639-005

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release	May 1998
-002	Added Specification Changes #2 and #3.	July 1998
-003	Added Specification Changes #4, #5 and C1 Stepping Information.	October 1998
-004	Added Documentation Change #1	November 1998
-005	Added Documentation Change #2	April 1999

Preface

This document is an update to the specifications contained in the Intel® 440BX AGPset Datasheet, Revision 1.0, Order number 290633, and contains issues affecting all designs using the Intel 82443BX Host Bridge/Controller. It is intended for hardware system manufacturers. It contains Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the Intel® 82443BX, behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The Intel® 82443BX may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
B-1	8086h	7190h/7192h	02h
C-1	8086h	7190h/7192h	03h

NOTES:

1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space. The default value is 7190h. When AGP is disabled, the value is 7192h.
3. The Revision Number correspond to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.
4. The C-0 step device never entered production. As a result the C-1 step revision number ID remains 03h.

Component Marking Information

The Intel® 82443BX may be identified by the following component markings:

Stepping	S-Spec	Top Marking	Notes
B-1		FW82443BX Q628ES	Engineering Sample, FM Test
B-1		FW82443BX Q629ES	Engineering Sample, FM Test
B-1		FW82443BX Q630ES	Engineering Sample, T03 Test with Burn-In Full Production Flow
B-1	SL2T5	FW82443BX SL2T5	82443BX B-1 Production ASSY
C-1	SL2VH	FW82443BX SL2VH	82443BX C-1 Production ASSY
C-1	SL278	FW82443BX SL378	82443BX C-1 Remnants

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes which apply to the listed Intel® 82443BX steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

NO.	B1	C1	PLANS	SPECIFICATION CHANGES
1	X	X	DOC	Abort Disable Test Mode Configuration Bits
2	X	X	DOC	Selective Auto Precharge
3	X	X	DOC	Memory Data Buffer Strength Programming
4	X	X	DOC	Nand Tree testing
5	X	X	DOC	Processor PLL Lock Time

NO.	B1	C1	PLANS	ERRATA
1	X		FIX	Hard Reset Collision with Refresh
2	X		FIX	IPDLT Bit Setting
3	X		FIX	SDRAM Suspend Refresh
4	X		FIX	Refresh Collision with SUS_STAT# assertion (EDO Memory)

NO.	B1	C1	PLANS	SPECIFICATION CLARIFICATIONS
				There are currently no know 82443BX Specification Clarifications.

NO.	B1	C1	PLANS	DOCUMENTATION CHANGES
1		X	DOC	Marking Removed from C1 Stepping in Table of Changes Errata Section
2	X	X	DOC	Page iii is changed

Specification Changes

1. Abort Disable Test Mode Configuration Bits

Intel Reserved Register bits at offset F4h, bits 29 and 30 should be set to 1 for normal operation.

2. Selective Auto Precharge

Due to inconsistent behavior of the selective auto precharge feature with different SDRAM components, this feature will be removed from further revisions of the 82443BX External Design Specification. Bit 4 of the Paging Policy register, Offset 78-79h should be set to 0 (default). Bit 4 at Offset 78h will become an Intel Reserved bit location.

3. Memory Data Buffer Strength Programming

Characterization of the MD buffers has shown that the actual buffers are stronger than the simulated buffer strengths. As a result, new buffer strength settings are recommended in order to improve system noise margin. The new settings are described in the BIOS Specification Update, Rev 2.1 or later. Contact your local Intel Representative to obtain documentation.

4. 82443BX Nand Tree Testing

Intel® 82443BX Host Bridge/Controller Nand Tree Testing

This section provides information about the Nand tree testability features of the Intel 82443BX.

Test Mode Activation

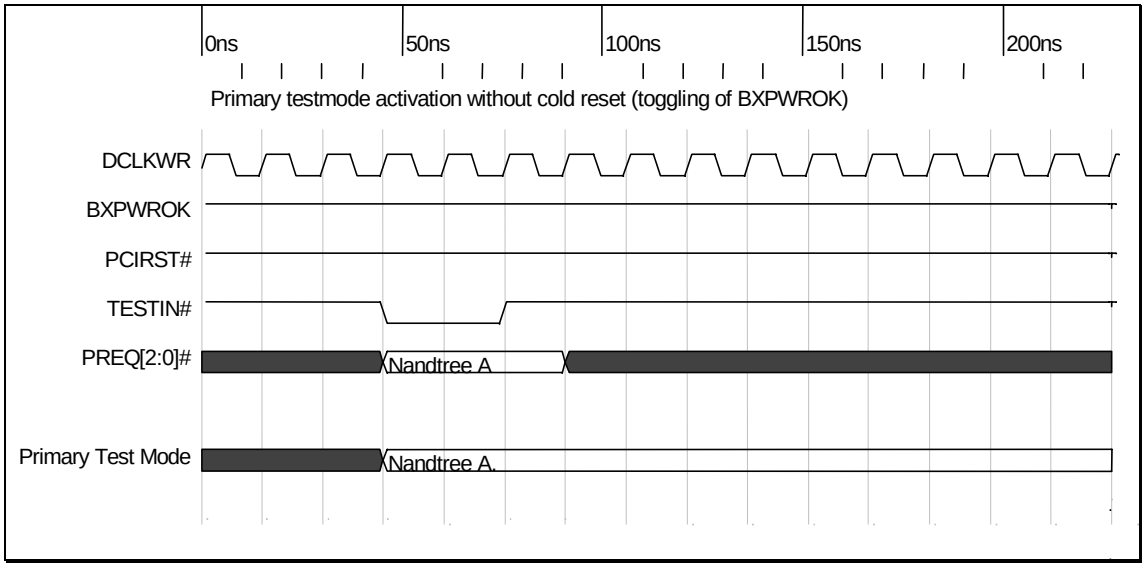
The primary test mode is enabled via TESTIN# pin. To enable a Nand Tree primary test mode, the TESTIN# input pin is asserted low and a 3-bit binary pattern is presented on the PCI PREQ[2:0]# input pins. Table 1 shows the PREQ[2:0]# signal encoding for Nand tree test modes enabled via the TESTIN# pin.

Table 1: Primary Test Modes

PREQ[2:0]#	Test Mode Enabled
000	Nandtree A
001	Nandtree B

The Figure 1 timing diagram shows the sequence required to enable a primary test mode. Note that the TESTIN# input pin acts as a latch enable, and the PREQ[2:0]# pins act as latch inputs. The test mode is decoded from the output of the latch.

Figure 1: Waveform of Primary Test mode



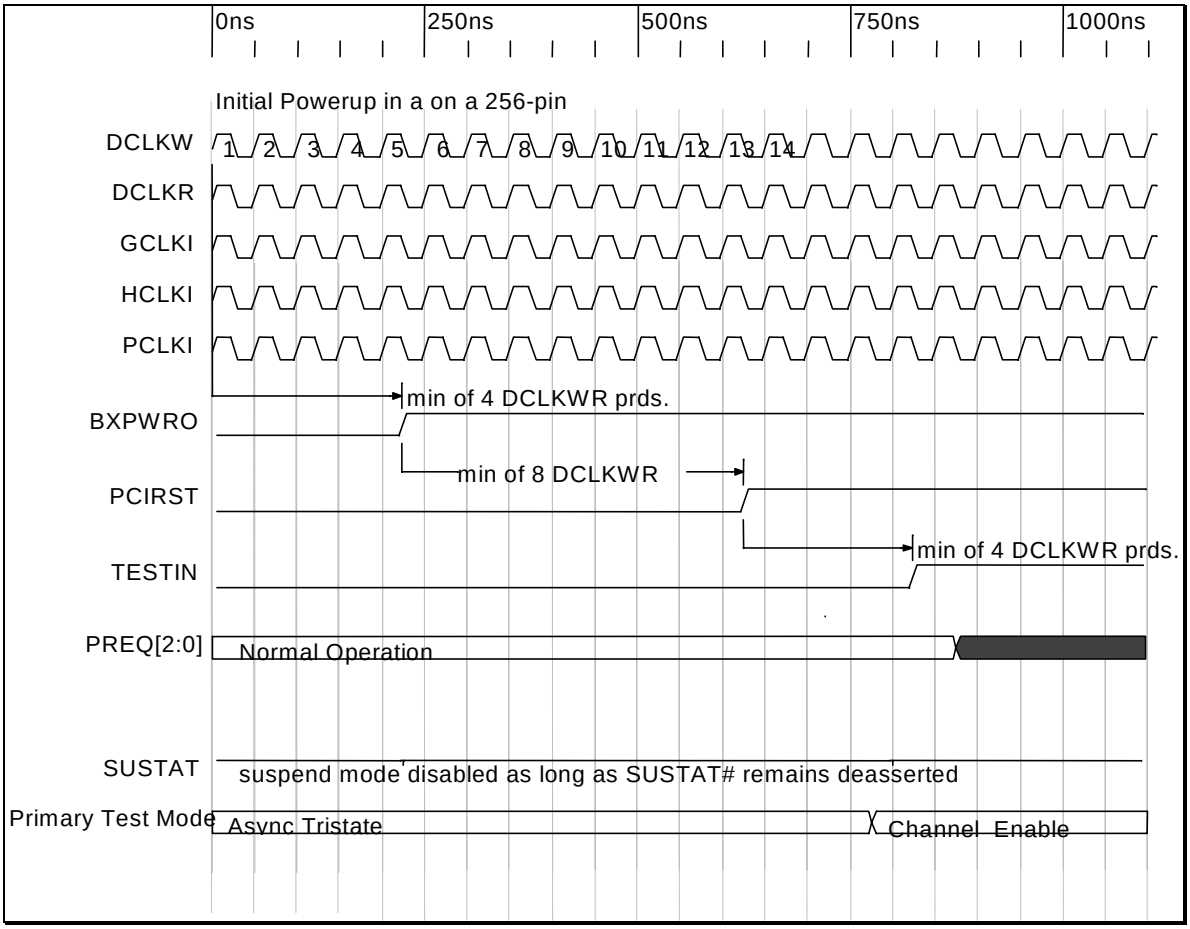
Tester Power-up Sequence

Figure 2 shows the typical power-up sequence of an 82443BX on a 256-pin tester.

At time 0, PCIRST# and TESTIN# must be asserted. The BXPWROK signal must also be asserted to indicate that a cold reset is in progress.

Once PCIRST# is deasserted, on the fourth DCLKWR positive edge, the TESTIN# can also be safely deasserted. PCIRST# and TESTIN# should not deassert at the same time because a race condition prevents the circuit from guaranteeing proper latching of primary test modes.

Figure 2: Typical power-up sequence



Primary Test Mode Details

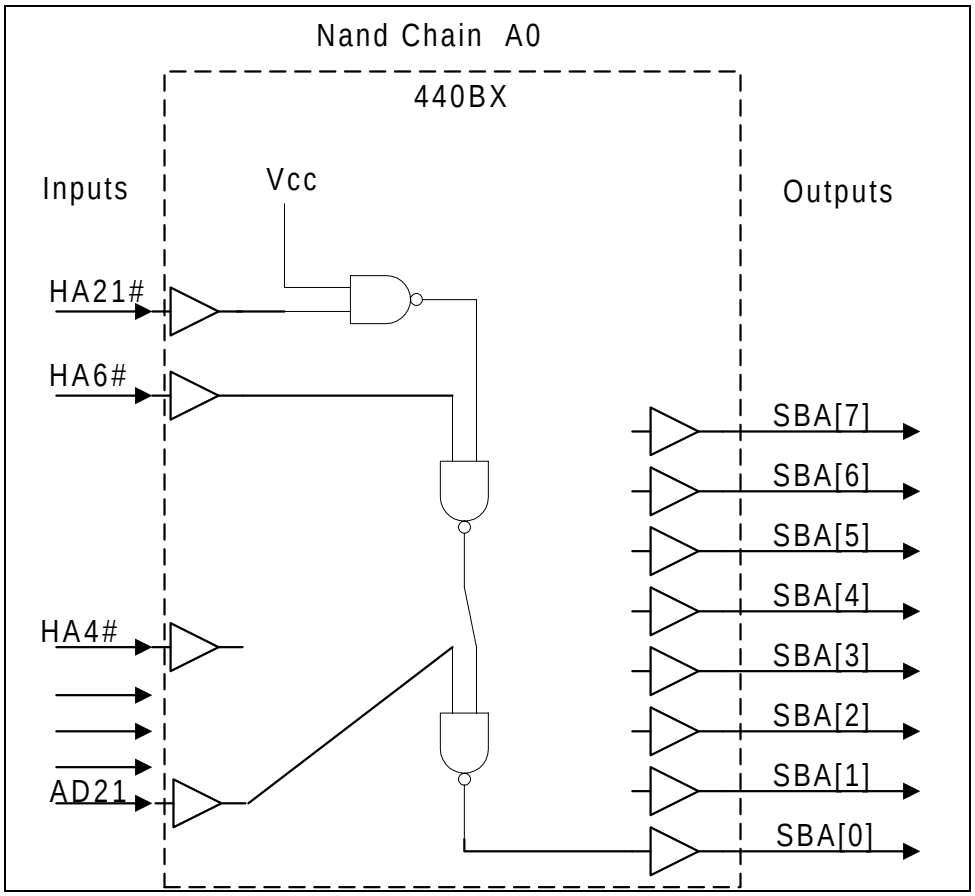
Nandtree A

The Nandtree A test mode is used for board level connectivity test. Its main purpose is to detect connectivity shorts between adjacent pins and to check proper bonding between I/O pads and I/O pins.

To help reduce the board level test cost, the Nand chain is limited to 60 pins per chain. This is accomplished by implementing 8 separate Nand chains.

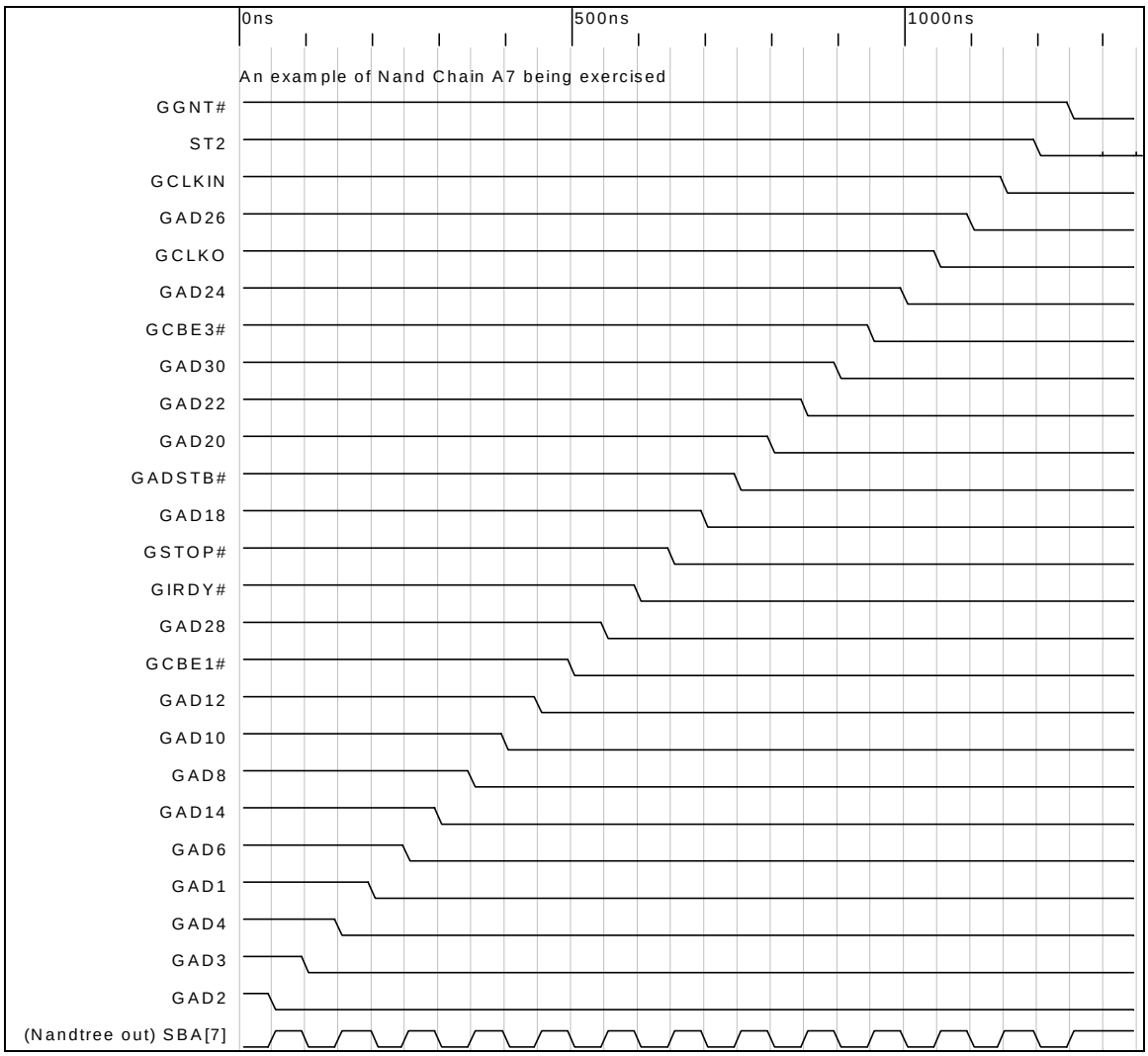
A conceptual diagram of the Nandtree is shown in figure 3.

Figure 3: Nand Chain A0 Connectivity



An example Nandtree test is shown in Figure 4. At first, all the input pins are driven to logic 1. Next, each input pin is driven to logic 0, in a sequence, so that the output pin, in this case SBA[0], toggles. By observing the Nandtree output pin, one can detect shorted and unconnected pins.

Figure 4: Waveform of Nand Chain #A7 Test



Nand chain pin assignments are shown in the following tables.

Table 2: Signals Not Included in Nandtree A or Nandtree B

Signals	Purpose
BXPWROK	Used for cold reset
PCIRST#	Used for cold and warm reset
TESTIN#	Used to enter Nandtree A and B test modes

Table 3: Nandtree A Outputs

Signals	Purpose
SBA[0]	Nand-Chain A0 Output
SBA[1]	Nand-Chain A1 Output
SBA[2]	Nand-Chain A2 Output
SBA[3]	Nand-Chain A3 Output
SBA[4]	Nand-Chain A4[1] and A8 Output
SBA[5]	Nand-Chain A5[1] and A9 Output
SBA[6]	Nand-Chain A6 Output
SBA[7]	Nand-Chain A7 Output

Legend for Table 3:

[1] - When MMO mode is disabled, Nandtree chains A4 and A5 are also deactivated. When MMO mode is enabled, Nand chains A4 and A5 are active during Nandtree A test mode. The output of Nandtree chains A4 and A5 (when MMO mode is enabled) must always go through chains A8 and A9, respectively, before it comes out on SBA[4] and SBA[5]. MMO mode is the MAB7# strap configuration controlling the “mobile mode operation”. When MMO mode is enabled the lower order Nand tree chains of the paired groups are also tested.

	Chain #A0		Chain #A1		Chain #A2		Chain #A3	
#	Pin Name	Pad#	Pin Name	Pad#	Pin Name	Pad#	Pin Name	Pad#
1	HA21#	111	HA15#	105	GNT3#	244	AD30	249
2	HA6#	114	HREQ0#	108	GNTO#	246	AD24	256
3	HA4#	116	HA18#	110	AD19	255	TRDY#	256
4	HA28#	119	HA23#	113	AD17	257	AD18	259
5	HA20#	121	HA31#	115	AD11	260	AD16	261
6	HA26#	131	BREQ0#	117	PAR	262	FRAME#	265
7	HA27#	133	HA10#	120	C/BE2#	263	IRDY#	267
8	HA30#	134	HA22#	123	AD15	266	AD12	268
9	HA24#	135	HD1#	129	STOP#	269	PLOCK#	270
10	CPURST#	137	HA11#	132	DEVSEL#	271	C/BE1#	275
11	HD32#	177	HD2#	138	SERR#	273	AD14	277
12	HD33#	179	HA29#	139	AD13	276	AD10	279
13	HD37#	181	HD4#	140	AD9	278	AD9	283
14	HD434#	182	HD0#	141	AD0	280	AD4	284
15	HD40#	183	HD3#	143	AD7	281	AD6	287
16	HD36#	185	HD8#	144	C/BEO#	285	AD2	288
17	HD35#	186	HD5#	145	AD5	289	AD1	291
18	HD44#	187	HD9#	146	AD3	290	CLKRUN#	373
19	HD34#	188	HD6#	147	MD34	382	WSC#	381
20	HD47#	189	HD7#	149	MD32	384	SUSTAT#	385
21	HD42#	191	HD10#	150	MD35	386	MD1	387
22	HD38#	192	HD12#	151	MD33	391	MD0	389
23	HD51#	193	HD14#	152	MD36	396	MD5	390
24	HD49#	194	HD15#	153	MD37	399	MD2	393
25	HD54#	195	HD17#	155	MD38	403	MD3	395
26	HD48#	197	HD11#	156	MD42	406	MD4	397
27	HD45#	198	HD18#	157	MD40	407	MD6	400
28	HD59#	199	HD13#	158	MD39	410	MD8	401
29	HD39#	200	HD20#	159	MD41	411	MD7	405
30	HD53#	201	HD16#	161	MD44	414	MD9	409
31	HD60#	203	HD21#	162	MD43	415	MD11	413
32	HD55#	204	HD19#	163	MD45	417	MD15	419
33	HD63#	205	HD22#	165	WEB#	427	MD10	420

34	HD41#	206		HD25#	167		SCASA#	433		MECC0	421
35	HD58#	207		HD23#	168		DQMA4	437		MD14	423
36	HD62#	209		HD26#	169		MD46	438		MECC1	424
37	HD46#	210		HD29#	170		MD47	442		MECC4	425
38	HD61#	211		HD27#	171		SCASB#	444		MD12	428
39	HD57#	212		HD31#	173		MAB0#	453		MECC5	429
40	HD52#	213		HD29#	175		MAB2#	457		WEA#	431
41	HD56#	215		HD24#	176		MAB4#	459		MD13	432
42	HD50#	216		HD30#	180		MAB1#	464		DQMA0	434
43	REQ1#	217		GNT1#	219		MAB5#	465		CSA1#	441
44	REQ0#	221		REQ4#	220		MAB8#	467		CSA2#	443
45	GNT2#	222		PHLDA#	226		MAB9#	473		CSA4#	445
46	PHOLD#	223		REQ2#	228		MAB11#	476		CSA3#	446
47	AD31	225		AD28	229		MAB12#	477		SRASA#	447
48	AD29	227		AD26	232		MAB3#	480		DQMA1	450
49	AD25	231		C/BE3#	235		MAB13#	481		SCA5#	451
50	GNTA4#	233		AD22	237		MAB6#	494		CSA0#	452
51	AD27	234		REQ3#	242		MAB7#	496		DQMA5	456
52	AD23	293		AD20	243		MAB10	498		CKE0	483
53	AD21	241		PCLKIN	245		DCLKWR	499		SRASB#	484

	Chain #A4	
#	Pin Name	Pad#
1	DQMB1	435
2	DQMB5	439
3	CKE3	488
4	CKE2	489
5	CKE4	491
6	CSB1#	495
7	CSB0#	497
8	CSB2#	501
9	CSB3#	3
10	CSB5#	5
11	DCLKO	6
12	CSB4#	9
13		
14		
15		
16		
17*		

Chain #A5	
Pin Name	Pad#
MAA0	449
MAA2	455
MAA4	458
MAA6	461
MAA5	463
MAA8	466
MAA9	469
MAA1	470
MAA10	471
MAA3	474
MAA11	475
MAA12	479
CKE1	485
CKE5	487
MAA7	490
MAA13	493
DCLKRD*	4*

*NOTE: Chain #A5, DCLKRD: This pad/pin was in use as part of this chain for the B1 stepping of the 82443BX. This pad/pin was removed from the chain for the C1 stepping. This should be the only chain that fails on the 82443BX C1 stepping if the 82443BX B1 stepping Nand tree test are used. All pins tested after DCLKRD will give the opposite data when testing an 82443BX C1 step device with the 82443BX B1 step Nand tree test.

To repair the Nand tree test of Chain #A5/#A9 (MMO enabled) for the 82443BX C1 stepping, remove DCLCKRD from the test and invert the expected data for all pins (MAA13, MAA7, CKE5, CKE1, MAA12, MAA11, MAA3, MAA10, MAA1, MAA9, MAA8, MAA5, MAA6, MAA4, MAA2, and MAA0) which were tested following the DCLKRD pin.

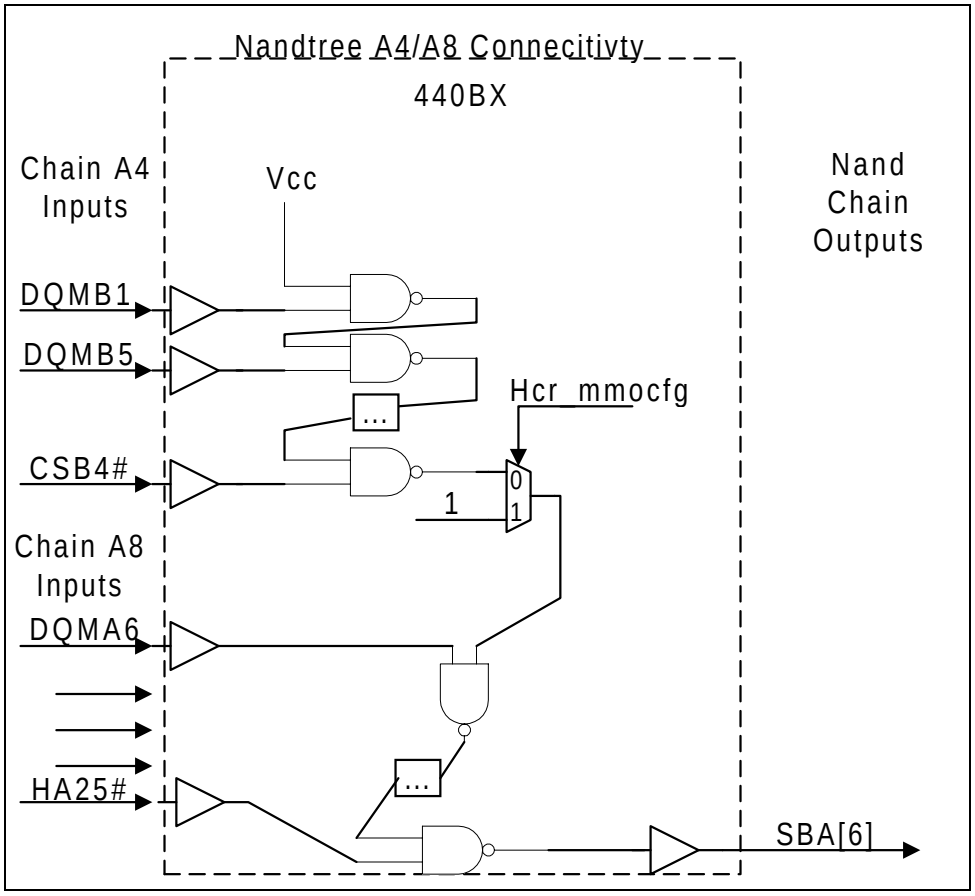
	Chain #A6	
#	Pin Name	Pad#
1	RBF#	292
2	GREQ#	294
3	ST1	295
4	PIPE#	299
5	ST0	302
6	SB-STB	305
7	GAD31	315
8	GAD29	317
9	GAD27	319
10	GAD23	322
11	GAD25	332
12	GAD17	333
13	GC/BE2#	335
14	GFRAME#	340
15	GTRDY#	341
16	GAD21	342
17	GPAR	345
18	GAD19	347
19	GAD15	350
20	GAD13	352
21	GDEVSEL#	355
22	GAD11	357
23	GAD7	361
24	GC/BE0#	362
25	GAD-STBA	365
26	GAD5	367
27	GAD9	370
28	GAD0	374

Chain #A7	
Pin Name	Pad#
GGNT#	293
ST2	298
GCLKIN	312
GAD26	323
GCLKO	324
GAD24	325
GC/BE3#	327
GAD30	328
GAD22	329
GAD20	331
GAD-STBB	336
GAD16	337
GAD18	339
GSTOP#	343
GIRDY#	346
GAD28	349
GC/BE1#	351
GAD12	353
GAD10	356
GAD8	359
GAD14	360
GAD6	363
GAD1	366
GAD4	369
GAD3	371
GAD2	375

	Chain #A8		Chain #A9	
#	Pin Name	Pad#	Pin Name	Pad#
1	DQMA6	8		
2	MECC2	13	DQMA2	7
3	DQMA7	15	DQMA3	11
4	MD50	18	MECC7	14
5	MD48	21	MECC6	17
6	MD49	27	MECC3	19
7	MD51	28	MD16	23
8	MD59	34	MD17	24
9	MD52	35	MD18	25
10	MD53	37	MD19	29
11	MD54	38	MD21	31
12	MD55	43	MD20	33
13	MD57	45	MD22	39
14	MD58	47	MD23	41
15	MD56	49	MD24	44
16	MD61	55	MD25	48
17	MD62	57	MD27	51
18	MD63	59	MD28	53
19	CRESET#	63	MD29	54
20	MD60	64	MD26	58
21	RS0#	69	MD31	61
22	RS2#	71	MD30	66
23	HREQ3#	75	RS1#	68
24	HREQ2#	77	HCLKIN	70
25	HREQ4#	81	HIT#	73
26	HREQ1#	83	DBSY#	76
27	BPRI#	85	DEFER#	79
28	BNR#	88	HITM#	82
29	HLOCK#	90	DRDY#	84
30	HA5#	93	HTRDY#	87
31	HA14#	95	HA9#	89

32	HA13#	97	HA3#	91
33	ADS#	101	HA7#	94
34	HA16#	104	HA8#	96
35	HA19#	107	HA12#	99
36	HA25#	109	HA17#	103

Figure 5: Waveform of Nandtree Chain Pair up (A4 and A8) & (A5 and A9)



Nandtree B

The Nandtree B test mode is used to test the SBA[7:0] pins. These pins are outputs during the Nandtree A test mode and are not tested in that mode. In Nandtree B test mode, the SBA[[7:0] signals become inputs and the CRESET# pin becomes the output.

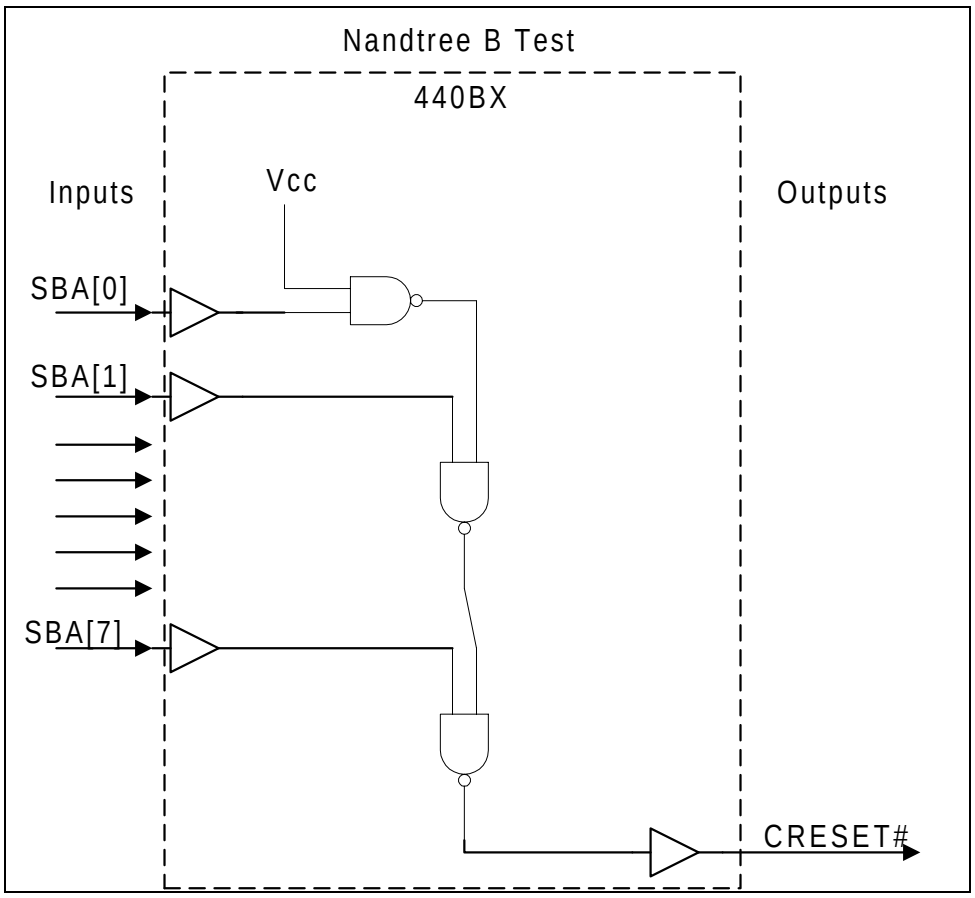
Table 5: Nandtree B Outputs

Signals	Purpose
CRESET#	Nand-Chain B0 Output

Table 6: Nandtree B Chain #B0

	Chain #B0	
#	Pin Name	Pad#
1	SBA0	297
2	SBA1	301
3	SBA2	303
4	SBA3	307
5	SBA4	308
6	SBA6	309
7	SBA5	311
8	SBA7	313

Figure 6: Diagram of Nandtree B Test mode



5. Processor PLL Lock Time Affects 82443BX

The 82443BX requires a minimum of 60uS between the deassertion of CPU__STP# and the deassertion of SUSTAT# for a CPU C3 exit. The 82443BX requires a minimum of 100uS between the deassertion of CPU__STP# and the deassertion of SUSTAT# for a cold boot.

The PIIX4/PIIX4E register CNTB-Count B (Function 3) at address offset 48h - 4Bh [10:6] (processor PLL lock count bits) and [5] (processor PLL lock resolution bit) control the processor lock time and resolution function. The default value of this register is 00h. These bits must be programmed to insure the 82443BX minimum time requirements between the deassertion of the signals are met.

Errata

1. Hard Reset Collision with Refresh

Problem: During a software generated hard reset, if a DRAM refresh cycle coincides with the activation of PCIRST#, the system will hang.

Implication: The system will hang.

Workaround: The system BIOS must disable refresh before generating the reset sequence. Refer to the 82443BX BIOS Specification Update for more details.

Status: This erratum will **not** be fixed in the B-1 stepping of the 82443BX. This erratum will be fixed in the C-0 stepping of the 82443BX.

2. IPDLT Bit Setting

Problem: System validation has uncovered a marginal internal timing path.

Implication: An incorrect address may be driven on the DRAM bus, resulting in memory data being fetched from the wrong location.

Workaround: The IPDLT bits (register offset 76h, bits 8 and 9) should be set to 01 (i.e. set bit 8 to 1).

Status: BIOS workaround (configuration register change). This erratum will also be fixed in the next stepping of the 82443BX.

3. SDRAM Suspend Refresh

Problem: This erratum may occur in Intel 440BX chipset platforms that implement suspend or Stop Clock (C3) states. Platforms that are affected include mobile SDRAM platforms using module MM-config mode (single CKE) and 4 DIMM desktop platforms using GCKE.

These platforms require the 440BX memory controller to stop the normal refresh and place the SDRAM in a self-refresh mode before the system transitions to one of these states. If the self-refresh trigger (SUSTAT1# signal asserted) occurs at the same time as an internally generated normal refresh request, the 440BX generates an incorrect CKE# and CS# signal sequence to the SDRAM. The SDRAM is not placed in self-refresh mode and memory contents may be lost.

Mobile SDRAM platforms using normal mode (not MM-config) and 3 DIMM desktop platforms are not affected. 4 DIMM desktop platforms that do not use GCKE are also not affected.

Implication: The observed effect of the erratum is a system hang, although data loss or corruption is theoretically possible.

Workaround: APM BIOS workaround:

POS, POSCCL, POSCL, STR and C3 states
The workaround disables normal refresh prior to entering these states and before the 443BX automatically generates the SDRAM self-refresh command. BIOS will re-enabling normal refresh on exit from these states.

ACPI BIOS workaround (TBD):

Status: Implement BIOS workaround. This erratum will also be fixed in the next stepping of the 82443BX.

4. Refresh Collision with SUS_STAT# assertion (EDO Memory)

Problem: On entry to STR or POSCL in a system with EDO memory, if SUSSTAT1# is asserted at the same time a DRAM refresh cycle occurs the normal refresh state machine is left in an improper state. Refresh control is transferred to the suspend refresh state machine which is not affected. When the system resumes from STR, refresh control is returned to the normal refresh state machine which is in an improper state.

Implication: The system will hang, typically with RAS# stuck high and CAS stuck low. During the execution of the resume code, operation will continue until the BIOS sets the NREF_EN bit to a 1 (443BX, Device#0, Register Offset 7Ah, bit4).

Workaround: A BIOS workaround consisting of aligning the occurrence of the 443BX north bridge refresh cycles away from the transitions of PIIX4 south bridge SUSCLK# (which controls the assertion of SUSSTAT#) is available.

Status: Implement BIOS workaround. This erratum will also be fixed in the next stepping of the 82443BX.

Specification Clarifications

There are currently no known 82443BX Specification Clarifications.

Documentation Changes

1. Marking Removed from C1 Stepping in Table of Changes Errata Section.

Marking in C1 Stepping “Table of Changes” Errrata Section in the previous release of Intel® 440BX Specification Update document does not apply.

2. Page iii, Intel 82443BX Features list, of the 440BX AGPset: 82443BX Host Bridge/Controller Data Sheet.

The “Integrated DRAM controller” section of the Intel 82443BX Features list on page iii of the Intel® 440BX AGPset: 82443BX Host Bridge/Controller data sheet is changed as follows:

The first item is changed to read:

“--- 128Mbit SDRAM technology is supported as stated in para 4.3 of page 4-14 of this document. As a result, 8Mbytes to 1Gbyte of memory is available depending on system implementation.”

The last item is changed to read:

“--- Enhanced SDRAM Open Page Architecture Support for 16-, 64-, and 128-Mbit SDRAM technology devices with 2K, 4K, and 8K page sizes.”

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