Intel 430TX PCIset 82439TX MTXC Specification Update

March 1998

Order Number: 290615-001

The Intel 82430TX PCIset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
March 1998	-001	Initial Release.

PREFACE

This document is an update to the specifications contained in the Intel 430TX PCIse 82439TX System Controller (MTXC) Datasheet (Order Number 290559-001) This document is intended for hardware system manufactures and software developers of applications, operating systems or tools. It contains Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Nomenclature

Specification Changes are modifications to the specifications of the Intel 430TX PCIset. These modifications will be reflected in the future releases of the affected specification.

Errata are design defects or errors. Errata may cause the Intel 82439TX PCIset's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The 82439TX MTXC stepping can be identified by the following register contents:

82439TX MTXC Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A-0	8086h	7100h	00h
A-1	8086h	7100h	01h
A-2	8086h	7100h	01h

NOTES:

1. PCI function 0 configuration space.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space.
3. The Revision Number correspond to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space. The Revision Number remains 01h for the A-2 stepping.

Specification Update for
Intel 430TX PCIset
82439TX MTXC

General Information

The information in this section applies to the 82439TX MTXC.

Component Markings

430TX PCISET IDENTIFICATION INFORMATION

Stepping	S-Spec	Top Marking	Freq.	Notes
A-0		FW82439TX Q516ES	66/33	Engineering Sample
A-0		FW82439TX Q517ES	66/33	Engineering Sample
A-1		FW82439TX Q536ES	66/33	Engineering Sample
A-1		FW82439TX Q537ES	66/33	Engineering Sample
A-1		FW82439TX S L238	66/33	Production
A-2	Q562	FW82439TX Q562ES	66/33	Engineering Sample
A-2	SL28T	FW82439TX S L28T	66/33	Production
A-2	Q557	FW82439TX Q557ES	66/33	Engineering Sample

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed Intel 440TX PCIset steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

82439TX MTXC

NO.	A0	A1	A2	PLANS	SPECIFICATION CHANGES
1	X	X	X		There are currently no known Specification Changes.
NO.	**A0**	**A1**		**PLANS**	**ERRATA**
1	X	X	X	NoFix	SDRAM Speculative Read Enable (SSRE)
2		X		Fix	Address Setup Time
3		X	X	NoFix	Fast Back-to-Back, Peer to Peer cycle
NO.	**A0**	**A1**	**A2**	**PLANS**	**SPECIFICATION CLARIFICATIONS**
1	X	X	X	Doc	Insuring Signal integrity in a lightly loaded systems
2		X	X	Doc	Insuring Correct Setting for Register Offset 53h
3		X	X	Doc	Bits 4 and 5, Register Offset 52h Clarification
4		X	X	Doc	MTXC Power Plane Sequencing
5	X	X	X	Doc	Timing of the SUSCLK and SUS_STAT# Signals For Resume Voltage Well Reset
NO.	**A0**	**A1**	**A2**	**PLANS**	**DOCUMENTATION CHANGES**
1		X	X	Doc	NAND Chain Mode
2		X	X	Doc	DRAMT - DRAM Timing Register Description
3	X	X	X	Doc	Vcc5REF Sequencing Circuit
4	X	X	X	Doc	SDRAM Performance Summary
5	X	X	X	Doc	SDRAM Control Register Bit 1 Description

82439TX (MTXC) SPECIFICATION CHANGES

There are currently no known 82439TX (MTXC) Specification Changes.

82439TX (MTXC) ERRATA

1. SDRAM Speculative Read Enable (SSRE)

PROBLEM: Due to a timing marginality during SDRAM read-page-hit cycles, the SSRE mode does not function properly and must be disabled. This mode provided a five clock read lead off during CPU read-page-hit cycles to main memory. This mode impacts SDRAM only.

IMPLICATION: If SSRE mode is enabled, the system may not function properly. Intel has tested this mode and found the performance impact of disabling the SSRE mode is minimal using the 430TX reference platform with 200MHz Pentium® processor with MMX™ technology, 16MB SDRAM, 512K PBSRAM L2, and hard drive in PIO Mode 4,

WORKAROUND: This errata is avoided by disabling the SSRE mode by clearing bit 7 in register offset 56h to “0”. This bit has been changed to a reserved bit and must always remain in its default state (0).

STATUS: There are no plans to fix this erratum.

2. Address Setup Time

PROBLEM: Intel’s 430TX external timing specification (ETS) specifies that the PCI address setup to the MTXC is 7.0ns. However, it has been determined that the MTXC requires a 7.7ns address setup on PCI AD lines 30 and 31.

IMPLICATION: If the PCI address setup to the MTXC is not met, then the MTXC will not complete the cycle correctly. This may result in a system failure or data error which is not immediately visible to the end user. There is no test currently available to expose this type of error to the end user, therefore, it is essential that the new timing requirement is met.

In a system with a 33Mhz PCI bus, the setup time is generated within a 30ns window. The delay components within this window are: valid delay, flight time, and PCI clock skew (the specific equation is: 30ns - valid delay - flight time - PCI clock skew - setup). In general, the OEM has control of the flight time and clock skew. Both of these delay components often have additional margin which should compensate for the increased timing requirement on the MTXC. OEM’s should evaluate their board designs to determine if additional clock skew and/or flight time margin is available.

WORKAROUND: The design should be laid-out in such a manner to compensate for the MTXC’s increased timing requirement. OEM’s should examine their existing designs to determine if their specific PCI flight time and PCI clock skews will provide sufficient timing margin.

To check your design for adequate margin:

1. Measure the PCI Clock Skew between the MTXC PCI Clock and the other PCI Clocks in your system. If the MTXC PCI clock lags behind the other PCI clocks, this issue should not be a problem. If the MTXC PCI clock leads the other PCI clocks by less than 1.3ns, this issue should not be a problem. This is assuming that all other parameters, external to the MTXC component, meet PCI bus timing requirements. The maximum skew is measured between any two components, not at the PCI connector. For example, if the measurement is being made between the MTXC and a PCI device in a slot, make the measurement from the MTXC to the device on the PCI card, and not to the connector the card is plugged in to. The measurements are generally made at the 1.5v to 1.5v level. However, refer to the PCI specification rev 2.1, section 4.3.1 for precise measurement points.
2. To get an idea of how much PCI flight time margin a particular system has – First make sure that your PCI bus is fully loaded (i.e. populate all of the slots). In general, the flight time is at its worst between the two devices on the bus that are furthest away from each other. However, for a complete measurement, check the PCI device nearest to, and furthest from the MTXC, excluding the PIIX4.

The maximum flight time is measured between any two components, not at the PCI connector. For example, when measuring the flight time, measure AD31 at the MTXC , on one probe, and AD31 at the initiating PCI device, on a second probe. The difference between these two measurements will give you the flight time on this line. For these measurements, the PCI master should be driving the address lines. Repeat the measurement for AD30. The measurements can be made from the 1.5v to the 1.5v level.

STATUS: This erratum is intended to be fixed in a future stepping of the component.

3. Fast Back-to-Back, PCI Peer-to-Peer Cycles

PROBLEM: If a fast back-to-back cycle occurs on the PCI bus between the same master peer device and the same slave peer device (i.e. MTXC and PIIX4 are not the intended targets), and at the same time a CPU cycle to PCI occurs, the MTXC may miss the second peer-to-peer cycle in the back-to-back sequence. The specific conditions that need to be met for this to occur, are as follows:

1. The PCI peer-to-peer, back-to-back transfer must happen at the same time the CPU is generating a host cycle to PCI. Specifically, between the rising edge of the first FRAME# (associated with the first cycle of the back-to-back transfer) to the rising edge of the second FRAME# (associated with the second cycle in the back-to-back transfer).
2. The PCI back-to-back transfer must be peer-to-peer and the transfer must not be targeting the PIIX4 or the MTXC.
3. The PCI master must be capable of running “fast” back-to-back cycles.
4. The second cycle of the back-to-back transfer must be targeting the same PCI slave device.
5. The PCI slave device must be doing a “fast” decode.
6. The first cycle in the back-to-back transfer must be a single transfer.
7. The first cycle in the back-to-back transfer must be a PCI write cycle (memory or I/O).

IMPLICATION: Intel observed this issue in a system simulation environment.

WORKAROUND: If deemed necessary by the OEM, this issue can be avoided by clearing bit 3 in register offset 50h to “0”. When set to “0”, this bit prevents CPU bus access during PCI peer-to-peer transfers.

STATUS: There are no plans to fix this erratum.

82439TX (MTXC) SPECIFICATION CLARIFICATIONS

1. Insuring Signal Integrity in a lightly loaded Systems

To insure that DRAM interface signal integrity is maintained for lightly loaded Mobile and desktop systems, series termination and/or diodes (Gnd and Vcc diodes) are recommended on the following signals: CAS#/DQMx, MWEx, SCASx, SRASx, CKEx, and all MA lines (note: RAS4# and RAS5# are also used as MA lines, depending on the configuration, and should be terminated when used as MA lines). This will insure that the overshoot, undershoot, and most importantly, ring-back does not cause any problems.

If series termination is used, use 10 ohms. This value provides the best signal integrity and flight time results. Place as close to the driver as possible. If diodes are used, the diodes should have a forward current of at least 200ma at 1 volt. A MMBD1203 diode or equivalent meets this requirement. The diodes should be placed at the end of the trace.

Diodes improve signal integrity without increasing the flight time. A 10 ohm series resistor will increase the flight time by approximately 300ps. Both provide similar signal integrity results.

2. Insuring Correct Setting for MTXC Register Offset 53h (CEC)

During normal operation, the value programmed into register offset 53h should not be changed from its default value of 14h. This register controls the time the MTXC remains idle during a DRAM Cache refresh.

3. Bits 4 and 5, Register Offset 52h Clarification

1. In the bit description for these two bits, “Pipelined Burst SRAM” (bits 5:4 = 00) also applies to a 512k L2 size when two 64kx32 SRAM devices are used.
2. The “Note:” in the register description for these to bits should be replaced with the following: When 512k, Two Banks of Pipelined Burst mode is selected (SCS = 10 and L2SRAMT = 11), NA# will be delayed by one HCLK during burst reads from L2 to ensure that the active bank is not de-selected too early by pipelining a cycle to the opposite bank.

4. MTXC Power Plane Sequencing

The following clarifies the MTXC power plane sequencing requirements described on page 10 of the MTXC EDS Rev. 1.0. In a system that implements VCC(CORE) and VCC(CPU) as independent power planes, the VCC(CPU) pins must power up after or simultaneous to VCC(CORE), and must power down before or simultaneous to VCC(CORE). At any time, VCC(CORE) should not be more than 1.2 volts below the VCC(CPU) plane. VCC(SUS) can power up and power down independent of all other power planes.

5. Timing Of The SUSCLK And SUS_STAT# Signals For Resume Voltage Well Reset

The following information is added as paragraph 4.6.2.2, MTXC Resume Voltage Well Reset, to the MTXC Data Book, Order Number 290559-001: The MTXC will transition from suspend refresh to normal refresh when it samples SUSCLK active (high) with the first sample of SUS_STAT# inactive (high). Samples are taken on the rising edge of the PCI clock. The MTX will reset its resume well (DRAM configuration registers go to default settings) when it samples SUSCLK inactive (low) with the first sample of SUS_STAT# inactive (high). The mechanism which allows this functionality is based on the PIIX4 deasserting the SUS_STAT# signal in relation to the SUSCLK, synchronized to the PCI clock. To not reset the suspend well within the MTXC, the PIIX4 will drive the SUS_STAT# signal just after the SUSCLK signal has gone high. To reset the resume well within the MTXC, the PIIX4 will drive the SUS_STAT# signal while the SUSCLK is disabled (low). Because of this functionality, SUSCLK should not be inverted for any reason in applications.

82439TX (MTXC) DOCUMENTATION CHANGES

The Documentation Changes listed in this section apply to the 82439TX (MTXC).

1 NAND Chain Mode

The pin name associated with CH3_25 should be MWE#, not MWEB# as shown on page 83 of the MTXC Data Sheet and page 65 of the MTXC EDS Rev 1.0.

2. DRAMT - DRAM Timing Register Description

The description for DRAMT - DRAM Timing Register, offset 58h, bits 6:5, should read as follows:

Bit	Description
6:5	**DRAM Read Burst Timing (DRBT).** The DRAM read burst timings are controlled by the DRBT field. Slower rates may be required in certain system designs to support loose layouts or slower memories. Most system designs will be able to use one of the faster burst mode timings. The timing used depends on the type of DRAM on a per-bank basis, as indicated by the DRT register.

DRBT	EDO Burst Rate	FPM Burst Rate
00	x444	x444
01	x333	x444
10	x222	x333
11	Reserved	Reserved

3. Vcc5REF Sequencing Circuit

Page 16, paragraph 2.4, Figure 2. “Example Vcc5REF Sequencing Circuit”, of the “Intel 430TX PCIset: 82439TX System Controller (MTXC)” data book (Order Number 290559-001), shows a Zener diode symbol between the 3.3V Vcc supply and the 5V supply. This is incorrect. The following should be implemented to correct this circuit:

1. The diode used in this circuit should be a Schottky diode (or any diode with a forward voltage drop of no more than 0.4V) and the symbol shown should be a Schottky diode symbol.

The reason for this correction is to provide circuit protection in case of 5V power loss.

4. SDRAM Performance Summary

Page 61, Table 18, “SDRAM Performance Summary”, of the “Intel 430TX PCIset: 82439TX System Controller (MTXC)” datasheet, Order Number 290559-001, is changed to correct typographical errors as shown below:

Table 18. SDRAM Performance Summary

Processor Cycle Type	60/66 MHz CL=3 Five Rows (Max)	60/66 MHz CL=2 Five Rows (Max)
Burst Read Page Hit	7-1-1-1	6-1-1-1
Read row Miss[1]	9-1-1-1	8-1-1-1
Read Page Miss	12-1-1-1	11-1-1-1
Back-to-Back Burst Reads Page Hit	7-1-1-1-2-1-1-1	6-1-1-1-2-1-1-1
Write Page Hit[2,3]	3	3
Write Row Miss[2,3]	6	5
Write Page Miss[2,3]	9	8
Posted Write[2,3]	3-1-1-1	3-1-1-1
Write retire rate from Posted Write Buffer	-1-1-1	-1-1-1
Reg 54h, Bit 5 (RCO)[5]	1	0
Reg 54h, Bit 4 (CL)	0	1
Reg 54h, Bit 3 (RT)	0	1
Reg 56h, Bit 4 (SLD)[4]	0	0

NOTES:

1. The row miss cycle assumes that the new page is closed from the prior cycle.
2. This cycle timing assumes the write buffer(DWB) is empty.
3. Write data is always posted as 3-1-1-1 (ADS# to BRDY#), if write buffers is available.
4. This bit (SLD) must be set to a 1 (speculative leadoff disable) in systems with cache and to 0 in systems without cache.
5. For a CL=3 part that can not meet a RAS to CAS timing (Trcd) of two HCLKs, RCO can be set to 0. This will add an HCLK to the leadoff cycle for Row miss and Page miss cycles.

5. SDRAM Control Register Bit 1 Description

Page 30 of the “Intel 430TX PCIset: 82439TX System Controller (MTXC)” data book (Order Number 290559-001), in the description of bit 1 of the SDRAM Control Register, the portion of the description relative to when the bit is set to 1: The sentence, “In this mode, the RAS#/CS5# signal becomes RAS#/CS5#/MA13 ...” is corrected to read, “In this mode, the RAS5#/CS5# signal becomes RAS5#/CS5#/MA13 ...”