PC SDRAM Specification

Revision 1.63

October 1998

Order Number: Not Applicable

THIS SPECIFICATION IS PROVIDED "AS IS" WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NONINFRINGEMENT, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION OR SAMPLE. Intel disclaims all liability, including liability for infringement of any proprietary rights, relating to use of information in this specification. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted herein.

Copyright © Intel Corporation 1996, 1997.

*Third-party brands and names are the property of their respective owners.

Revision 1.63

Contents

1.0 Introduction 1
1.1 Objective 1
1.2 Scope of This Document 1
1.3 Convention Used 1
2.0 Pinout and Signal Description 2
2.1 Device Pinouts 2
2.2 Signal Descriptions (Simplified) 6
3.0 Basic Functional Description 7
3.1 Mode Register and the Modes Required to be supported 7
3.2 Command Truth Table 8
3.3 Address Bit Maps 14
3.3.1 16M Address Bit Maps For Row And Column Addresses During Commands 14
3.3.2 64M Address Bit Maps for Row and Column Addresses During Commands 15
3.4 Power-Up and Initialization Sequence 15
3.4.1 Power Up Sequence 15
3.4.2 Initialization Sequence 16
3.5 Precharge Selected Bank 16
3.6 Precharge All 17
3.7 NOP and Device Deselect 17
3.8 Row activate 17
3.9 Read Bank 18
3.10 Write Bank 18
3.11 Mode Register Set Command 18
4.0 Essential Functionality for the “PC SDRAM” Device 20
4.1 Burst Read and Burst Write 20
4.2 Multibank Ping Pong Access 21
4.3 Read and Write With Autoprecharge 22
4.4 Precharge Termination of Burst 22
4.4.1 Precharge Command After a Burst Read 22
4.4.2 Precharge Termination of a Burst Read 23
4.4.3 Precharge Command After a Burst Write 24
4.4.4 Precharge Termination of a Burst Write 24
4.5 Read Terminated By Read 24
4.6 Write Terminated By Write 25
4.7 Read Terminated By Write 25
4.8 Write Terminated By Read 26
4.9 SDRAM Commands, To Two Or Four Banks, In Consecutive Clocks 27
4.10 Next Command To Same Bank After Precharge 27
4.10.1 Precharge Bank 27
4.10.2 Precharge All 27
4.10.3 Read-Auto_Precharge 27
4.10.4 Write-Auto_Precharge 27
4.11 Concurrent Precharge Commands To Multiple Rows 27

4.12 Back to back Command With Auto Precharge 28
4.13 DQM# Latency 30
4.14 Back to Back Command Support 30
4.15 Auto Refresh (CBR) Command 30
4.16 Self Refresh Entry/Exit 31
4.17 Low Power ICCLP 32
4.18 Non-Required SDRAM Functionality 32
4.19 Multibank Operation 32

5.0 Synchronous DRAM AC/DC Parameters 41

5.1 DC Specifications 41
5.2 A.C. Specifications 43
5.3 IBIS: I/V Characteristics for Input and Output Buffers 43
5.4 IBIS Reference 48
5.5 A.C. Timing Parameters 49
5.6 Device Options 50
5.7 Output Load Specification 53
5.8 100 MHz Active Power in Application 54

Figures

1 Pin Assignment for 16M Devices (2Mx8, 4Mx4) 2
2 Pin Assignment for 16M Device (1Mx16) 3
3 Pin Assignment for 64M/128M Devices (16Mx4, 8Mx8, 4Mx16, 16Mx8, and 8Mx16) 4
4 Pin Assignment for 256M Devices (16Mx16, 32Mx8, and 64Mx4) 5
5 Power Up Initialization Sequence 16
6 Row Activate, Read and Precharge 18
7 Mode Register Set Command 19
8 Read and Write Commands (Burst Length 4 Shown) 21
9 Two Bank Ping Pong Read 22
10 Precharge Command After Burst Read 23
11 Read Terminated by Precharge (Outputs DQM# Controlled) 23
12 Precharge Command after Burst Write 24
13 Precharge Command After Write 24
14 Read Terminated By Read 25
15 Write Terminated with Write 25
16 Read Terminated By Write 26
17 Write terminated by Read (CL=2) 26
18 Read Command with Auto Precharge (BL=4) 28
19 Read Command with Auto Precharge (BL=1) 28
20 Write Command With Autoprecharge (BL=4) 29
21 Write Command With Autoprecharge (Bl=1) 29
22 DQM# Latency, Read Cycle 30
23 DQM# Latency, Write Cycle 30
24 Auto Refresh and Precharge All Command 31
25 Self Refresh Entry and Exit 31
26 Low Power ICCLP 32
27 Multibank Timing Relationship Diagram A 33
28 Multibank Timing Relationship Diagram B 33
29 Multibank Timing Relationship Diagram C 33
30 Multibank Timing Relationship Diagram D 34
31 Multibank Timing Relationship Diagram E 34
32 Multibank Timing Relationship Diagram F 34
33 Multibank Timing Relationship Diagram G 35
34 Multibank Timing Relationship Diagram H 35
35 Multibank Timing Relationship Diagram I 35
36 Multibank Timing Relationship Diagram J 36
37 Multibank Timing Relationship Diagram K 36
38 Multibank Timing Relationship Diagram L 36
39 Multibank Timing Relationship Diagram M 37
40 Multibank Timing Relationship Diagram N 37
41 Multibank Timing Relationship Diagram O 37
42 Multibank Timing Relationship Diagram P 38
43 Multibank Timing Relationship Diagram Q 38
44 Multibank Timing Relationship Diagram R 38
45 Multibank Timing Relationship Diagram S 39
46 Multibank Timing Relationship Diagram T 39
47 Multibank Timing Relationship Diagram U 39
48 Multibank Timing Relationship Diagram V 40

49 Multibank Timing Relationship Diagram W 40
50 Multibank Timing Relationship Diagram X 40
51 Multibank Timing Relationship Diagram Y 41
52 Multibank Timing Relationship Diagram Z 41
53 SDRAM VSS Clamp Characteristics 44
54 SDRAM VCC Clamp Characteristics 45
55 SDRAM DQ Output Buffer Pull-Down Characteristics 46
56 SDRAM DQ Output Buffer Pull-Up Characteristics (For VCC = 3.0v - 3.45v) 47
57 A.C Timing Parameters 51
58 Read Cycle with timing 51
59 Write Cycle with timing 52
60 Output Load Circuit 53

Tables

1 Pin Functional Description (16M bit devices) 6
2 Latency Mode (LT Field) 7
3 Wrap Type (WT Field) 7
4 Burst Length (BL Field) 7
5 Burst Address Ordering for Burst Length (BL=1,2,4) 7
6 Command Truth Table 8
7 DQM# Truth Table 9
8 Operative Command Table 9
9 Row/Column Addresssing Per Memory Size/# Banks 13
10 Row Address Table (ACT, PRE) 14
11 Column Address Table (Read/Write/Read AP/Write AP) 14
12 Row Address Table (ACT, PRE) (per JEDEC Standard) 15
13 Column Address Table (Read/Write/Read AP/Write AP) 15
14 Partial list of Timing Paramters for Multibank Timing Relationship Diagrams (Figure 27 to Figure 51) 32
15 Absolute Maximum D.C. Rating 41
16 D.C Operating Requirements 42
17 Maximum AC Operating Requirements 43
18 Refresh Rate 43
19 SDRAM DQ Buffer Output Drive Characteristics 43
20 Data Points For Figure 53 44
21 Data Points For Figure 54 45
22 Data Points For Figure 55 46
23 Data Points For Figure 56 47
24 100/66 MHz AC Timing Parameters For CL=2 and 3 49
25 Matrix for 66 MHz Devices and The Target for 100 MHz Devices 50

Revision History

Rev.	Description
1.63	• Document Re-formatting. No specification content changes
1.62	• Add 7.8usec refresh rate for 256M Devices
1.61	• Add 256M Pinout • Add 64Mx4 Addressing definition • Remove 64M 2 bank addressing definition • Added: Clock will stabilize within 100usec before 1st command to SDRAM
1.6	• *Add 256M bit addressing* • *Set 64M 4 Bank Precharge Table, A11=A12, A12=A13* • *Set Troh=CL as max value , not min* • *Clarify Tambient operation conditons*
1.51	• Corrected 64M/128 Pin out Pin45/46 • Iccslfrf current changed to 1ma • Cin to be measured at 23C, 1Mhz, 1.4v bias, 200mv swing, Vcc = 3.3v • Trise/Tfall times to be characterized into 50pf, values given • Changed Vin/Vout max from VDD+0.5V to 4.5V • Changed tohz max (66Mhz) from 9ns to 12ns
1.5	• 128M bit Pin out (54pin TSOP) • 128M bit Addressing Support • Change Power Up Sequence, only CS# needs to be inactive • Add Tohz, Output valid to Z Time • Add Output Load Section • Active Power Discussion

1.0 Introduction

1.1 Objective

The objective of this document is to define a new Synchronous DRAM specification (“PC SDRAM”) which will remove extra functionality from the current JEDEC standard SDRAM specification, so that it will be a “fully compatible” device among all vendor designed parts. It should be easy to design and manufacture and highly cost optimized for the main stream volume desktop Intel architecture PCs.

1.2 Scope of This Document

The scope of this document is limited to identify and define all the essential functionality that is needed to be implemented for the first generation “PC SDRAM”. Implementation details are left to the designers of the device.

1.3 Convention Used

The following lists some of the nomenclature conventions used in this document:

- The “#” sign at the end of a signal name indicates active low signals (e.g., CS#, RAS#, etc).
- “B0” or “B1” at the end of a command name indicates the bank (e.g., READB0 indicates the READ Command for Bank 0; READB1 indicates the READ Command for Bank 0).
- “(A)” indicates the start address for the associated command (e.g., READB0(A)).
- “WRITEA” indicates a Write at an address starting at location (A); Either Bank
- “DQ(A1)” indicates the 1st data item for the access starting at location (A).

2.0 Pinout and Signal Description

2.1 Device Pinouts

The pinout for different SDRAM configurations are shown in this section.

Figure 1. Pin Assignment for 16M Devices (2Mx8, 4Mx4)

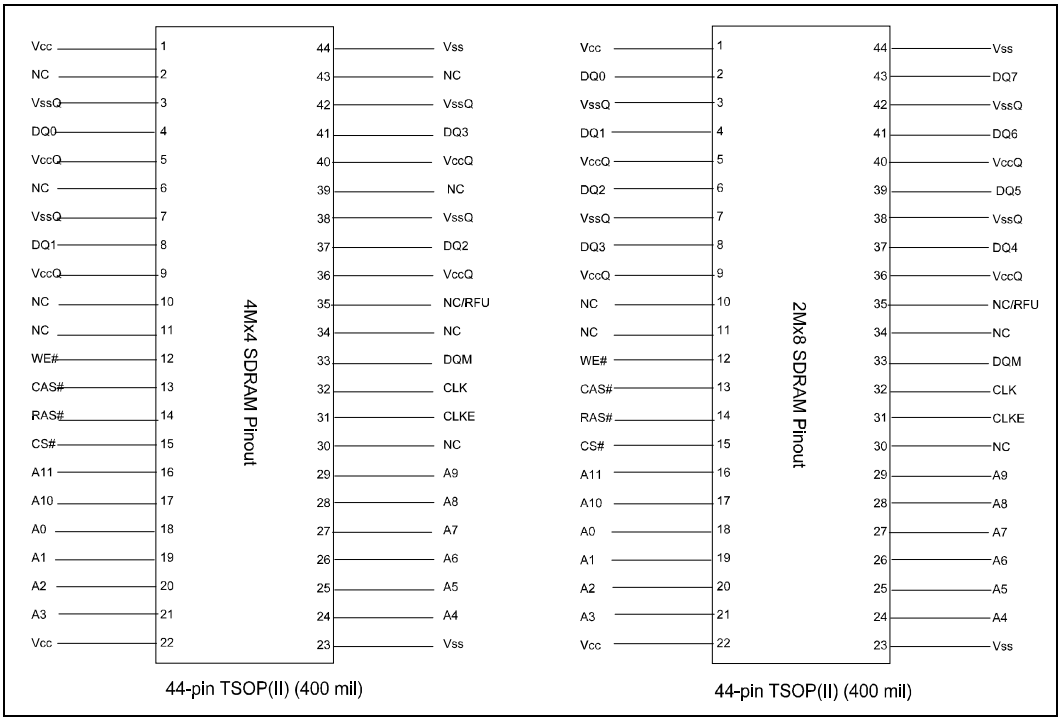


Figure 2. Pin Assignment for 16M Device (1Mx16)

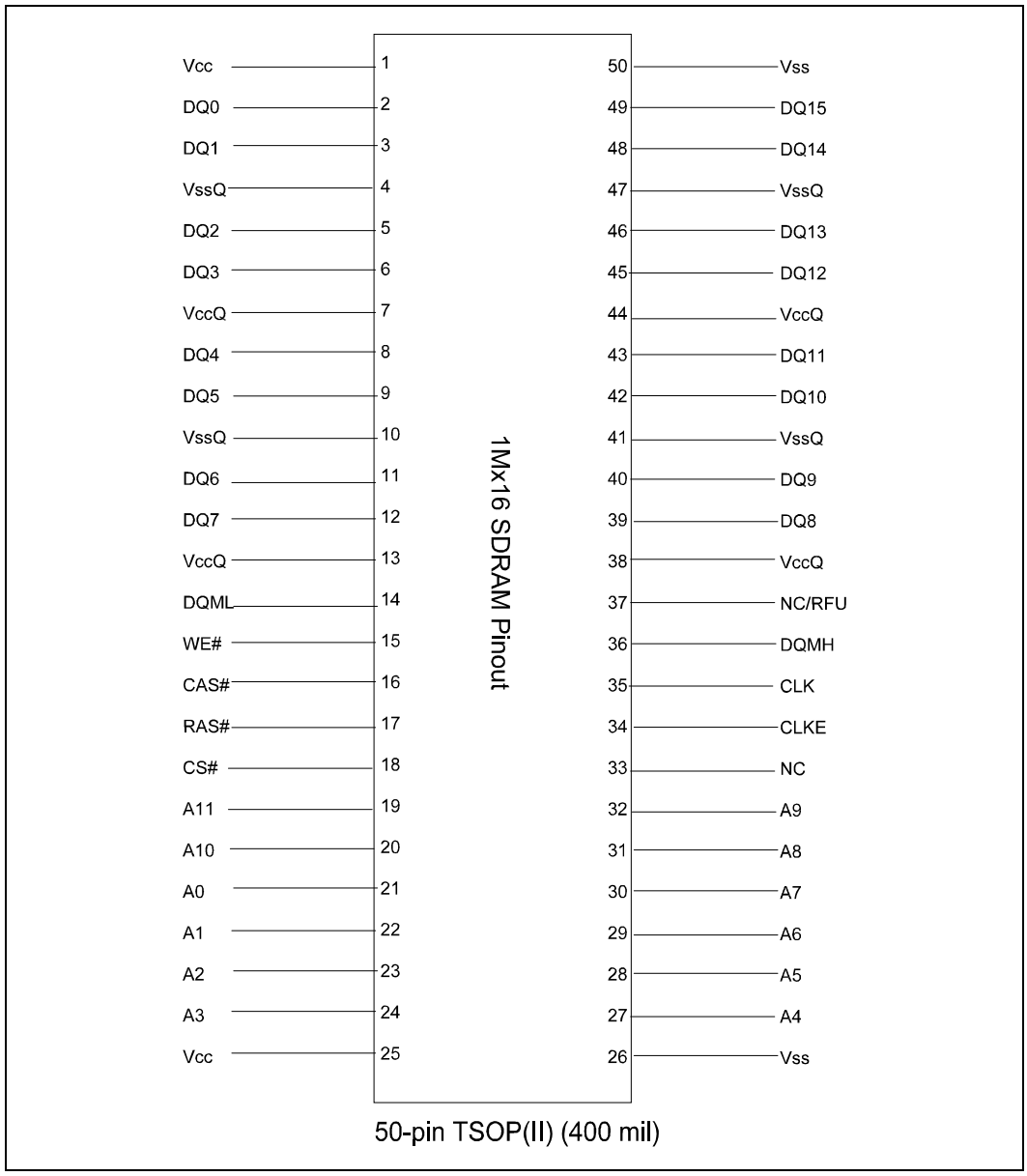
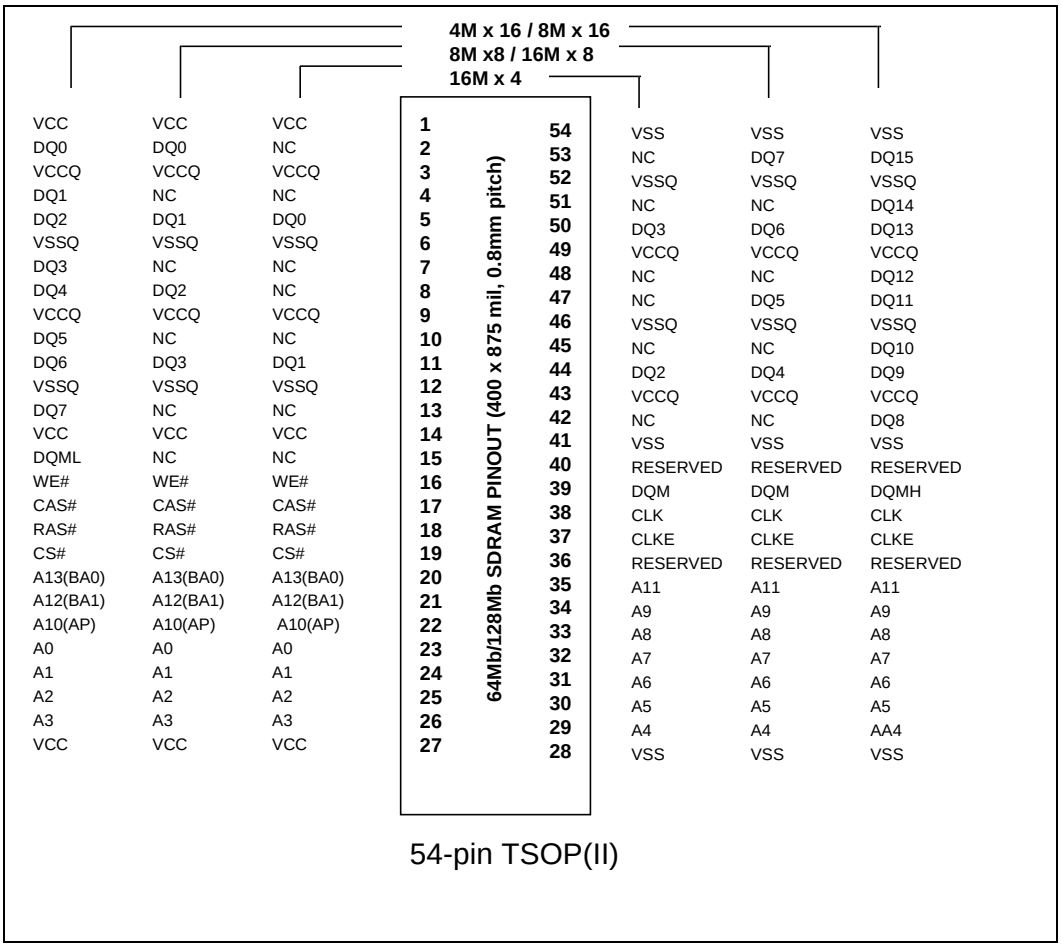
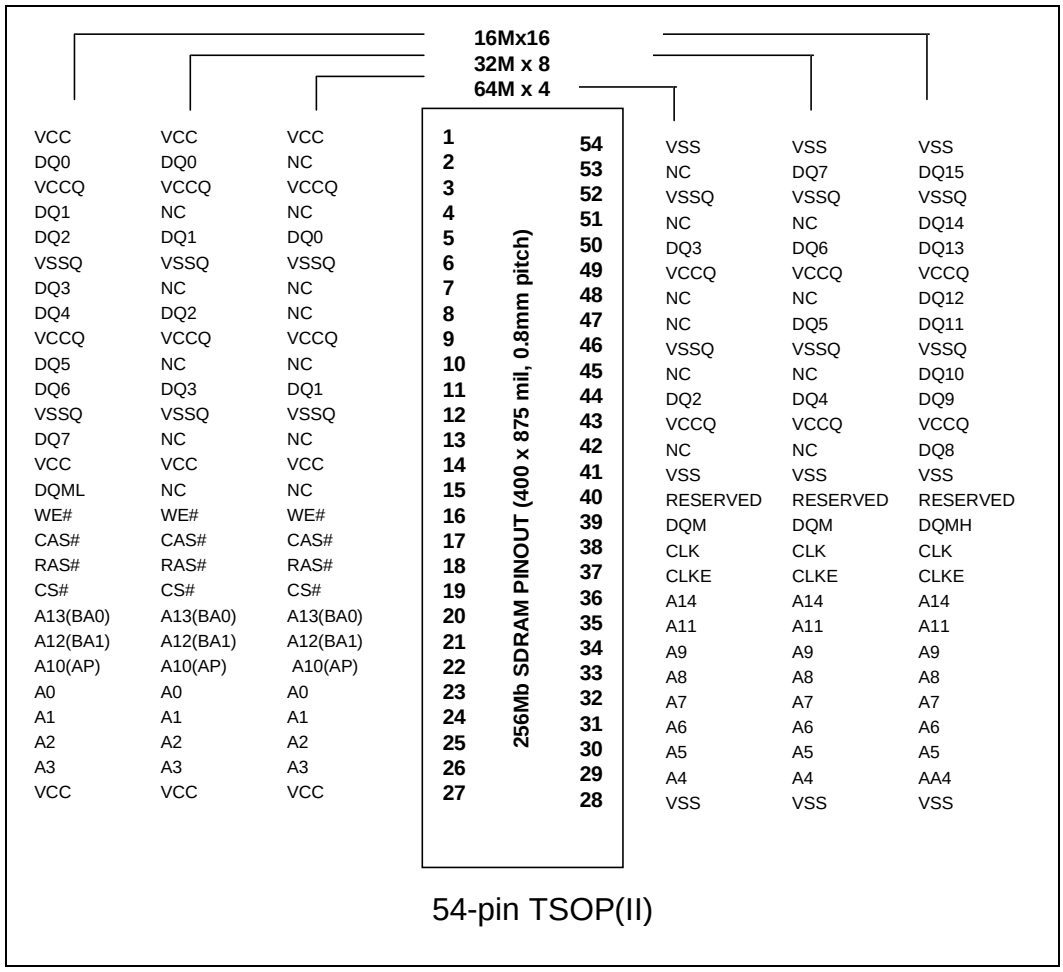


Figure 3. Pin Assignment for 64M/128M Devices (16Mx4, 8Mx8, 4Mx16, 16Mx8, and 8Mx16)



54-pin TSOP(II)

Figure 4. Pin Assignment for 256M Devices (16Mx16, 32Mx8, and 64Mx4)



2.2 Signal Descriptions (Simplified)

Table 1. Pin Functional Description (16M bit devices)

Symbol	Type	Description[1]
A[n:0]	Input - Synchronous	Some address pin definitions change as a function of array size and # of banks used.
CLK	Input - Clock	Master Clock input.
CKE	Input - Clock Enable	Activates the CLK signal when high and deactivates when low. By deactivating the clock, CLKE low intitates the Power Down mode, Self Refresh mode or Suspend Mode.
RAS#	Input - Synchronous	Row address strobe.
CS#	Input - Synchronous	Selects chip when active.
CAS#	Input - Synchronous	Column address strobe.
WE#	Input - Synchronous	Write Enable strobe.
DQM#,DQML/H#	Input - Synchronous	DQ Mask. Active high. Controls the data output buffers in read mode. In write mode it masks the data from being written to the memory array.
DQ(x:0)	Input/Output - Synchronous	Data IO pins.
NC/RFU	No connect/ Reserved for Future Use	This pin should be left No Connect on the device so that the normal functionality of the device is not be affected by the external connection to this pin. This pin could be used in future.
Vcc, Vss	Power pins	Supply Pins for the core
VccQ, VssQ	Power pins	Supply Pins for the output buffers

NOTES:
1. See the Truth Table and functional description for detailed information about the functionality.

3.0 Basic Functional Description

3.1 Mode Register and the Modes Required to be supported

Mode Register Set: (Programming mode)

11	10	9	8	7	6 ... 4	3	2 ... 0
0	0	0	0	0	LTMODE	WT	BL

Table 2. Latency Mode (LT Field)

Bits (654)	CAS# Latency
010	2
011	3
All Other	reserved

Table 3. Wrap Type (WT Field)

Bit 3	Type
0	Linear
1	Interleave

Table 4. Burst Length (BL Field)

Bits (210)	Burst Length
000	1
001	2
010	4
All Other	reserved

Table 5. Burst Address Ordering for Burst Length (BL=1,2,4)

Burst Length	Starting Bit	Interleave	Linear
2	0	0,1	0,1
2	1	1,0	1,0
4	00	0,1,2,3	0,1,2,3
4	01	1,0,3,2	1,2,3,0
4	10	2,3,0,1	2,3,0,1
4	11	3,2,1,0	3,0,1,2

3.2 Command Truth Table

Table 6. Command Truth Table

Function	Symbol	CKE n-1	CKE n	CS#	RAS#	CAS#	WE#	A11	A10	BA(0:1)	A9-A0
Device deselect	DSEL	H	X	H	X	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X	X
Read	READ	H	X	L	H	L	H	V	L	V	V
Read w/ auto precharge	READAP	H	X	L	H	L	H	V	H	V	V
Write	WRIT	H	X	L	H	L	L	V	L	V	V
Write w/ auto precharge	WRITEAP	H	X	L	H	L	L	V	H	V	V
Bank Activate	ACT	H	X	L	L	H	H	V	V	V	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X	X
Auto refresh	CBR	H	H	L	L	L	H	X	X	X	X
Self refresh entry from IDLE	SLFRSH	H	L	L	L	L	H	X	X	X	X
Self refresh exit	SLFRSHX	L	H	H	X	X	X	X	X	X	X
Power Down entry from IDLE	PWRDN	H	L	X	X	X	X	X	X	X	X
Power Down exit	PWRDNX	L	H	H	X	X	X	X	X	X	X
Mode register set	MRS	H	X	L	L	L	L	L	L	V	V

NOTES:
1. H: High Level, L: Low Level, X: don't care, V: Valid data input

Table 7. DQM# Truth Table

Function	CKE n-1	CKE n	DQM# U	DQM# L
Data write/output enable	H	X	L	L
Data mask/output disable	H	X	H	H
Upper byte write enable/lower byte mask	H	X	L	H
Lower byte write enable/high byte mask	H	X	H	L

NOTES:
1. H: High Level, L: Low Level, X: don't care

Table 8. Operative Command Table (Sheet 1 of 4)

Current state	CS#	RAS#	CAS#	WE#	Address	Command	Action	Notes
Idle	H	X	X	X	X	DSEL	Nop or Power Down	3
	L	H	H	H	X	NOP	Nop or Power Down	3
	L	H	L	H	BA,CA,A10	READ/READAP	ILLEGAL	4
	L	H	L	L	BA,CA,A10	WRIT/WRITEAP	ILLEGAL	4
	L	L	H	H	BA,RA	ACT	Row Active	
	L	L	H	L	BA,A10	PRE/PALL	NOP	
	L	L	L	H	X	CBR/SELF	Refresh or Self refresh	5
	L	L	L	L	Op-code	MRS	Mode Register access	
Row active	H	X	X	X	X	DSEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	L	H	BA,CA,A10	READ/READAP	Begin read: Optional AP	6
	L	H	L	L	BA,CA,A10	WRIT/WRITEAP	Begin write: Optional AP	6
	L	L	H	H	BA,RA	ACT	ILLEGAL	4
	L	L	H	L	BA,A10	PRE/PALL	Precharge	7
	L	L	L	H	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	OP-code	MRS	ILLEGAL	14
READ	H	X	X	X	X	DSEL	Continue burst to end -> Row active	
	L	H	H	H	X	NOP	Continue burst to end -> Row active	
	L	H	L	H	BA,CA,A10	READ/READAP	Term burst, new read:Optional AP	8
	L	H	L	L	BA,CA,A10	WRIT/WRITEAP	Term burst,start write:Optional AP	8,9
	L	L	H	H	BA,RA	ACT	ILLEGAL	4

Table 8. Operative Command Table (Sheet 2 of 4)

Current state	CS#	RAS#	CAS#	WE#	Address	Command	Action	Notes
	L	L	H	L	BA,A10	PRE/PALL	Term burst,precharge	
	L	L	L	H	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	Opcode	MRS	ILLEGAL	14
WRITE	H	X	X	X	X	DSEL	Continue burst to end ->Write recovering	
	L	H	H	H	X	NOP	Continue burst to end -> Write recovering	
	L	H	L	H	BA,CA,A10	READ/READAP	Term burst, start read: optional AP	8,9
	L	H	L	L	BA,CA,A10	WRIT/WRITEAP	Term burst, new write: optional AP	8
	L	L	H	H	BA,RA	ACT	ILLEGAL	4
	L	L	H	L	BA,A10	PRE/PALL	Term burst precharging	10
	L	L	L	H	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	Op Code	MRS	ILLEGAL	14
Read with auto precharge	H	X	X	X	X	DSEL	Continue burst to end -> precharging	
	L	H	H	H	X	NOP	Continue burst to end -> precharging	
	L	H	L	H	BA,CA,A10	READ/READAP	ILLEGAL	13
	L	H	L	L	BA,CA,A10	WRIT/WRITEAP	ILLEGAL	13
	L	L	H	H	BA,RA	ACT	ILLEGAL	4,13
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	4,13
	L	L	L	H	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	Opcode	MRS	ILLEGAL	14
Write with auto precharge	H	X	X	X	X	DSEL	Continue burst to end ->Write recovering with auto precharge	
	L	H	H	H	X	NOP	Continue bust to end-> Write recovering with auto precharge	
	L	H	L	H	BA,CA,A10	READ/READAP	ILLEGAL	13
	L	H	L	L	BA,CA,A10	WRIT/WRITEAP	ILLEGAL	13
	L	L	H	H	BA,RA	ACT	ILLEGAL	4,13
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	4,13
	L	L	L	H	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	Opcode	MRS	ILLEGAL	14

Table 8. Operative Command Table (Sheet 3 of 4)

Current state	CS#	RAS#	CAS#	WE#	Address	Command	Action	Notes
Precharging	H	X	X	X	X	DSEL	NOP- Enter Idle after Trp	
	L	H	H	H	X	NOP	NOP-Enter Idle after Trp	
	L	H	L	H	BA,CA,A10	READ/READAP	ILLEGAL	4,13
	L	H	L	L	BA,CA,A10	WRIT/WRITEAP	ILLEGAL	4,13
	L	L	H	H	BA,RA	ACT	ILLEGAL	4,13
	L	L	H	L	BA,A10	PRE/PALL	NOP- Enter Idle after Trp	
	L	L	L	H	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	Op Code	MRS	ILLEGAL	14
Row activating	H	X	X	X	X	DSEL	NOP- Enter row active after Trcd	
	L	H	H	H	X	NOP	NOP- Enter row active after Trcd	
	L	H	L	H	BA,CA,A10	READ/ READAP	ILLEGAL	4,13
	L	H	L	L	BA,CA,A10	WRIT/ WRITEAP	ILLEGAL	4,13
	L	L	H	H	BA,RA	ACT	ILLEGAL	4,11,13
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	4,13
	L	L	L	H	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	Opcode	MRS	ILLEGAL	14
Write Recovering	H	X	X	X	X	DSEL	NOP - Enter row active after Tdpl	
	L	H	H	H	X	NOP	NOP - Enter row active after Tdpl	
	L	H	L	H	BA,CA,A10	READ/ READAP	Start Read, optional AP	9
	L	H	L	L	BA,CA,A10	WRIT/ WRITEAP	New Write, optional AP	
	L	L	H	H	BA,RA	ACT	ILLEGAL	4,13
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	4,14
	L	L	L	H	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	Opcode	MRS	ILLEGAL	14
Write recovering with auto precharge	H	X	X	X	X	DSEL	NOP - Enter precharge after Tdpl	
	L	H	H	H	X	NOP	NOP - Enter precharge after Tdpl	
	L	H	L	H	BA,CA,A10	READ/ READAP	ILLEGAL	4,9,13

Table 8. Operative Command Table (Sheet 4 of 4)

Current state	CS#	RAS#	CAS#	WE#	Address	Command	Action	Notes
	L	H	L	L	BA,CA,A10	WRIT/ WRITEAP	ILLEGAL	4,13
	L	L	H	H	BA,RA	ACT	ILLEGAL	4,13
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	4,14
	L	L	L	H	X	CBR/SELF	ILLEGAL	14
	L	L	L	L	Op Code	MRS	ILLEGAL	14
Refreshing	H	X	X	X	X	DSEL	NOP - Enter idle after trc	
	L	H	H	H	X	NOP	NOP- Enter idle after trc	
	L	H	L	X	X	READ/ READAP	ILLEGAL	14
	L	L	H	X	X	ACT/PRE/PALL	ILLEGAL	14
	L	L	L	X	X	CBR/SELF/MRS	ILLEGAL	14
Mode Register accessing	H	X	X	X	X	DSEL	NOP - Enter idle after tmrd	
	L	H	H	H	X	NOP	NOP - Enter idle after tmrd	
	L	H	L	X	X	READ/ WRITE/ READAP/ WRITEAP	ILLEGAL	14
	L	L	X	X	X	ACT/PRE/PALL/ CBR/SELF/MRS	ILLEGAL	14

NOTES:
1. H: High Level, L: Low Level, X: don't care, V: Valid data input, BA: Bank Address, AP: (Auto Precharge), CA: (Column Address), RA: (Row Address)
2. All entries assume that CKE was active (high level) during the preceding clock cycle.
3. If both banks are idle and CKE is inactive (low level), then in power down mode.
4. Illegal to bank in specified states. Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
5. If both banks are idle and CKE is inactive (low level), then Self refresh mode.
6. Illegal if trcd is not satisfied.
7. Illegal if tras is not satisfied.
8. Must satisfy burst interupt condition.
9. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
10. Must mask preceding data which don't satisfy tdpl.
11. Illegal if trrd is not satisfied.
12. Burst Stop command is disabled.
13. Ilegal for single bank, but legal for other banks in multi-bank devices.
14. Illegal for all banks.

Table 9. Row/Column Addresssing Per Memory Size/# Banks

Memory Size	# Banks	# Bank Addresses	# Row Addresses	# Column Addresses
16M 2 bank				
1Mx16	2	1	11	8
2Mx8	2	1	11	9
4Mx4	2	1	11	10
64M 4 bank				
2Mx32	4	2	11	8
4Mx16	4	2	12	8
8Mx8	4	2	12	9
16Mx4	4	2	12	10
128M 4 bank				
4Mx32	4	2	12	8
8Mx16	4	2	12	9
16Mx8	4	2	12	10
32Mx4	4	2	12	11
256M 4 bank				
8Mx32	4	2	13	8
16Mx16	4	2	13	9
32Mx8	4	2	13	10
64Mx4	4	2	13	11

3.3 Address Bit Maps

3.3.1 16M Address Bit Maps For Row And Column Addresses During Commands

Table 10. Row Address Table (ACT, PRE)

Address Bit	Value	Command Type	Function	Memory Organization
A11	0	Row Activate (ACT), PRE,	Bank0 Activate/ Precharge	1Mx16, 2Mx8, 4Mx4
A11	1	Row Activate (ACT), PRE	Bank1 Activate/ Precharge	1Mx16, 2Mx8, 4Mx4
A10	0,1	Row Activate (ACT)	Row address	1Mx16, 2Mx8, 4Mx4
A10	0	Precharge Single Bank (PRE)	Precharge Selected Bank	1Mx16, 2Mx8, 4Mx4
A10	1	Precharge All Banks (PALL)	Precharge All Banks	1Mx16, 2Mx8, 4Mx4
A9-A0	V	Row Activate (ACT)	Row Address	1Mx16, 2Mx8, 4Mx4

Table 11. Column Address Table (Read/Write/Read AP/Write AP)

Address Bit	Value	Command Type	Function	Memory Organization
A11	0	Read(READ), Write(WRITE)	Bank0 Read/Write	1Mx16, 2Mx8, 4Mx4
A11	1	Read(READ), Write(WRITE)	Bank1 Read/Write	1Mx16, 2Mx8, 4Mx4
A10	0	Read(READ), Write(WRITE)	Disable Auto Precharge during Command	1Mx16, 2Mx8, 4Mx4
A10	1	Read(READ), Write(WRITE)	Enable Auto Precharge during Command	1Mx16, 2Mx8, 4Mx4
A9	V	Read(READ), Write(WRITE)	Column Address	4Mx4
A9	X	Read(READ), Write(WRITE)	None	1Mx16, 2Mx8
A8	V	Read(READ), Write(WRITE)	Column Address	4Mx4, 2Mx8
A8	X	Read(READ), Write(WRITE)	None	1Mx16
A0-A7	V	Read(READ), Write(WRITE)	Column Address	1Mx16, 2Mx8, 4Mx4

3.3.2 64M Address Bit Maps for Row and Column Addresses During Commands

Table 12. Row Address Table (ACT, PRE) (per JEDEC Standard)

Address Bit	Value	Command Type	Function	Memory Organization
BA0	0,1	Bank Select	Bank0/1 (2 bank device)	x4,x8,x16,x32
BA1	0,1	Bank Select	Bank2/3 (4 bank device)	x4,x8,x16,x32
A12	V	Row Activate (ACT)	Row Address (2 bank only)	x4,x8,x16
A11	V	Row Activate (ACT)	Row Address	x32 (2 bank only)
A11	V	Row Activate (ACT)	Row Address	x4,x8,x16
A10	V	Row Activate (ACT)	Row Address	x4,x8,x16,x32
A10	0	Precharge Single Bank (PRE)	PREcharge Selected Bank	x4,x8,x16,x32
A10	1	Precharge All Banks (PALL)	PREcharge All Banks	x4,x8,x16,x32
A9-A0	V	Row Activate (ACT)	Row Address	x4,x8,x16,x32

Table 13. Column Address Table (Read/Write/Read AP/Write AP)

Address Bit	Value	Command Type	Function	Memory Organization
BA0	0,1	Bank Select	Bank0/1 (2 bank device)	x4,x8,x16,x32
BA1	0,1	Bank Select	Bank2/3 (4 bank device)	x4,x8,x16,x32
A10	0	Read(READ), Write(WRITE)	Disable Auto Precharge during Command	x4,x8.x16,x32
A10	1	Read(READ), Write(WRITE)	Enable Auto Precharge during Command	x4,x8,x16,x32
A9	V	Read(READ), Write(WRITE)	Column Address	x4
A9	X	Read(READ), Write(WRITE)	None	x8,x16,x32
A8	V	Read(READ), Write(WRITE)	Column Address	x4,x8,x32
A8	X	Read(READ), Write(WRITE)	None	x16
A0-A7	V	Read(READ), Write(WRITE)	Column Address	x4,x8,x16,x32

3.4 Power-Up and Initialization Sequence

3.4.1 Power Up Sequence

The SDRAM should be initialized by the following sequence of operations:

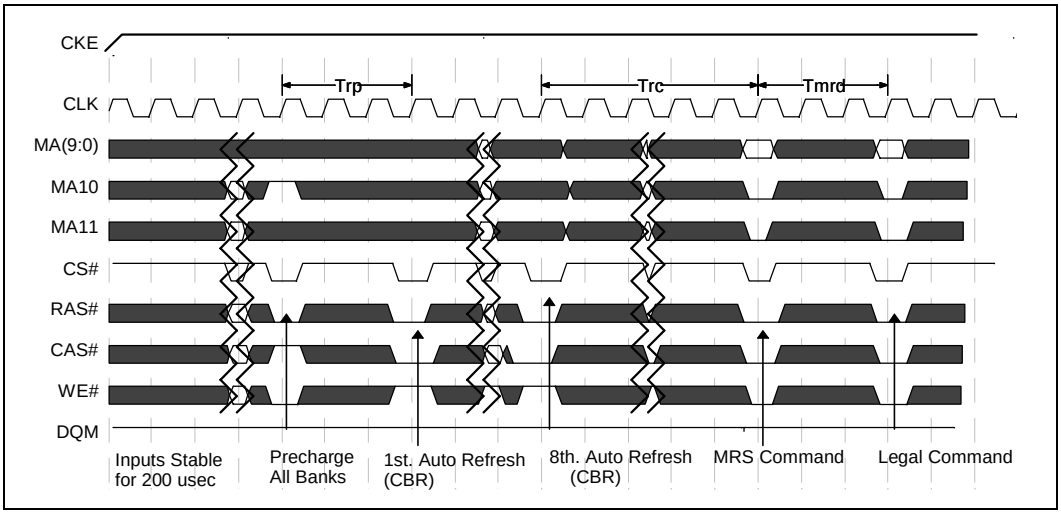
1. Clock will be applied at power up along with power (clock frequency will be unknown).
2. The clock will stabilize within 100usec before the first command to SDRAM is attempted.
3. All the control inputs, RAS#, CAS#, WE#, CS# will be held in an undefined state (either valid high or low) during reset. After reset is complete CS# will be held inactive before the first access to SDRAM is attempted. All other address and control signals will be driven to a valid state.
4. The levels on all the address inputs should be ignored. (All the address inputs can be indeterminate.)

3.4.2 Initialization Sequence

The initialization sequence can be issued at *anytime*. Following the initialization sequence, the device must be ready for full functionality. SDRAM devices are initialized by the following sequence:

1. At least one NOP cycle will be issued after the 1msec device deselect.
2. A minimum pause of 200usec will be provided after the NOP.
3. A precharge all (PALL) will be issued to the SDRAM.
4. 8 Auto refresh (CBR) refresh cycles will be provided.
5. A mode register set (MRS) cycle will be issued to program the SDRAM parameters (e.g., Burst length, CAS# latency etc.).
6. After MRS the device should be ready for full functionality within 3 clocks after T_{mrd} is met.

Figure 5. Power Up Initialization Sequence



3.5 Precharge Selected Bank

The precharge operation should be performed on the active bank when precharge selected bank command is issued. When the precharge command is issued with address A10 low, A11 selects the bank to be precharged. At the end of the precharge selected bank command the selected bank should be in idle state after the minimum t_{RP} is met.

3.6 Precharge All

All the banks should be precharged at the same time when this command is issued. When the precharge command is issued with address A_{10} high then all the banks will be precharged. At the end of the precharge all command all the banks should be in idle state after the minimum t_{RP} is met.

A10	A11	16M 2 Bank Precharge (type)
Low	Low	Precharge bank 0
Low	High	Precharge bank 1
High	X	Precharge All banks

A10	A12	A13	64M 4 Bank Precharge (type)
Low	Low	Low	Precharge Bank 0
Low	High	Low	Precharge Bank 1
Low	Low	High	Precharge Bank 2
Low	High	High	Precharge Bank 3
High	X	X	Precharge All Banks

3.7 NOP and Device Deselect

The device should be deselected by deactivating the CS# signal. In this mode SDRAM should ignore all the control inputs. The SDRAMs are put in NOP mode when CS# is active and by deactivating RAS#, CAS# and WE#. For both Deselect and NOP the device should finish the current operation when this command is issued.

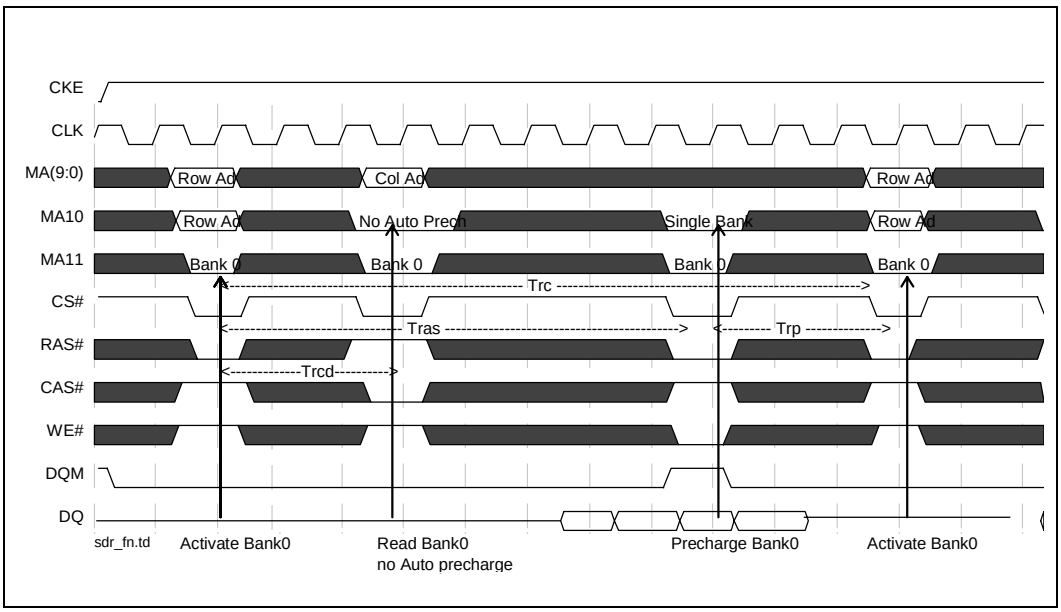
3.8 Row activate

This command selects a row in a specified bank of the device. Read and write operations can only be initiated on this activated bank after the minimum t_{RCD} time is elapsed from the activate command.

3.9 Read Bank

This command is used after the row activate command to initiate the burst read of data. The read command is initiated by activating CS#, CAS# and deasserting WE# at the same clock sampling (rising) edge as described in the command truth table. The length of the burst and the CAS# latency time will be determined by the values programmed during the MRS command.

Figure 6. Row Activate, Read and Precharge



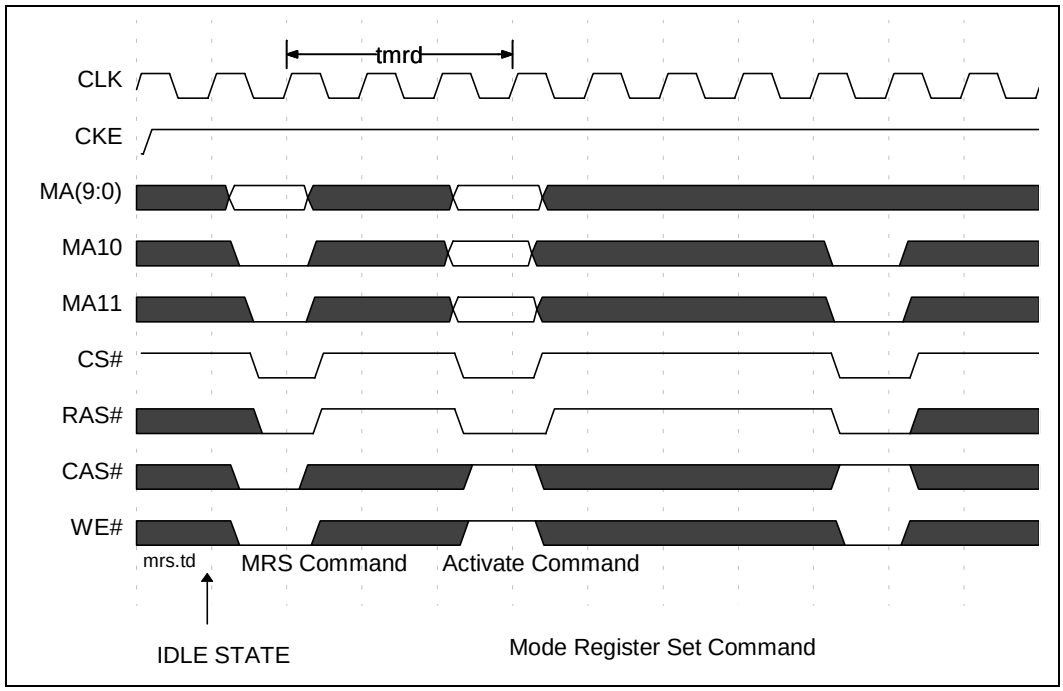
3.10 Write Bank

This command is used after the row activate command to initiate the burst write of data. The write command is initiated by activating CS#, CAS# and WE# at the same clock sampling (rising) edge as described in the command truth table. The length of the burst will be determined by the values programmed during the MRS command.

3.11 Mode Register Set Command

This command programs the SDRAM for the desired operating mode. This command should be used after power up as defined in the power up sequence before the actual operation of the SDRAM is initiated. The functionality of the SDRAM device can be altered by re-programming the mode register through the execution of Mode Register Set command. All the banks should be precharged (i.e., in idle state) before the MRS command can be issued.

Figure 7. Mode Register Set Command



4.0 Essential Functionality for the “PC SDRAM” Device

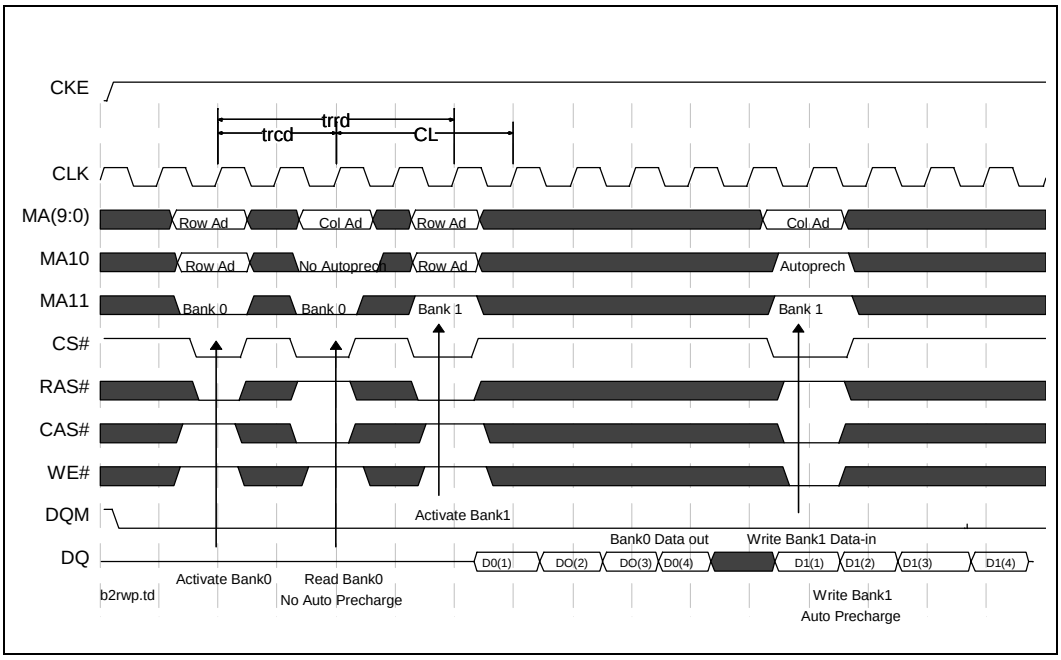
The essential functionality that is required for the “PC SDRAM” device is described below:

- Burst Read
- Burst Write
- Multi bank ping pong access
- Burst Read with Autoprecharge
- Burst Write with Autoprecharge
- Burst Read terminated with precharge
- Burst Write terminated with precharge
- Burst Read terminated with another Burst Read/Write
- Burst Write terminated with another Burst Write/Read
- DQM# masking
- Fastest command to command delay of 1 clock
- Precharge All command
- Auto Refresh
- CL=2,3
- Burst Length 1,2 and 4
- Self Refresh Command
- Power Down
- Multibank Operation

4.1 Burst Read and Burst Write

Burst read and write commands are initiated as shown in the diagram below. The bank first needs to be activated (if not already activated) through the activate bank command and then the read or write command should be initiated. Read and write is distinguished by the WE# signal state as shown. Trcd (RAS# to CAS# delay) must be met to initiate a command after the activate command.

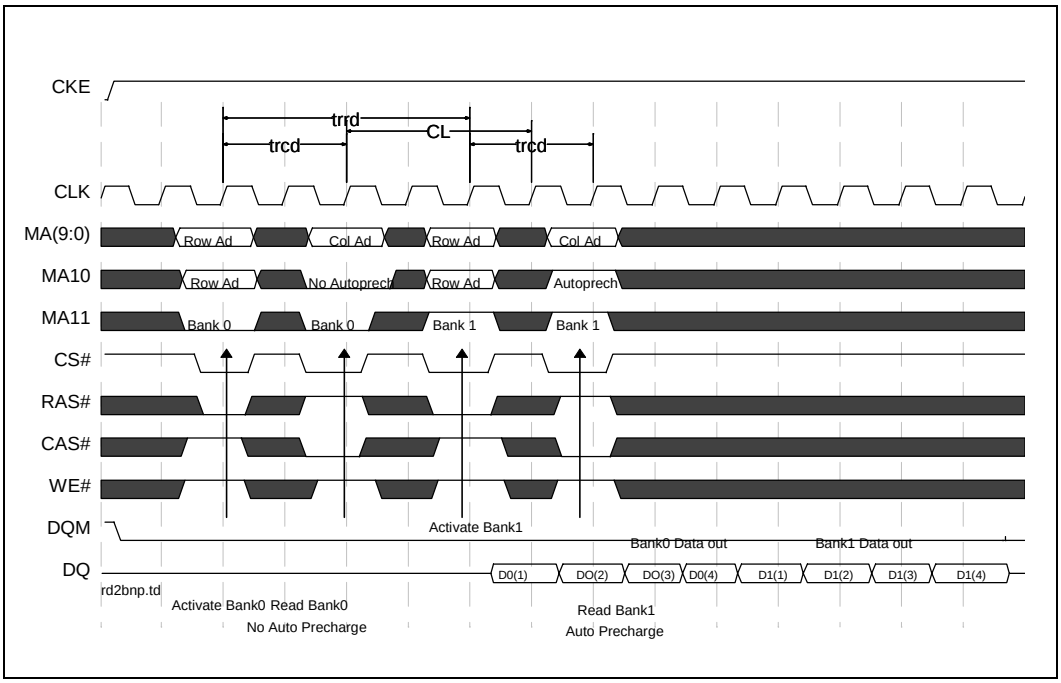
Figure 8. Read and Write Commands (Burst Length 4 Shown)



4.2 Multibank Ping Pong Access

Two bank ping pong access is described in the following diagram. Another bank can be activated while the first bank is being accessed as shown. RAS# to RAS# delay Trrd must be met while activating another bank.

Figure 9. Two Bank Ping Pong Read



4.3 Read and Write With Autoprecharge

Burst reads and writes with auto precharge commands are initiated *with autoprecharge if A10 is to high* while the read or write commands are issued as shown in the previous Figure 8 and Figure 9.

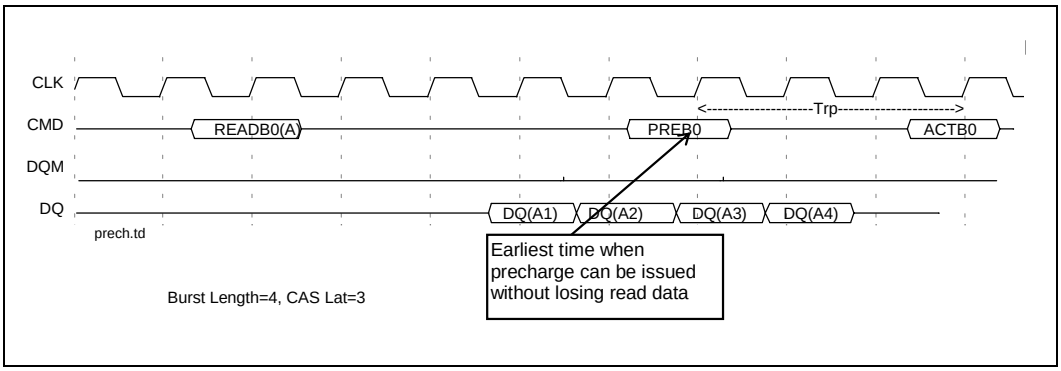
4.4 Precharge Termination of Burst

Burst reads and writes without autoprecharge can be terminated prematurely by precharge command. (If the burst read or write command was issued in auto precharge mode then the commands may not be terminated prematurely for that bank). See Multibank Figure 48 for illustration.

4.4.1 Precharge Command After a Burst Read

The earliest a precharge command can be issued after a Read command without the loss of data is CL + BL - 2 clocks. The precharge command can be issued as soon as the tras time is met. The earliest time that precharge can be issued is shown for the CAS# Latency = 3 devices.

Figure 10. Precharge Command After Burst Read

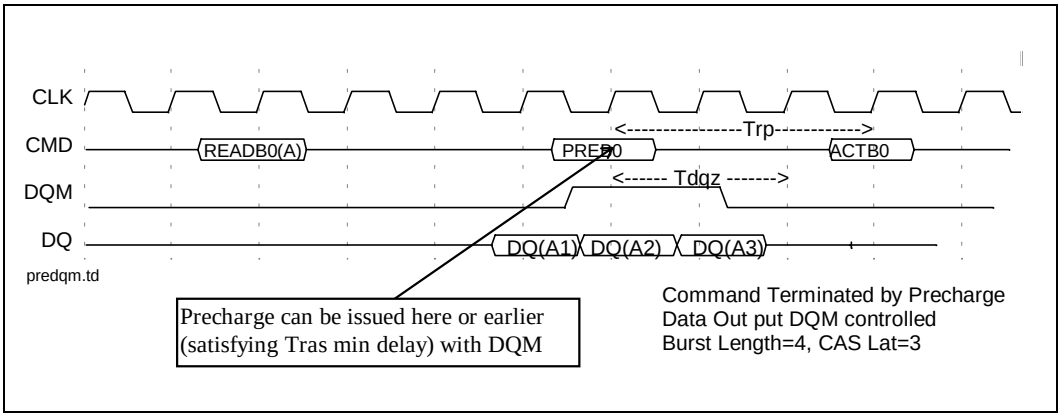


4.4.2 Precharge Termination of a Burst Read

Burst Read (with no autoprecharge) can be terminated earlier using a precharge command along with the DQM# as shown in Figure 11 (min tras must be met). This terminates reads when the remaining data elements are not needed. It allows starting the precharge early. The remaining data is undefined. DQM# should be used to mask.

Figure 11 shows the output data buffers being controlled by the DQM# signal. The data buffers get tristated after the t_{dqz} delay as shown. Without deasserting DQM#, DQ(A4) is undefined.

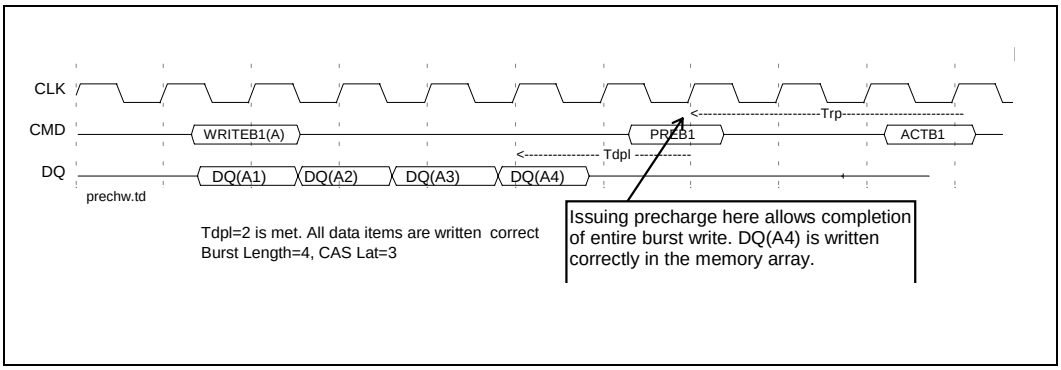
Figure 11. Read Terminated by Precharge (Outputs DQM# Controlled)



4.4.3 Precharge Command After a Burst Write

The earliest time that precharge can be issued is Tdpl clocks after the last data.

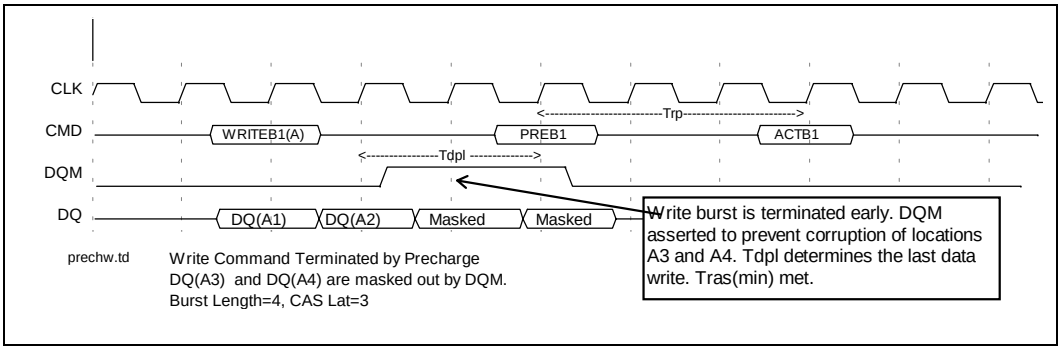
Figure 12. Precharge Command after Burst Write



4.4.4 Precharge Termination of a Burst Write

To terminate Burst Write early with precharge command the DQM# signal should be used as shown. Data sampled Tdpl clocks before precharge command will be written correctly. Data sampled afterword and before the precharge command is undefined. DQM# should be used to prevent the location from being corrupted. DQM# must be asserted active to prevent location (A3 and A4 in this case) from being corrupted. DQ(A2) will be written correctly as tdpl is met.

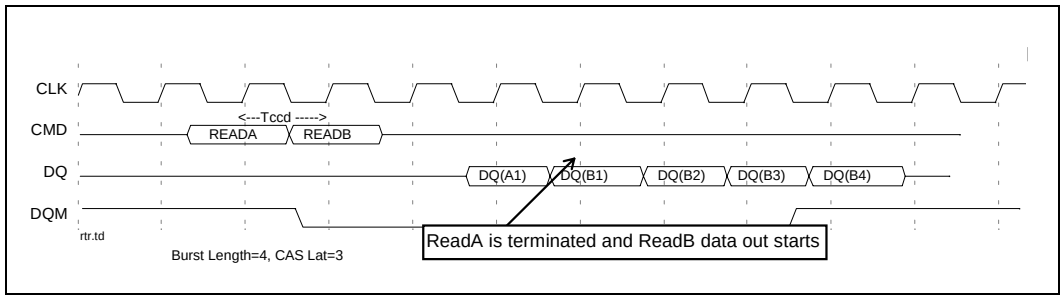
Figure 13. Precharge Command After Write



4.5 Read Terminated By Read

A Read Command should terminate the previous read command and the data should be available after CAS# Latency for the new comand. Fastest command to command delay is determined by Tccd (1 clock as shown).

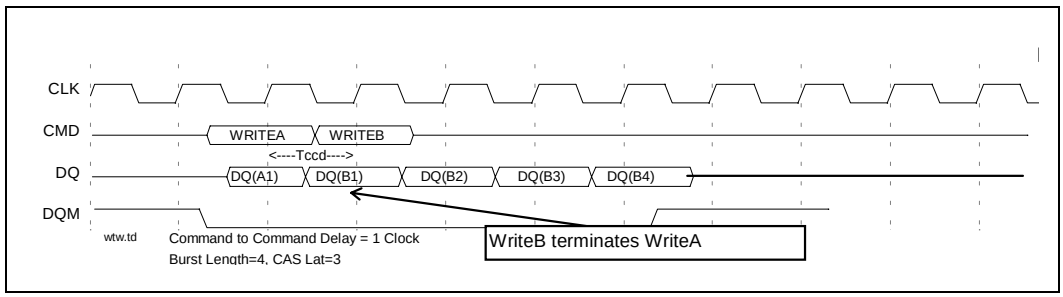
Figure 14. Read Terminated By Read



4.6 Write Terminated By Write

A Write Command should terminate the previous write command and the new burst write command should start with the new command as shown. Fastest command to commad delay is determined by Tccd (1 clock as shown).

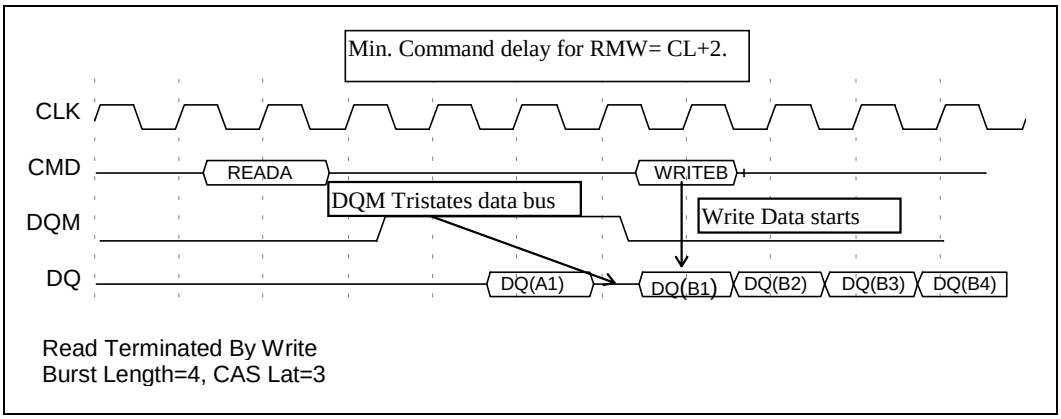
Figure 15. Write Terminated with Write



4.7 Read Terminated By Write

A Write Command should terminate the previous read command and the new burst write should start as shown in Figure 15. The minimum theoretical command delay is 1 clock. But for practical purposes the minimum command delay, for a valid operation (e.g., read-modified-write) should be = CAS# Latency + buffer turn around cycle + 1. The DQM# must be held active to keep the ouput buffer in HiZ as shown to prevent the internal IO buffer conflict between the read data (in pipe) and the write data driven on the input pins.

Figure 16. Read Terminated By Write



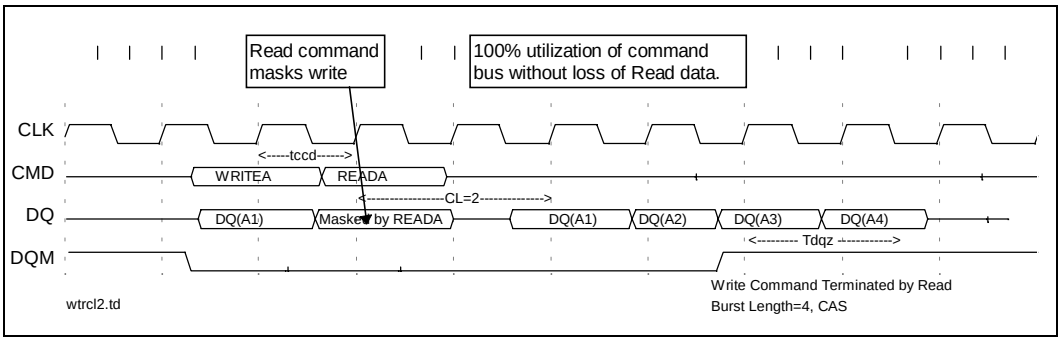
4.8 Write Terminated By Read

A Read Command should terminate the previous write command and the new burst read should start as shown. In case of with tccd=1, CL=3 and tdqz=2, there is no loss of data bandwidth even if DQM# is activated to mask the write data.

In the case of CL=2 and tdqz=2, the activation of DQM# signal causes the first read data to be lost, if read command is issued (tccd=1). To preserve the first read data the issue of READ command has to be delayed (tccd=2). This implementation reduces the command bus utilization.

For 100% command bus utilization with CL=2, the READ command should mask the write data as shown.

Figure 17. Write terminated by Read (CL=2)



4.9 SDRAM Commands, To Two Or Four Banks, In Consecutive Clocks

Given **COMMAND1** detected by SDRAM component (to bank(i)), it will handle correctly **COMMAND2** (to bank(j)) that is detected in the next clock or later.

- Note that bank(i) and bank(j) could be any banks of the component while i is different than j.
- Also, note that COMMAND1 (or COMMAND2) can be: Precharge-Bank, Internally-Scheduled_Auto-Prechrge, Activate, Read or Write. COMMAND1/2 cannot be a Precharge-All.

4.10 Next Command To Same Bank After Precharge

4.10.1 Precharge Bank

If a Precharge-Bank command (to bank(k)) is detected by SDRAM component in CLK(n), then there will be no commands presented to this bank until CLK(n+tRP).

4.10.2 Precharge All

If a Precharge-All command is detected by SDRAM component in CLK(n), then there will be no commands presented to this component until CLK(n+tRP).

4.10.3 Read-Auto_Precharge

- If a Read with Auto-Precharge command (to bank(k)) is detected by SDRAM component in CLK(n), then there will be no commands presented to this bank until CLK(n+CL+BL-2+tRP).

4.10.4 Write-Auto_Precharge

If a Write with Auto-Precharge command (to bank(k)) is detected by SDRAM component in CLK(n), then there will be no commands presented to this bank until CLK(n+BL+DAL-1).

4.11 Concurrent Precharge Commands To Multiple Rows

In various events, given the controller’s ability to maintain open banks of multiple rows, the controller would want to close all banks of all rows. In these cases, a PRE-ALL commands to multiple rows is performed in the same clock.

4.12 Back to back Command With Auto Precharge

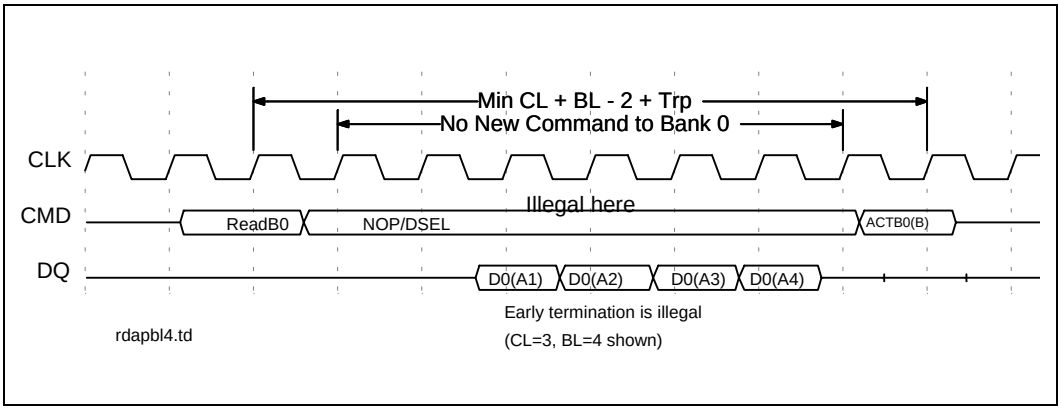
Read or write burst initiated with auto precharge (A10=high during read or write) will execute the read or write normally with the exception that after the burst operation is over the accessed bank will start to precharge. To access the bank again it has to be explicitly reactivated with activate bank command.

The commands initiated with autoprecharge could not be terminated with any other commands for that bank.

The earliest possible command (to the same bank) after autoprecharge command is shown in Figure 19 for read.

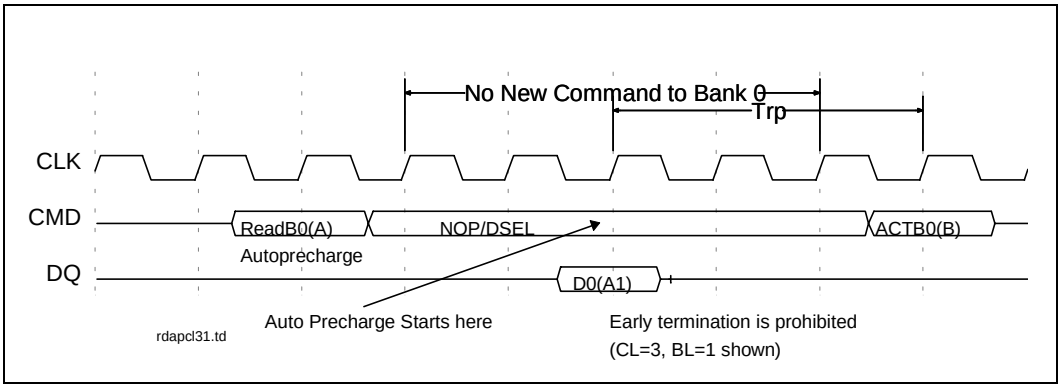
Cases for Burst Length = 4 and Burst Length = 1 are shown below.

Figure 18. Read Command with Auto Precharge (BL=4)



Note: For BL=1, minimum activation time is controlled by Trp.

Figure 19. Read Command with Auto Precharge (BL=1)



For writes with autoprecharge, the earliest possible next command (to the same bank) could be issued after BL + Tdal -1 clocks is met as shown in Figure 20 and Figure 21.

Figure 20. Write Command With Autoprecharge (BL=4)

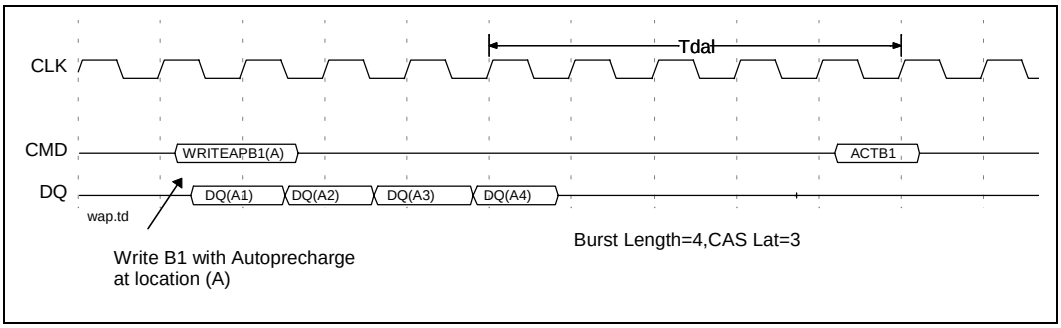
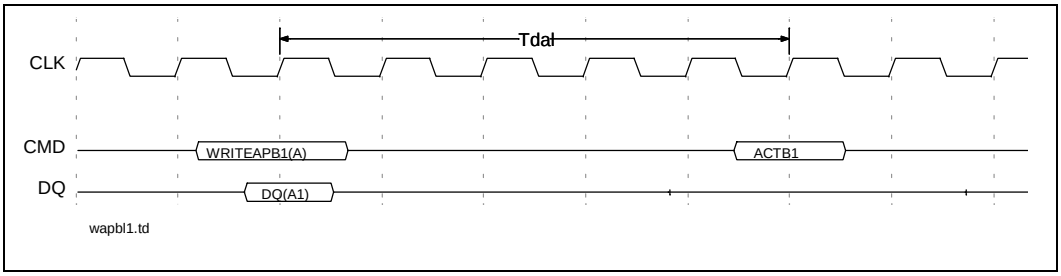


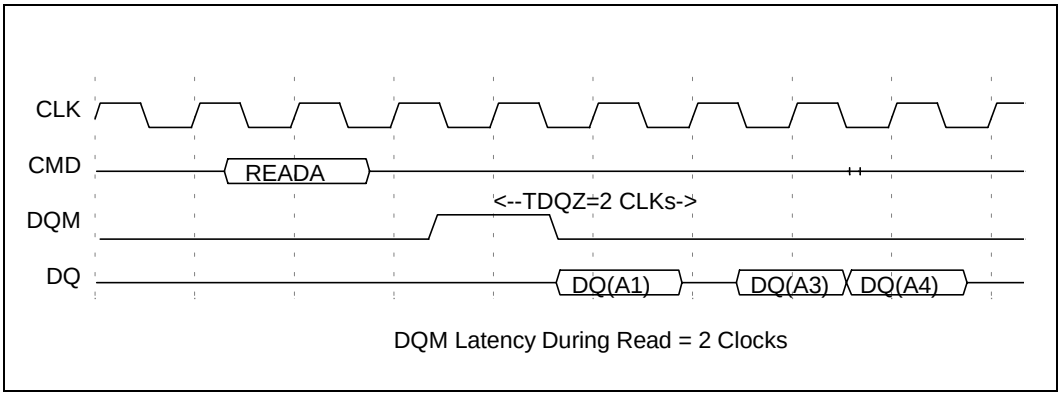
Figure 21. Write Command With Autoprecharge (Bl=1)



4.13 DQM# Latency

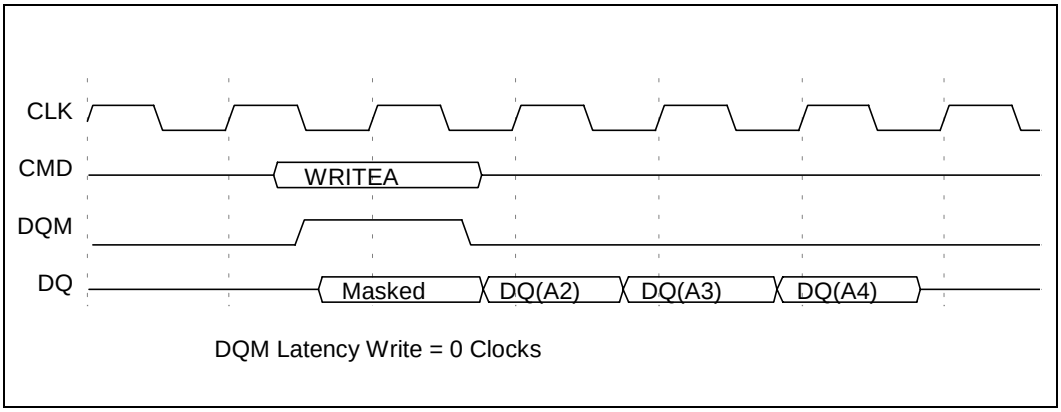
DQM# latency for read cycle, tdqz, for output disable is 2 clocks as shown in Figure 22.

Figure 22. DQM# Latency, Read Cycle



Input mask during write cycle Tdqm, should be zero as shown in Figure 23.

Figure 23. DQM# Latency, Write Cycle



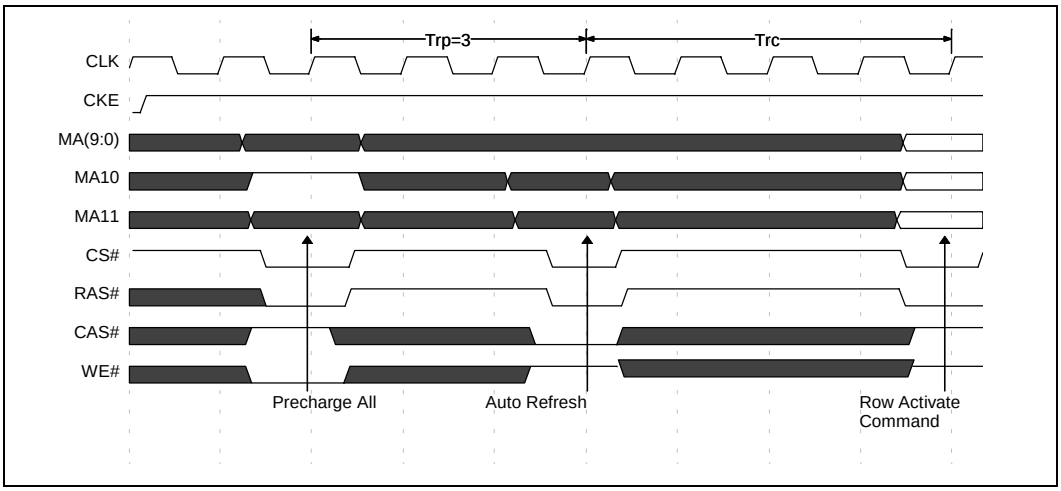
4.14 Back to Back Command Support

Minimum command to command delay of 1 Clock should be supported.

4.15 Auto Refresh (CBR) Command

An auto refresh (CBR) should be used to refresh the SDRAM array explicitly. Refresh addresses should be generated internally by the SDRAM device and incremented after each auto refresh automatically. No commands (including another auto refresh) should be issued until a minimum trc is satisfied.

Figure 24. Auto Refresh and Precharge All Command



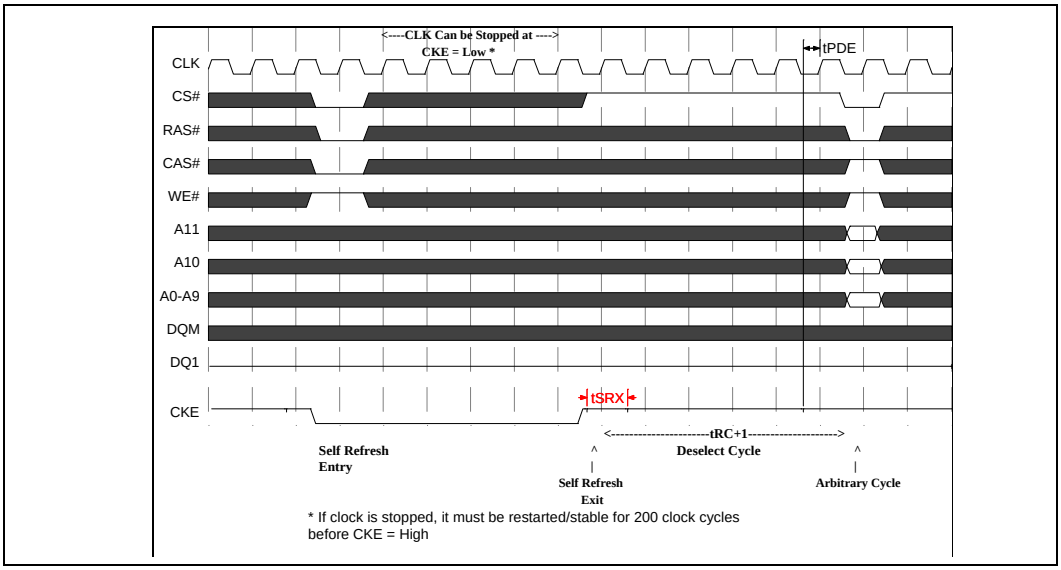
4.16 Self Refresh Entry/Exit

The self refresh mode is entered by having CS#, RAS#, and CAS# held low with WE# high at the rising edge of the clock, while CKE is low. Once SDRAM enters the Self Refresh mode, all inputs except CKE will be in a don't care state and outputs will be in tri-stated. The external clock may be halted while the device is in Self Refresh mode, however, the clock must be restarted 200 cycles before CKE is high. The self refresh command is exited by asserting CKE high. A new command may be given trc +1 clocks after CKE is high.

Self Refresh Entry and Exit is illustrated in Figure 25.

The ICC self refresh current (ICCSLFR) is specified in Table 16. This is independent of the external clock.

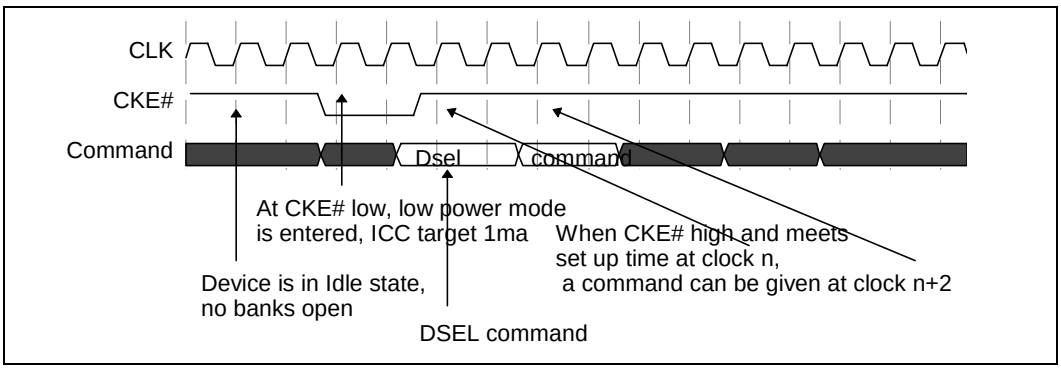
Figure 25. Self Refresh Entry and Exit



4.17 Low Power ICCLP

A low power ICCLP can be achieved by asserting CKE# low as indicated in Figure 26. The device will be in the idle state, all banks closed before CKE# is asserted low. Upon CKE# low, the device will enter this defined low power mode. The device will exit low power mode when CKE# is sampled high at clock n. A command may be given at clock n+2.

Figure 26. Low Power ICCLP



4.18 Non-Required SDRAM Functionality

Support of the following functionalities are not required in the first generation of the “PC SDRAM” devices.

- Burst Stop Command (BST)

4.19 Multibank Operation

Figure 27 to Figure 51 depict the type of multibank functional cycles for Intel chipsets. Table 14 specifies some of the timing parameters used for the multibank timing relationship diagrams. CL, trcd and trp can all have values of 2 or 3.

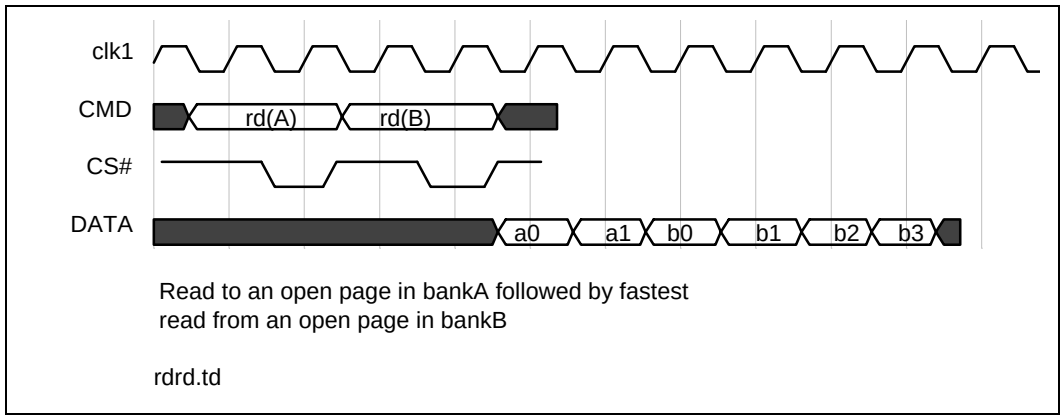
Note: The same behavior applies when these parameters change.

Table 14. Partial list of Timing Paramters for Multibank Timing Relationship Diagrams (Figure 27 to Figure 51)

CMD setup[1]	MA, RAS#, CAS# and WE# setup to CS#	1CLK
CL	CAS# latency	3 CLK
BL	Burst Length	4
trp	RAS# Pre charge	3 CLK
tras	RAS# active time	5 CLK
trcd	RAS# to CAS# delay	2 CLK

NOTES:
1. In general, 100 MHz SDRAM design can work with no setup time between MA, command and CS# signals, when system timing allow it. In the following diagrams, the ability to handle a new command and address - every clock, is not presented.

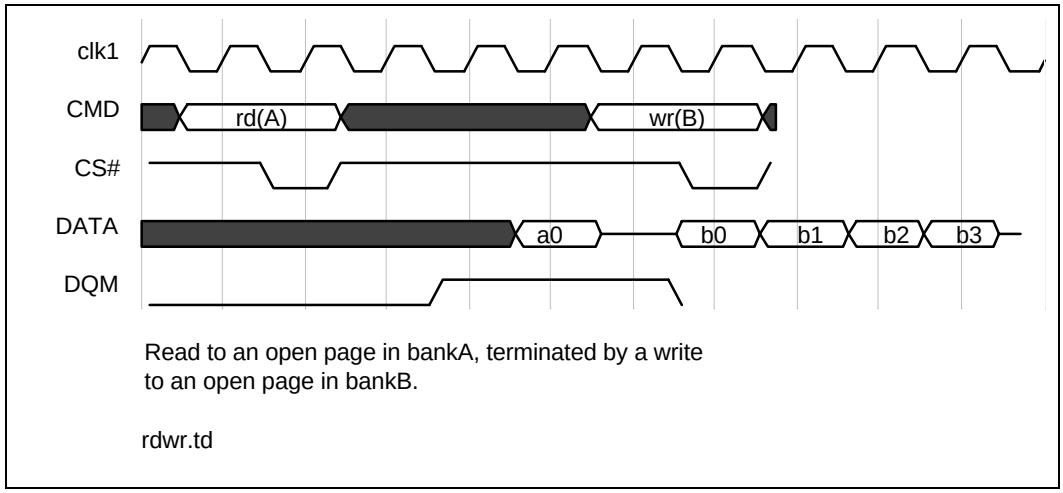
Figure 27. Multibank Timing Relationship Diagram A



Read to an open page in bankA followed by fastest read from an open page in bankB

rdrd.td

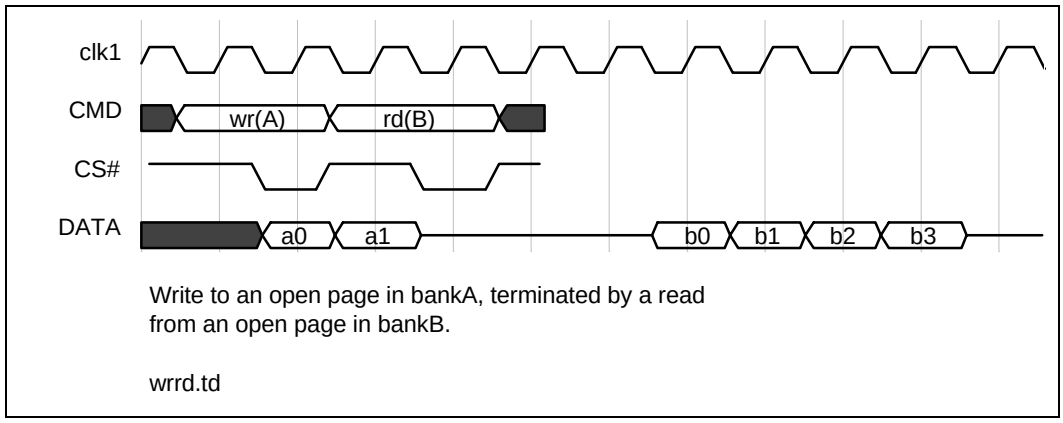
Figure 28. Multibank Timing Relationship Diagram B



Read to an open page in bankA, terminated by a write to an open page in bankB.

rdwr.td

Figure 29. Multibank Timing Relationship Diagram C



Write to an open page in bankA, terminated by a read from an open page in bankB.

wrrd.td

Figure 30. Multibank Timing Relationship Diagram D

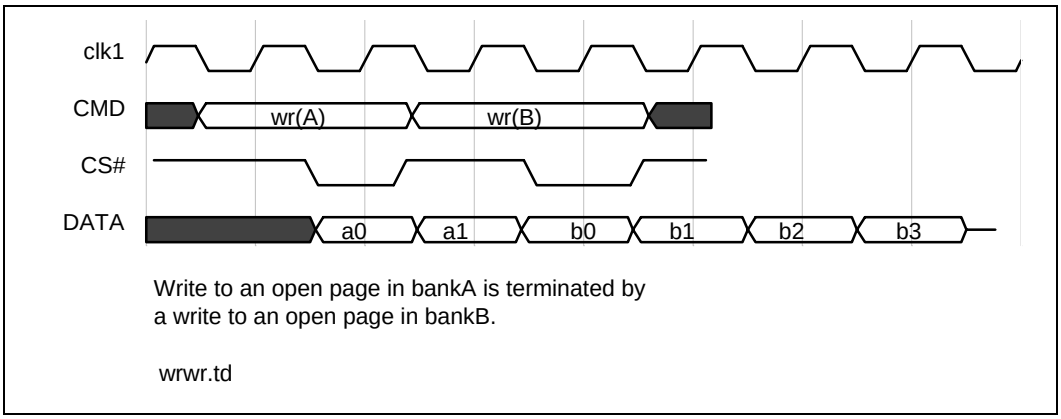


Figure 31. Multibank Timing Relationship Diagram E

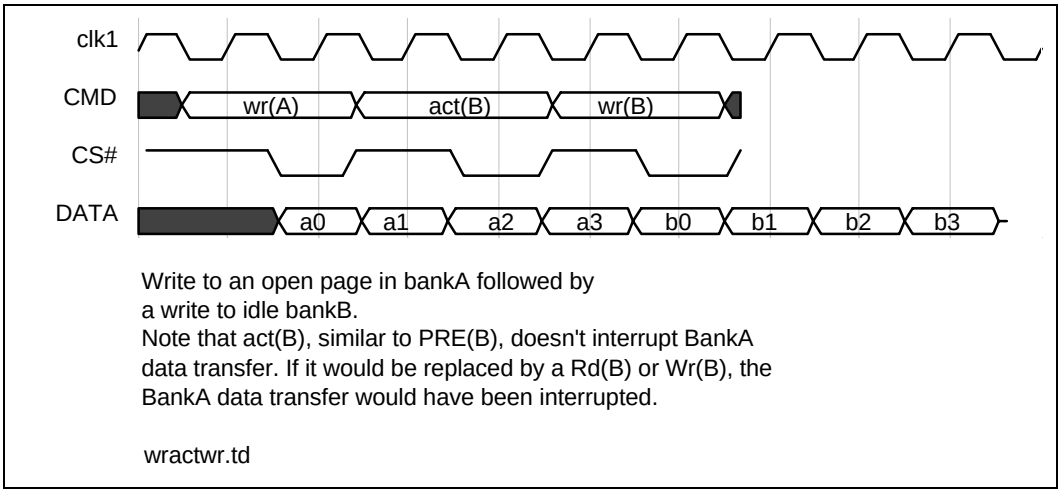


Figure 32. Multibank Timing Relationship Diagram F

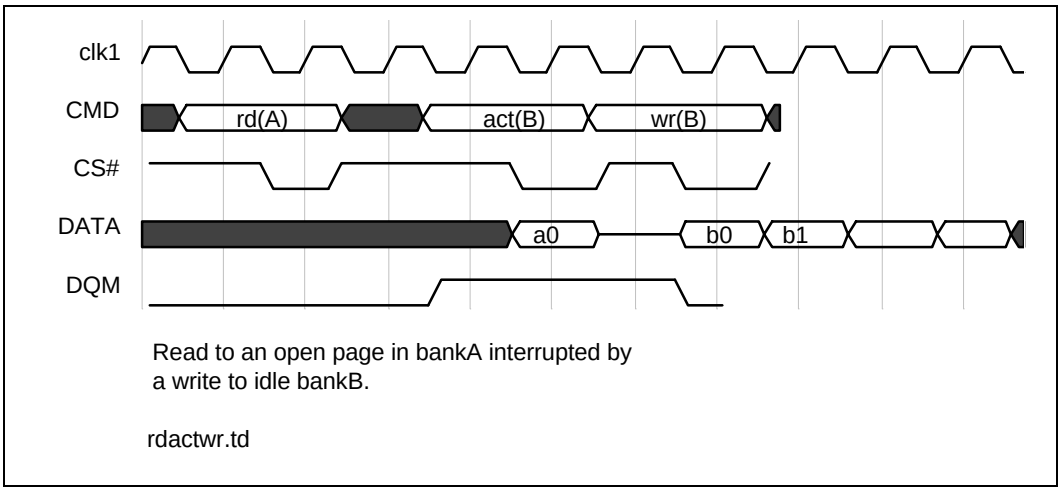
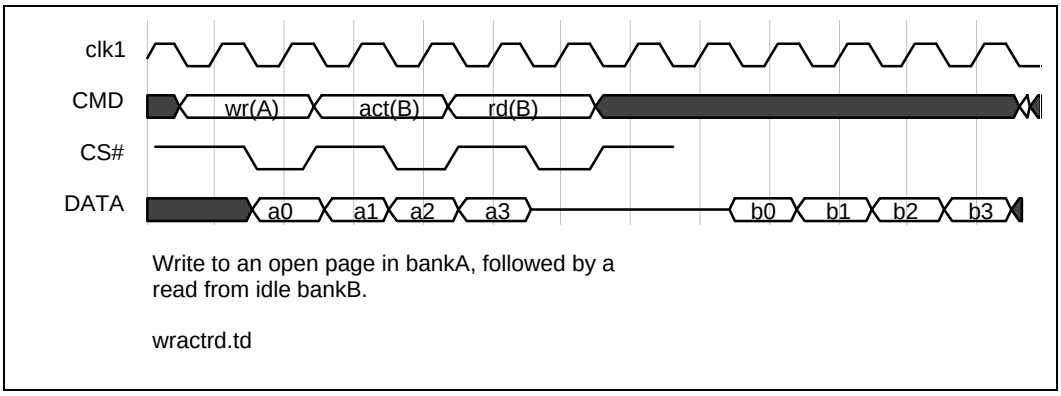


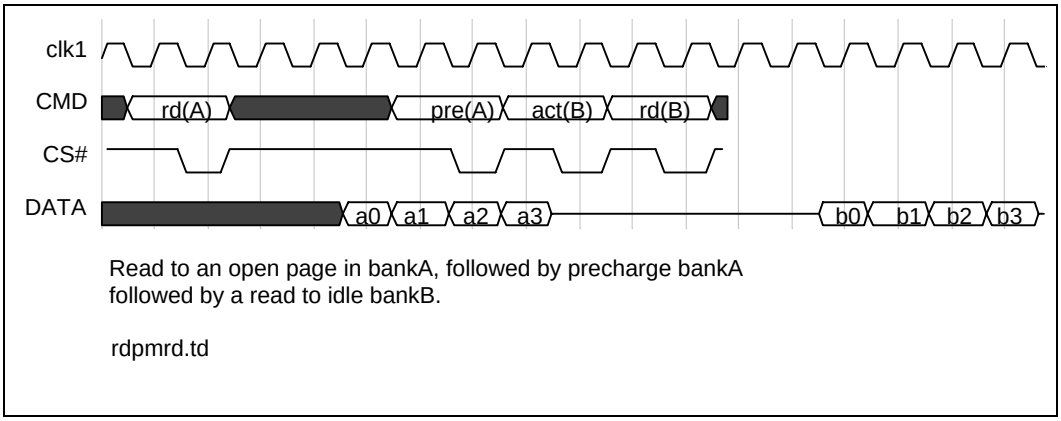
Figure 33. Multibank Timing Relationship Diagram G



Write to an open page in bankA, followed by a read from idle bankB.

wractrd.td

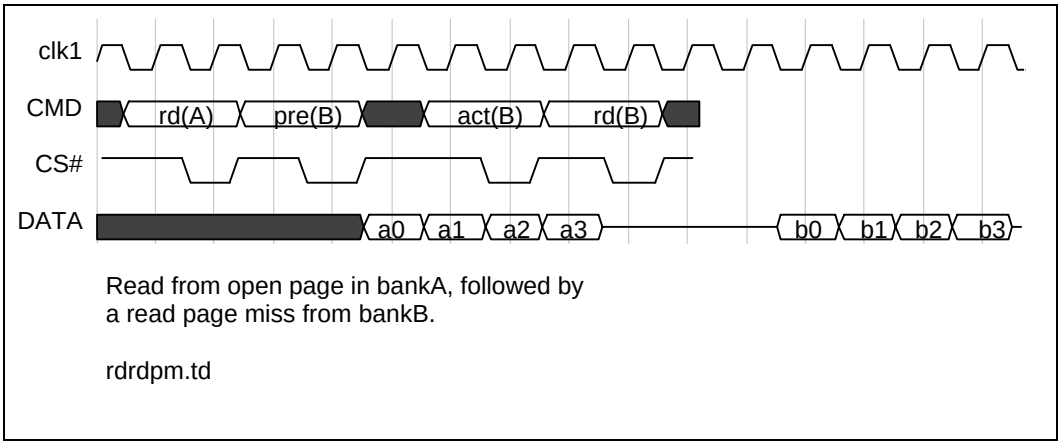
Figure 34. Multibank Timing Relationship Diagram H



Read to an open page in bankA, followed by precharge bankA followed by a read to idle bankB.

rdpmrd.td

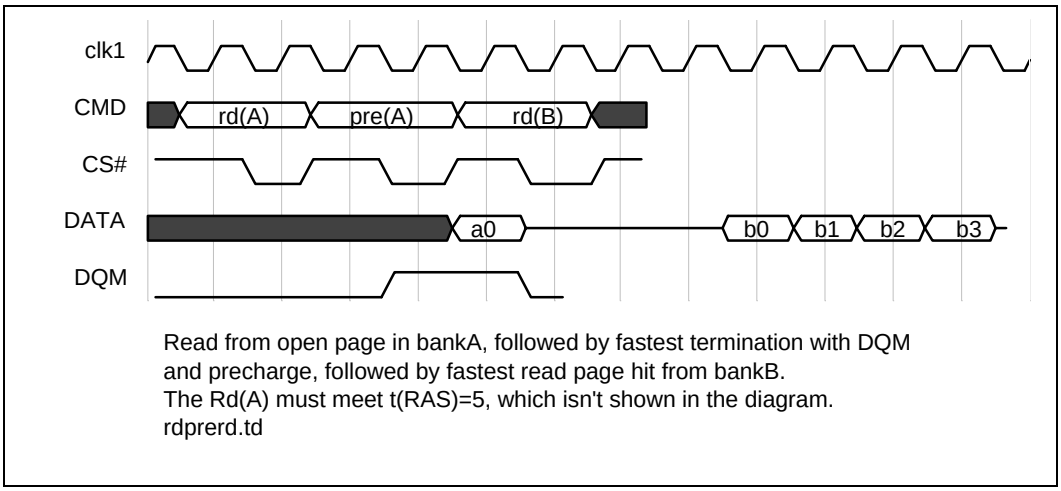
Figure 35. Multibank Timing Relationship Diagram I



Read from open page in bankA, followed by a read page miss from bankB.

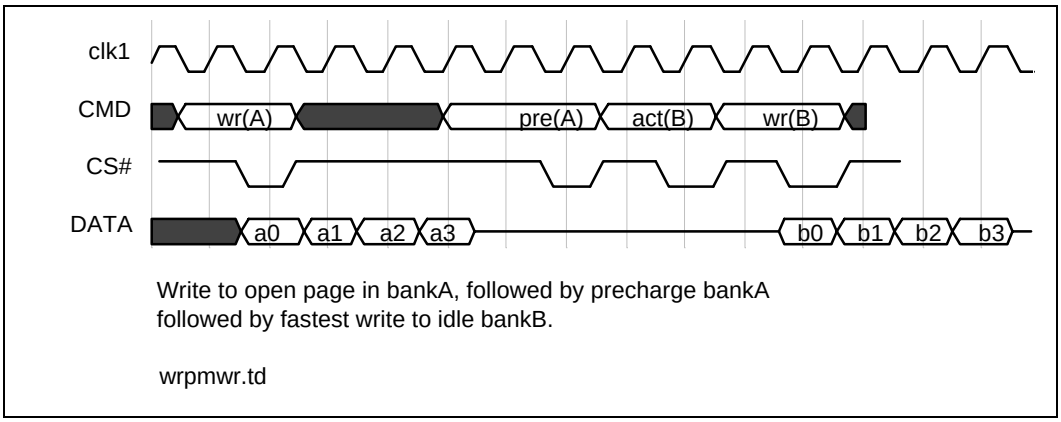
rdrdpm.td

Figure 36. Multibank Timing Relationship Diagram J



Read from open page in bankA, followed by fastest termination with DQM and precharge, followed by fastest read page hit from bankB.
The Rd(A) must meet t(RAS)=5, which isn't shown in the diagram.
rdprerd.td

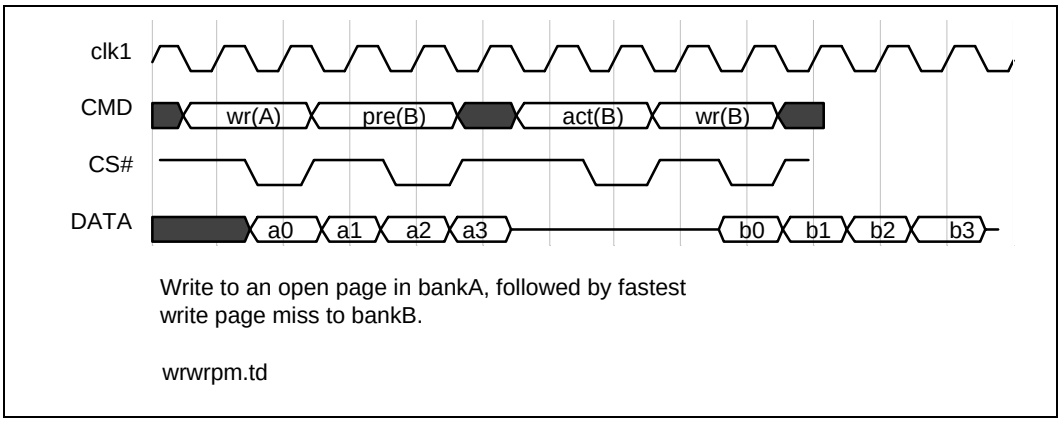
Figure 37. Multibank Timing Relationship Diagram K



Write to open page in bankA, followed by precharge bankA followed by fastest write to idle bankB.

wrpmwr.td

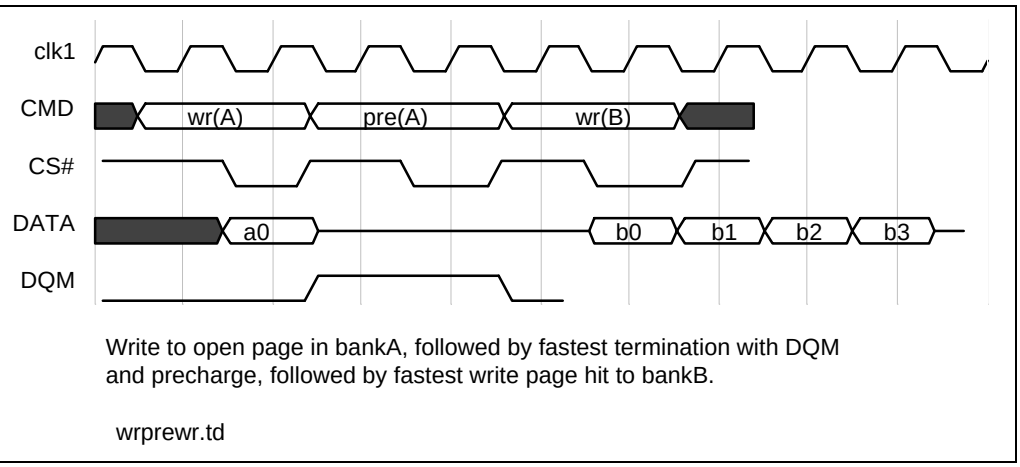
Figure 38. Multibank Timing Relationship Diagram L



Write to an open page in bankA, followed by fastest write page miss to bankB.

wrwrpm.td

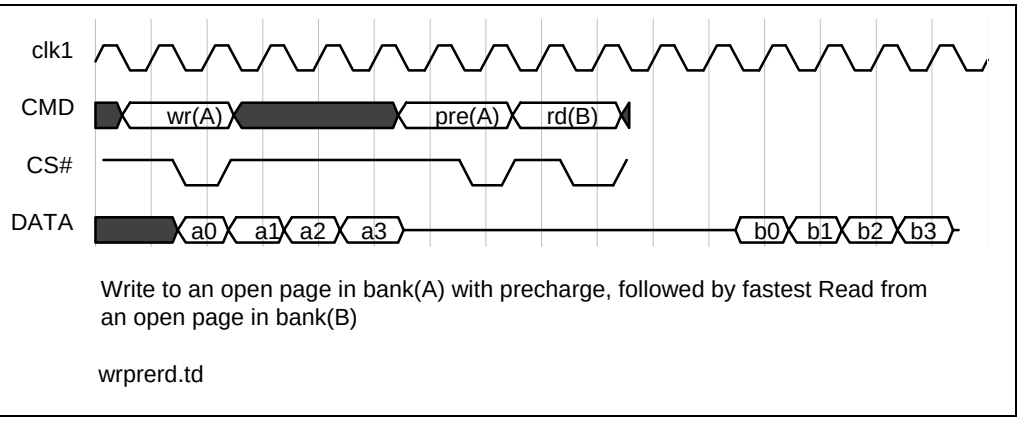
Figure 39. Multibank Timing Relationship Diagram M



Write to open page in bankA, followed by fastest termination with DQM and precharge, followed by fastest write page hit to bankB.

wrprewr.td

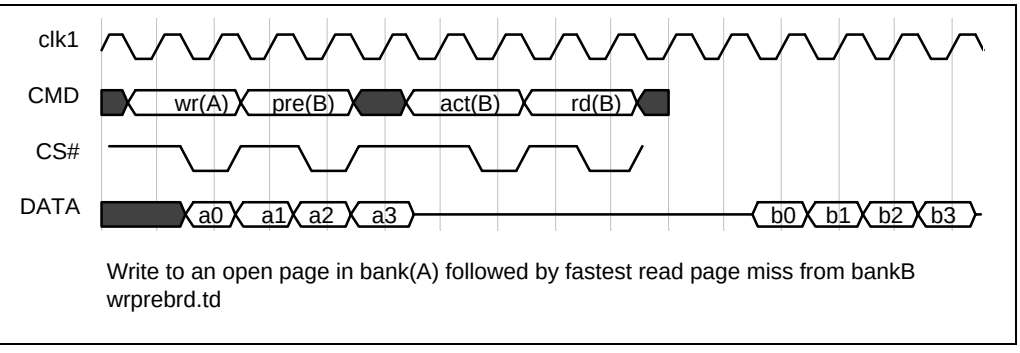
Figure 40. Multibank Timing Relationship Diagram N



Write to an open page in bank(A) with precharge, followed by fastest Read from an open page in bank(B)

wrprerd.td

Figure 41. Multibank Timing Relationship Diagram O



Write to an open page in bank(A) followed by fastest read page miss from bankB

wrprebrd.td

Figure 42. Multibank Timing Relationship Diagram P

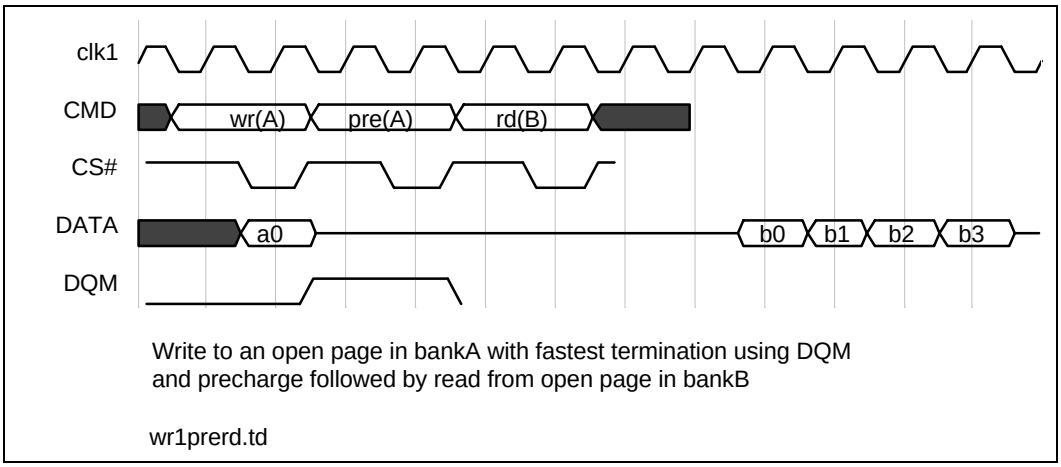


Figure 43. Multibank Timing Relationship Diagram Q

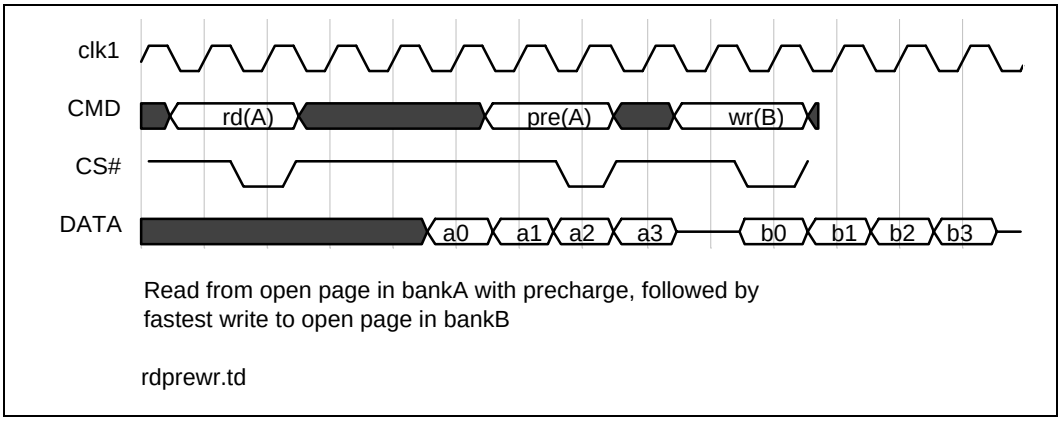


Figure 44. Multibank Timing Relationship Diagram R

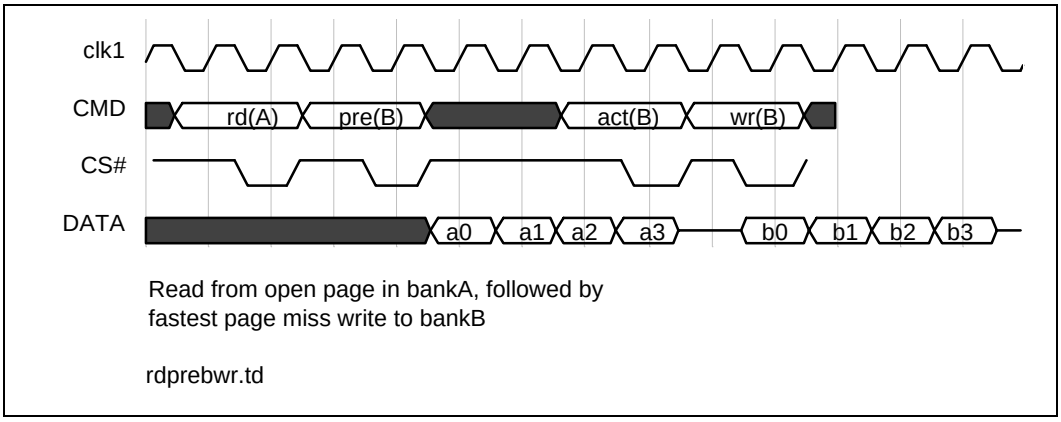
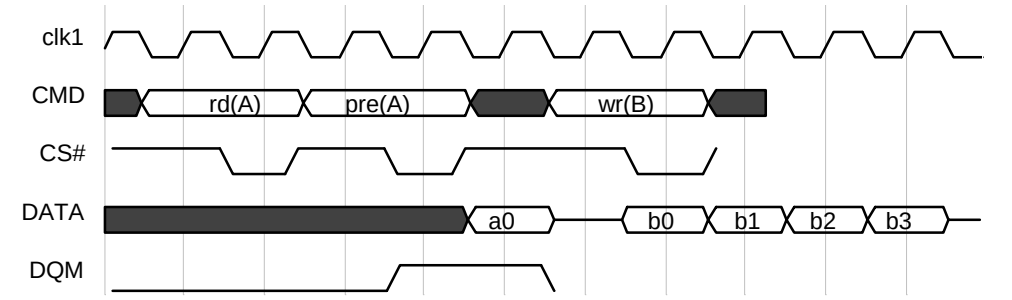


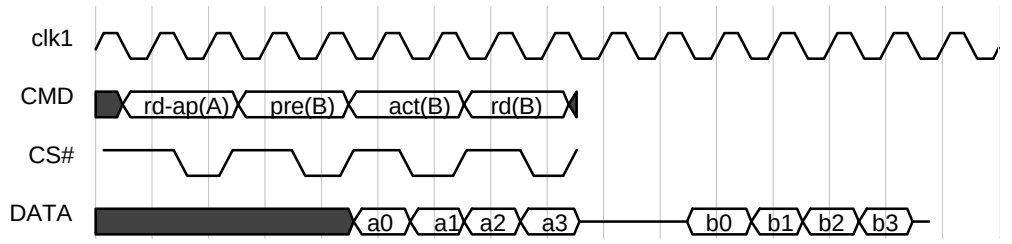
Figure 45. Multibank Timing Relationship Diagram S



Read to an open page in bankA with fastest termination, using DQM and precharge, followed by fastest write to an open page in bankB

rd1prewr.td

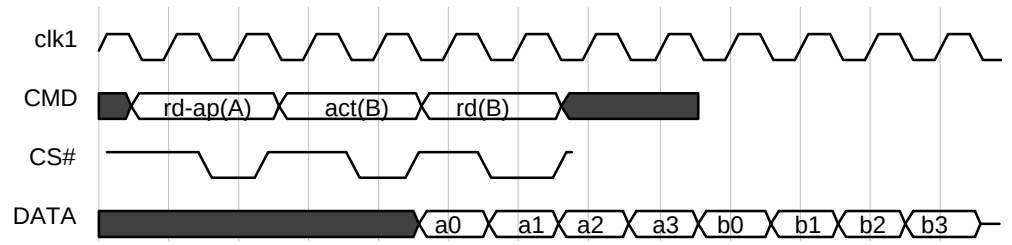
Figure 46. Multibank Timing Relationship Diagram T



Read with Auto-Precharge to an open page in bankA, followed by the fastest read page miss in bankB.
BankA is in idle state t(RP) clocks after data phase A2

rdaprd1.td

Figure 47. Multibank Timing Relationship Diagram U



Read with Auto-Precharge to an open page in bankA, followed by the fastest read from idle bankB.
BankA is in idle state t(RP) clocks after data phase A2

rdaprd2.td

Figure 48. Multibank Timing Relationship Diagram V

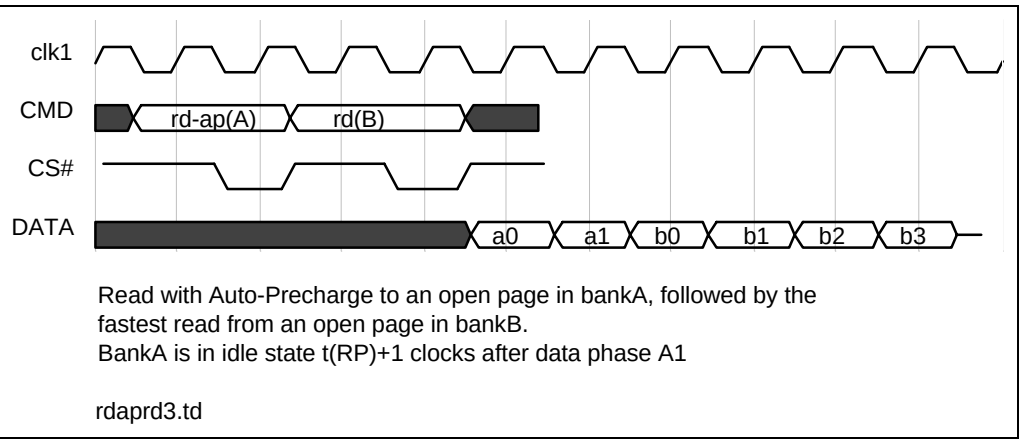


Figure 49. Multibank Timing Relationship Diagram W

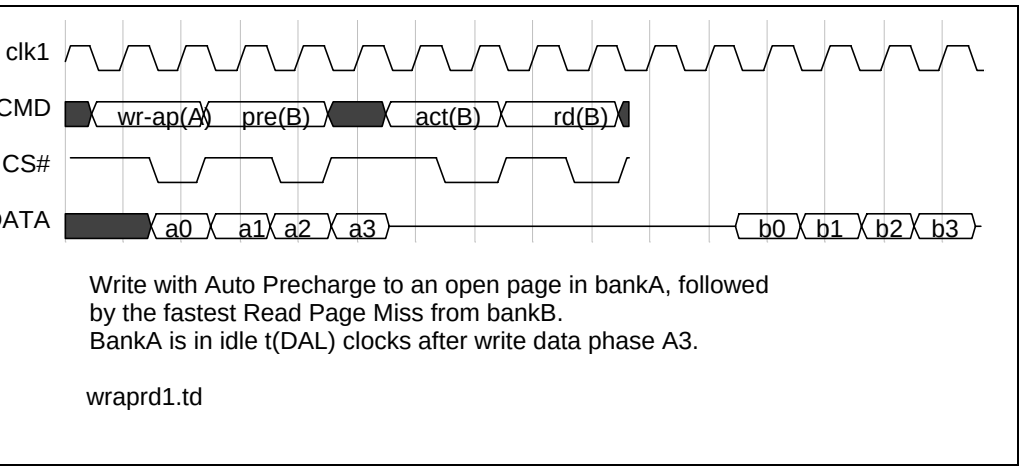


Figure 50. Multibank Timing Relationship Diagram X

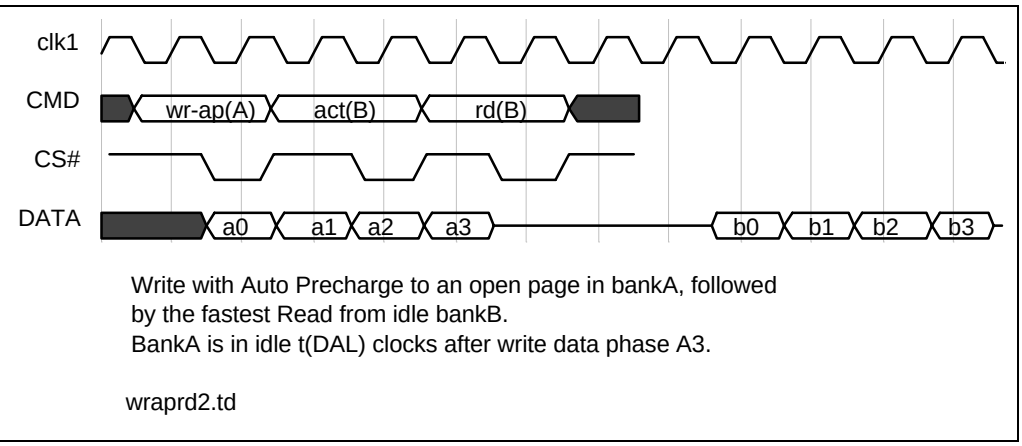
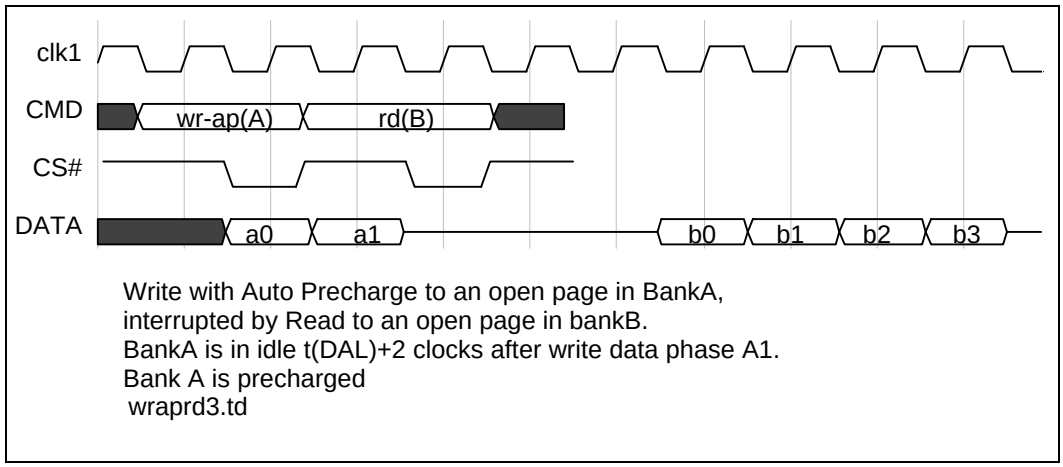
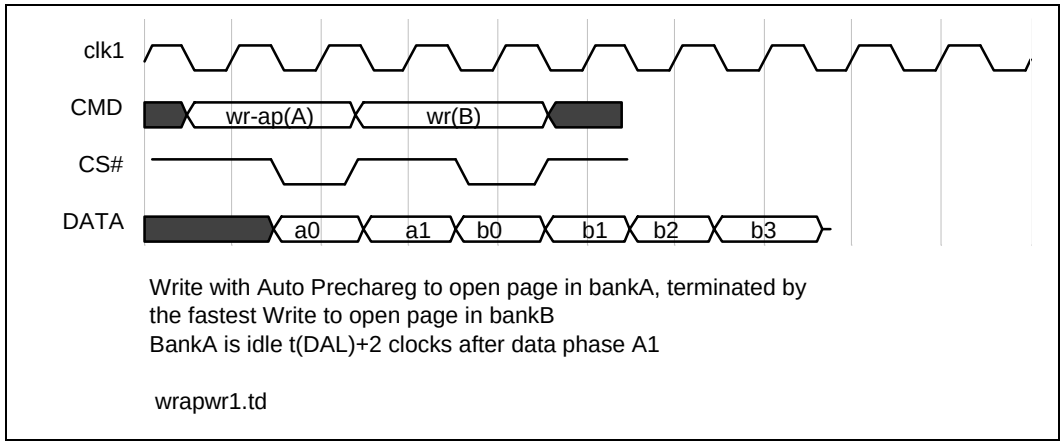


Figure 51. Multibank Timing Relationship Diagram Y



Write with Auto Precharge to an open page in BankA,
interrupted by Read to an open page in bankB.
BankA is in idle t(DAL)+2 clocks after write data phase A1.
Bank A is precharged
wraprd3.td

Figure 52. Multibank Timing Relationship Diagram Z



Write with Auto Prechareg to open page in bankA, terminated by
the fastest Write to open page in bankB
BankA is idle t(DAL)+2 clocks after data phase A1

wrapwr1.td

5.0 Synchronous DRAM AC/DC Parameters

5.1 DC Specifications

Table 15. Absolute Maximum D.C. Rating

Symbol	Parameter	Min	Max	Units	Notes
Vin, Vout	Voltage on any pin w.r.t V_{SS}	-0.5	4.5	V	
V_{DD}, V_{DDQ}	Voltage Supply pins pin w.r.t V_{SS}	-0.5	4.5	V	
Ts	Storage Temperature	-55	125	°C	

Table 16. D.C Operating Requirements

Symbol	Parameter	Condition	Min	Max	Units	Notes
VDD	Supply Voltage		3.0	3.6	V	
VDDQ	I/O Supply Voltage		3. 0	3.6	V	
Iil	Input Leakage Current	0 < Vin < VDDQ	-10	+10	µA	1,2
Icclp	Icc Low Power	CKE low, all banks closed	0	2	ma	
Iccslfrf	Icc Self Refresh Current		0	400/1000	ua	4
Iccac	Icc active	All banks open, ping-pong reads,BL=4		140/165	ma	16M/ 64M 3
Voh	Output High Voltage (For full I/V relationships see IBIS Section)	Ioh = -4 mA	2.4		V	
Vol	Output Low Voltage (For full I/V relationships see IBIS Section)	Iol = 4 mA		0.4	V	
Cin	Input Pin Capacitance	@1 MHz, 23°C Tj, 1.4v bias, 200mv swing, Vcc=3.3v	2.5	5.0	pF	Target 3.75pf
CI/O	I/O Pin Capacitance	@1 MHz, 23°C Tj, 1.4v bias, 200mv swing, Vcc=3.3v	4.0	6.5	pF	Target 5.25pf
Cclk	Pin Capacitance	@1 MHz, 23°C Tj, 1.4v bias, 200mv swing, Vcc=3.3v	2.5	4.0	pF	Target 3.25pf
Lpin	Pin Inductance			10	nH	2
Ta	Ambient Temperature	No Airflow	0	55	°C	5

NOTES:

1. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
2. This is a recommendation, not an absolute requirement. The actual value should be provided with the component data sheet.
3. No Activate or Precharge currents should be included in the Iccac value.
4. 16M/64M Low power applications may require an improved specification.
5. Components need to operate on a module in an application environment with local ambient of 55°C. Specified conditions are: 500 Mbytes/sec Read (800 Mbytes/sec being 100%), 50% data toggle rate (or 00110011 as you read per the following read definition), O LFM airflow, Cload = 60pf (emulating a 3 DIMM system). Vector definition conditions for 4 bank device: (if 2 bank then use bank A/B only)
   a. Activate Bank A
   b. Burst 4 read from bank A
   c. Activate Bank B
   d. Burst 4 read from bank B
   e. Activate Bank C
   f. Burst 4 read from bank C
   g. Activate Bank D
   h. Burst 4 read from bank D
   i. Burst 4 read from bank A
   j. Burst 4 read from bank B
   k. Burst 4 read from bank C
   l. Burst 4 read from bank D
   m. If end of page, precharge, then GOTO Step a. (open new page)
   n. Else GOTO Step i.

5.2 A.C. Specifications

Table 17. Maximum AC Operating Requirements

Symbol	Parameter	Min	Max	Units	Notes
Vih	Input High Voltage	2.0	VDDQ+2.0	V	1,2
Vil	Input Low Voltage	VSSQ – 2.0	0.8	V	1,2

NOTES:
1. The overshoot and undershoot voltage duration is <=3ns with no input clamp diodes
2. The VDDQ and VSSQ are the operating parameters (not absolute max. parameters)

Table 18. Refresh Rate

Symbol	Parameter	Min	Max	Units	Notes
Tref	Refresh rate / row	15.6/7.8		usec	1,2

NOTES:
1. The overall array refresh is determined by multiplying the specified row refresh rate by the number of rows in the total array.
2. 7.8usec refresh rate for 256M bit devices only.

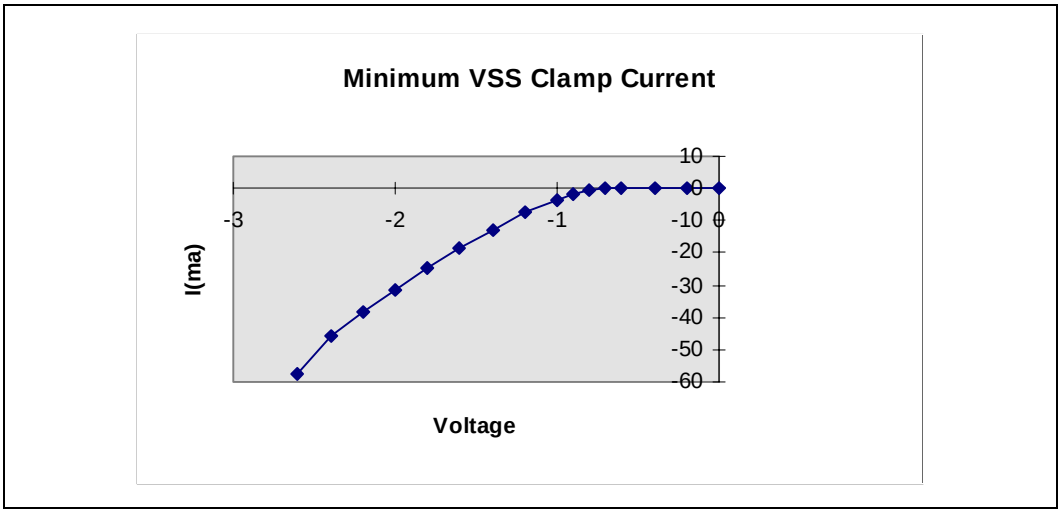
5.3 IBIS: I/V Characteristics for Input and Output Buffers

Table 19. SDRAM DQ Buffer Output Drive Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
trh	Output Rise Time	measure in linear region: 1.2v - 1.8v	1.37		4.37	Volts / nS	4
tfh	Output Fall Time	measure in linear region: 1.2v - 1.8v	1.30		3.8	Volts / nS	4
trh	Output Rise Time	measure in linear region: 1.2v - 1.8v	2.8	3.9	5.6	Volts / nS	1, 2, 3
tfh	Output Fall Time	measure in linear region: 1.2v - 1.8v	2.0	2.9	5.0	Volts / nS	1, 2, 3
$I_{ol(AC)}$	Switching Current Low	Vout = 1.65 V	75.4		---	mA	
	(Test Point)	Vout = 1.65 V	---		202.5	mA	
$I_{oh(AC)}$	Switching Current High	Vout = 1.65 V	-73.0		---	mA	
	(Test Point)	Vout =1.65 V	---		-248.0	mA	

NOTES:
1. Output rise and fall time must be guaranteed across VDD, process and temperature range.
2. Rise time specification based on 0 pF plus 50 Ohms to VSS, use these values to design to.
3. Fall time specification based on 0 pF plus 50 Ohms to VDD, use these values to design to.
4. Measured into 50pf only, use these values to characterize to.
5. All measurements done with respect to VSS.

Figure 53. SDRAM VSS Clamp Characteristics

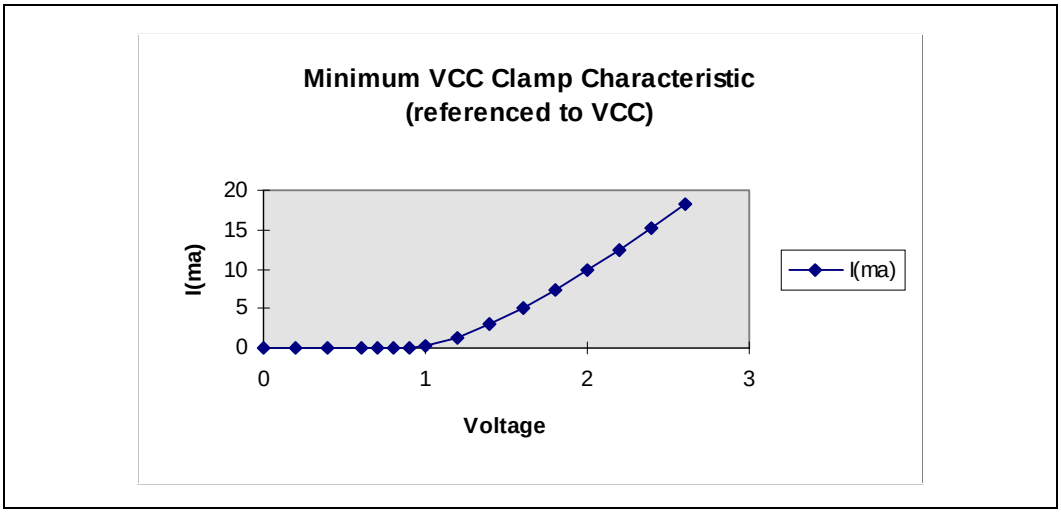


NOTES:
1. Required for CK, CS, DQMB, DQ and CKE pins.
2. Must meet the temperature and voltage range specified above.
3. This drawing is not to scale. Comparisons should be made to the data table provided.

Table 20. Data Points For Figure 53

VSS	I(ma)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.65
-1.2	-7.57
-1	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0
-0.4	0
-0.2	0
0	0

Figure 54. SDRAM VCC Clamp Characteristics

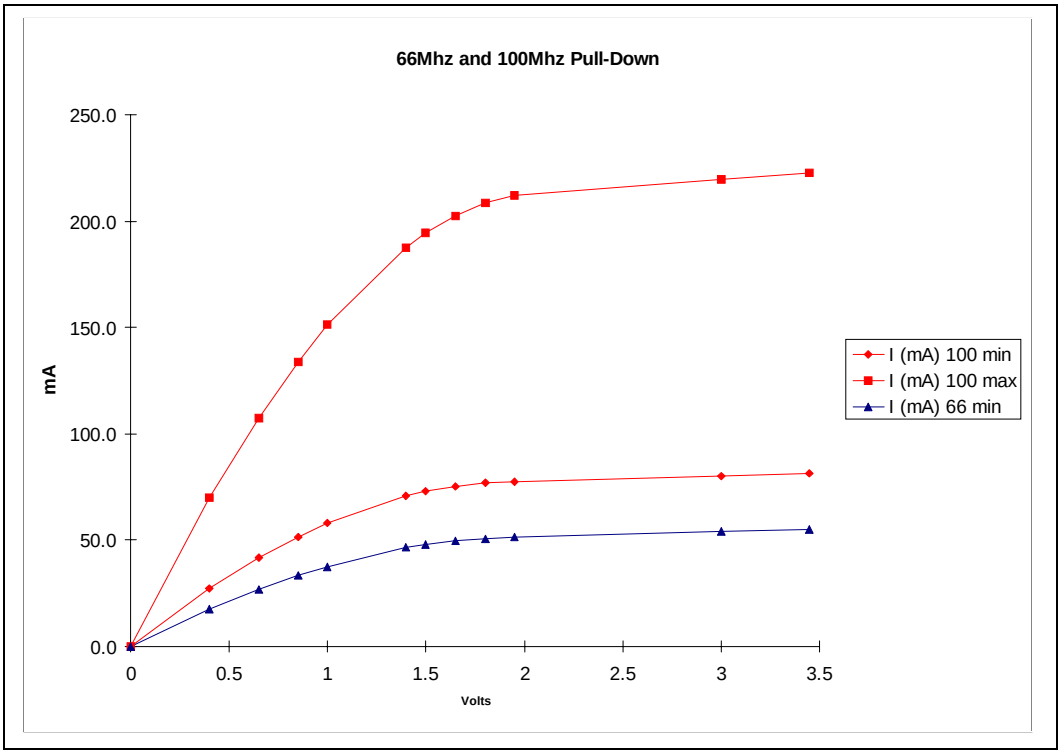


NOTES:
1. Required for CK, CS, DQMB, DQ and CKE pins.
2. This data is referenced to the VCC voltage.
3. Must meet the temperature and voltage range specified above.
4. This drawing is not to scale. Comparisons should be made to the data table provided.

Table 21. Data Points For Figure 54

VCC	I(ma)
2.6	18.31
2.4	15.3
2.2	12.48
2	9.83
1.8	7.35
1.6	5.06
1.4	3.02
1.2	1.34
1	0.23
0.9	0
0.8	0
0.7	0
0.6	0
0.4	0
0.2	0
0	0

Figure 55. SDRAM DQ Output Buffer Pull-Down Characteristics

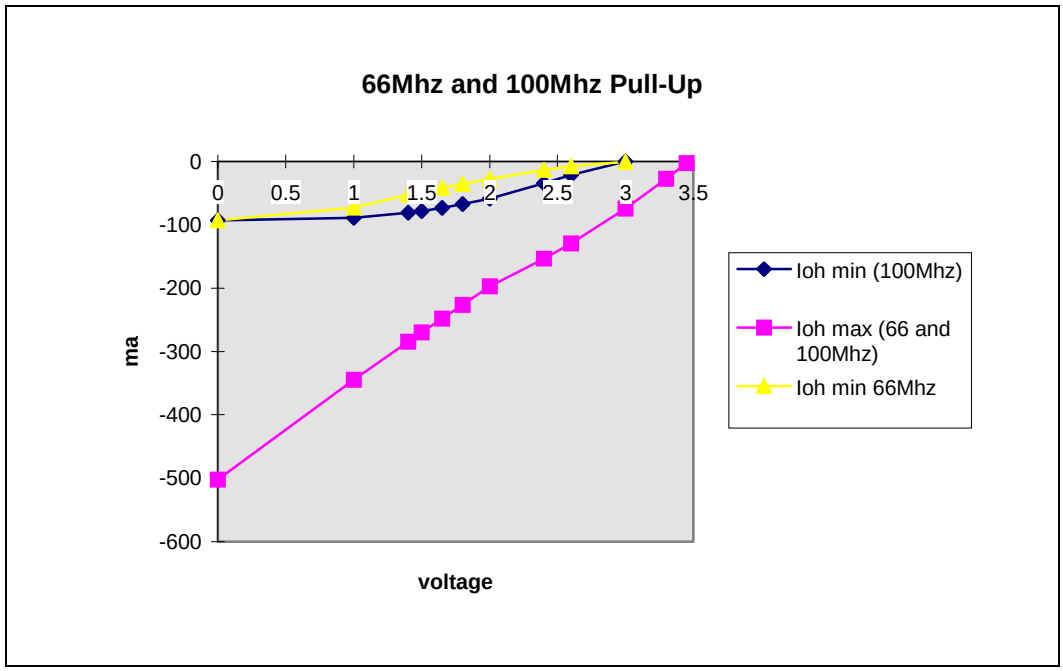


NOTES:
1. Must meet the temperature and voltage range specified above.
2. This drawing is not to scale. Comparisons should be made to the data table provided.

Table 22. Data Points For Figure 55

Pulldown			
Voltage (V)	I (ma)	I (ma)	I (ma)
	100 min	100 Max	66 min
0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3	80.3	219.6	54.2
3.45	81.4	222.6	54.9

Figure 56. SDRAM DQ Output Buffer Pull-Up Characteristics (For VCC = 3.0v - 3.45v)



NOTES:
1. Must meet the temperature and voltage range specified above.
2. This drawing is not to scale. Comparisons should be made to the data table provided.

The following are the data points for Figure 56.

Table 23. Data Points For Figure 56

Pullup			
Voltage	**100 MHz min**	**100 MHz max**	**66 MHz min**
(V)	**I(ma)**	**I(ma)**	**I(ma)**
3.45		-2.4	
3.3		-27.3	
3	0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2	-58.7	-197	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73	-248	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1	-88.6	-344.5	-72.5
0	-93	-502.4	-93

5.4 IBIS Reference

The IBIS Open Forum is an industry-wide forum that controls the official IBIS specification. Minutes of IBIS meetings, email correspondence, proposals for specification changes, etc. are on-line at "vhdl.org". To join in the email discussions, send a message to "ibis-request@vhdl.org" and request that your name be added to the IBIS mail reflector. Be sure to include your email address.

To download a copy of the specification, the golden parser, various public-domain models, the *IBIS Overview* in PostScript, and other information, either phone in by modem or use FTP.

FTP: (IP address 198.31.14.3)
login as "anonymous"
password is your email address

Modem: (408)945-4170
login as "guest"
password is your email address

IBIS-related files are in the directory "/pub/ibis" and its sub-directories.

To get documents by email, send an email message to "archive@vhdl.org" with the following commands in the message body:

path <your_email_address>
send docs <name_of_document>

For direct modem access, dial-up to the vhdl.org system at (408) 945-4170. You can use any baud rate up to 14,400, any parity, start and stop bits, and any v.* settings. Log in using the "guest" account. Simple UNIX commands such as "cd", "ls", and "cat" are available and you can download files using "kermit", "zmodem", or "sz" (another zmodem application).

For Internet access, use "ftp vhdl.org" (or "ftp 198.31.14.3") and log in as user "anonymous". The gopher utility is available and highly recommended. Gopher to "vhdl.org". Set "binary" mode for transferring binary files (*.doc, *.fm, *.xls).

The IBIS specification and overview are also available from Intel's AMO APPS BBS, via modem dial-up to (916) 356-3600.

The IBIS home page can be found at **http://www.eia.org/eig/ibis/ibis.htm**

5.5 A.C. Timing Parameters

Table 24. 100/66 MHz AC Timing Parameters For C_L=2 and 3

Parameter	Symbol	Speed Grade 66 MHz		Speed Grade[1] 100 MHz		Unit	Notes Ta 0-65C, Vcc 3.0v - 3.6v
		Min	Max	Min	Max		
Clock Period	Tclk	15		10		ns	
Clock High Time	Tch	5		3		ns	Rated @1.5V
Clock Low Time	Tcl	5		3		ns	
Input Setup Times	Tsi	3		2		ns	
Input Hold Times	Thi	1.5		1		ns	
Output Valid From Clock	Tac					ns	
CAS# Latency = 2			10.0		7.0	ns	limited application, 2 banks *all outputs switching*
CAS# Latency = 2			9.0		6.0	ns	LVTTL levels, Rated @ 50 pf *all outputs switching* 5.2ns @ 0pf
CAS# Latency = 3			9.0		6.0	ns	LVTTL levels, Rated@50pf *all outputs switching* 5.2ns @ 0pf
Output Hold From Clock	Toh	3		3		ns	3ns @ 50pf Need 1.8ns @ 0pf
Output Valid to Z	tohz	3	12	3	9	ns	
CAS# to CAS# Delay	tccd	1		1		Tclk	
CAS# Bank Delay	Tcbd	1		1		Tclk	
CKE to Clock Disable	Tcke	1		1		Tclk	
RAS# Precharge Time	Trp	3/2		3/2		Tclk	Trp=2 a SPD Option
RAS# Active Time	Tras	5		5		Tclk	
Activate to Command Delay (RAS# to CAS# Delay)	Trcd	2		3/2		Tclk	Trcd =2 a SPD Option
RAS# to RAS# Bank Activate Delay	Trrd	2		2		Tclk	
RAS# Cycle Time	Trc	8		8/7		Tclk	7 clks for trp=2
DQM# to Input Data Delay	Tdqd	0		0		Tclk	
Write Cmd. to Input Data Delay	Tdwd	0		0		Tclk	
Mode Register set to Active delay	Tmrd	3		3		Tclk	
Precharge to O/P in High-Z	Troh		CL[2]		CL[2]	Tclk	
DQM# to Data in HiZ for read	Tdqz	2		2		Tclk	

Table 24. 100/66 MHz AC Timing Parameters For C_L=2 and 3

Parameter	Symbol	Speed Grade 66 MHz		Speed Grade[1] 100 MHz		Unit	Notes Ta 0-65C, Vcc 3.0v - 3.6v
		Min	Max	Min	Max		
DQM# to Data mask for write	Tdqm	0		0		Tclk	Data Masked on the same clock
Data-in to PRE Command Period	Tdpl	2		2		Tclk	
Data-in to ACT (PRE) Command period (Auto precharge)	Tdal	5		5		Tclk	
Power Down Mode Entry	Tsb		1		1	Tclk	
Self Refresh Exit Time	Tsrx	10		1		Tclk	10ns for 66 MHz
Power Down Exit Set up Time	Tpde	1		1		Tclk	Timing is asynchronous. If Tset is not met by rising edge of CLK then CKE is assumed latched on next cycle.
Clock Stop During Self Refresh or Power Down	Tclkstp	200		200		Tclk	If the clock is stopped during self refresh or powerdown, 200 clocks are required before CKE is high

NOTES:
1. Access times to be measured w/ input signals of 1v/ns edge rate, 0.8v to 2.0v.
2. *CL* = CAS# Latency

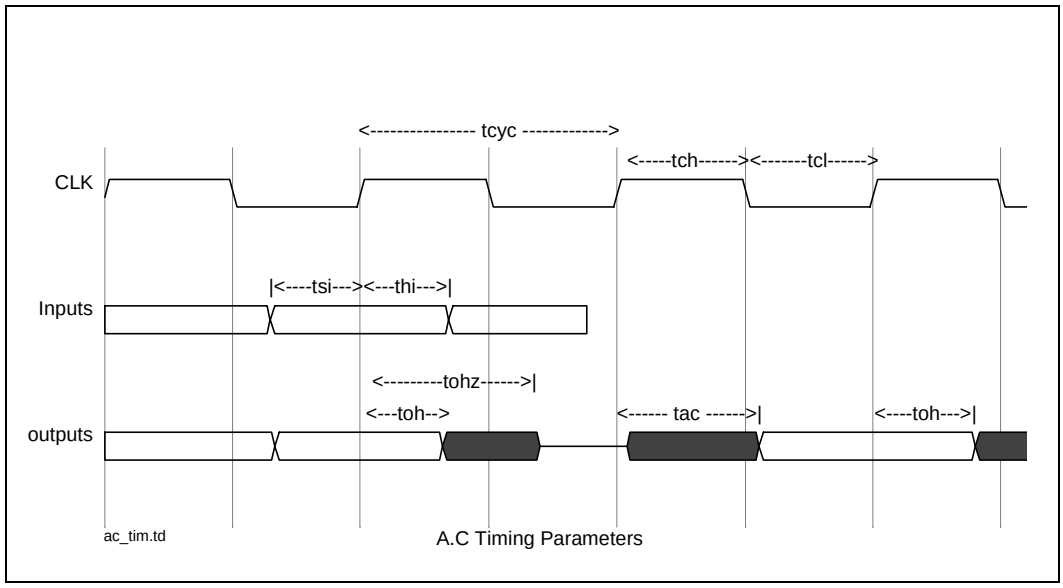
5.6 Device Options

Via SPD control on a memory module, Intel's chipset's can be programmed to effectively use either CL2 or CL3 devices and different values of Trcd and Trp. Below is a matrix for 66 MHz devices and the target for 100 MHz devices.

Table 25. Matrix for 66 MHz Devices and The Target for 100 MHz Devices

	CL	Trcd	Trp	Trc	Comment
66 MHz	3 clks	2 clks	3 clks	8 clks	
	2 clks	2 clks	3 clks	8 clks	
	2 clks	2 clks	2 clks	7 clks	
100 MHz	3 clks	3 clks	3 clks	8 clks	slowest supported
	3 clks	2 clks	2clks	7 clks	target
	3 clks	2 clks	3clks	8 clks	2nd choice
	2 clks	2 clks	2 clks	7 clks	goal

Figure 57. A.C Timing Parameters



NOTES:
1. Reference level is set at 1.5V, AC measurements are specified into 50pf load.
2. input edge rates are specified as 1.0v/ns (0.8v to 2.0v)

Figure 58. Read Cycle with timing

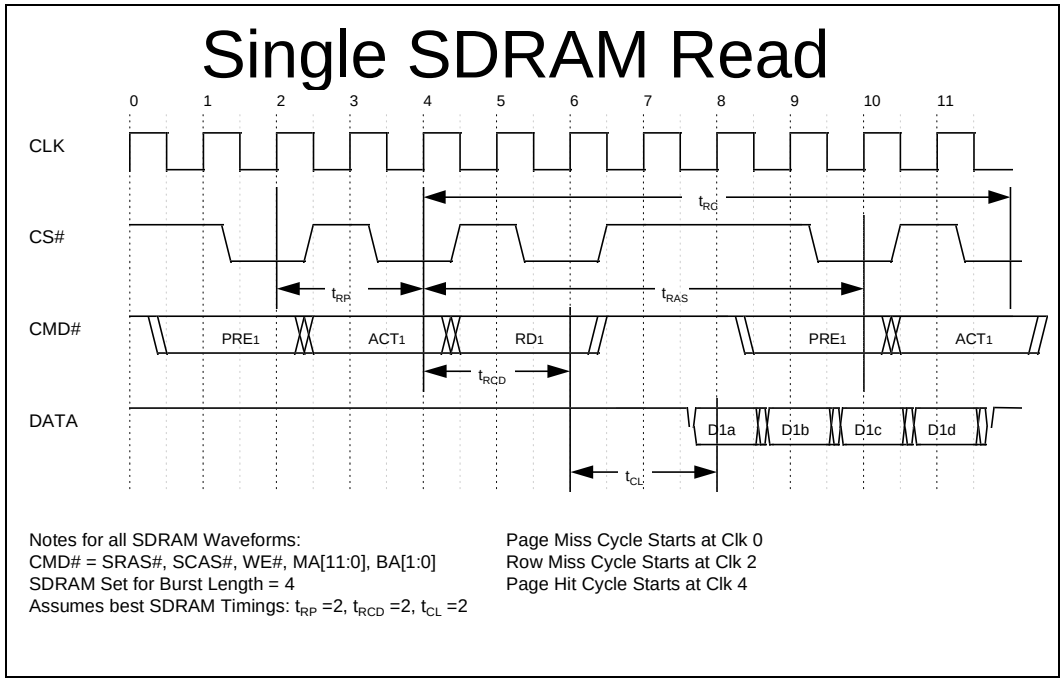
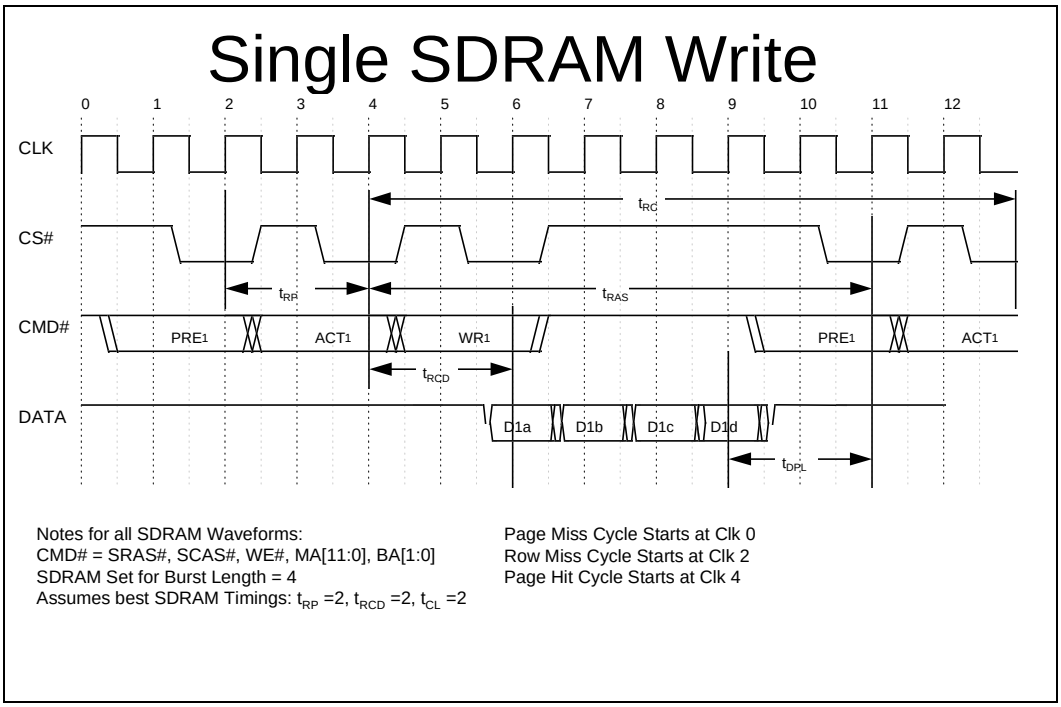


Figure 59. Write Cycle with timing



5.7 Output Load Specification

Access times for both 66 MHz and 100 MHz SDRAM devices are specified into a 50pf load only, without resistive termination.

Applications which are being simulated and implemented ***do not*** have a resistive termination.

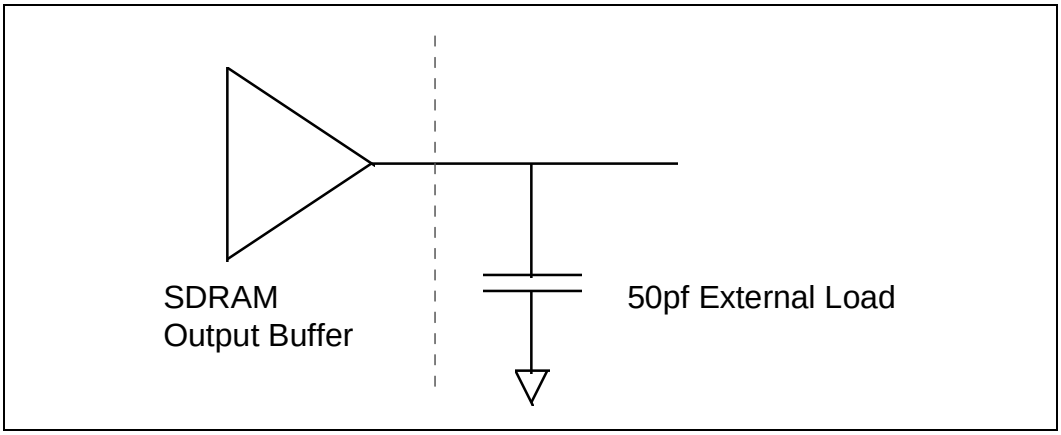
Both Tac and Toh specifications are simulated based on the following:

	66 MHz	100 MHz	Load
Tac	9ns	6ns	50pf
Toh	3ns	3ns	50pf

NOTES:
1. @ Vcc= 3.0v to 3.6v
2. @ Ta= 0C to 65C

If test conditions other than 50pf capacitive load are used, then the proper correlation factor should be used for your specific test condition.

Figure 60. Output Load Circuit



5.8 100 MHz Active Power in Application

Main memory chipset controllers for the PC will support up to 4 double sided DIMMs, or 8 rows of memory. The distributed capacitance of the data load could reach up to 80pf.

Or,

8 data lines x 6.5pf/line + controller cap + (4 x socket cap) + 3pf/DIMM trace cap x #DIMM

8 x 6.5 + 8 pf + (4 x 2) + 3 x4

52 + 8 + 8 +12 = 80pf

Vcc is specified at 3.0v to 3.6v, although 3.45v is viewed as the sustained max Vcc in the system.

Total device power can be broken into 2 segments, core power and I/O power, or:

Power (total) = Power (core) + Power (I/O)

Power (core) for 16M devices is viewed as 140ma x 3.45 = 483 mw

Power (core) for 64M devices is viewed as 165ma x 3.45 = 569 mw

Power (I/O) is ~CV^2F, where C is the distributed capacitance which the DRAM sees while driving, V is the voltage swing of the I/O and F is the data rate frequency. If clock frequency is used the power is ~1/2 cV^2F.

At 50 MHz data rate, 3.3v signal swing and 80pf capacitance

$CV^2F = 80x10^{-12} \times 3.3^{2} \times 50x10^{6}$

= 43mw per I/O for 100% read bandwidth

for 8 I/Os,

43mw x8 = 344mw

for 16 I/Os,

43mw x 16 = 640mw

For core + I/O (8Mx8 and 4Mx16 devices)

569mw + 344mw = 913mw, for 8Mx8 device.

569mw + 640mw = 1.26W , for 4Mx16 device.

Each DRAM supplier should understand the implications of this type of power for their specific design and process. The typical PC application has 0 LFM airflow over the main memory array

(natural convection applies). The specification for 0 LFM applications is a local ambient of 55C.

DIMM spacing in the application can be ~400mil spacing, center to center. The motherboard can be mounted horizontally or vertically.