# PC SDRAM Registered DIMM Design Support Document

## REVISION 1.2

October 1998

The information in this document is subject to change.

## TABLE OF CONTENTS

1 LIST OF TABLES ..... 4
2 LIST OF FIGURES ..... 5
3 REVISION HISTORY ..... 6
4 Introduction ..... 7
4.1 Related Documents 7
4.2 DIMM Configurations 8
5 Environmental Requirements ..... 8
5.1 Safety - UL Rating 8
6 Mechanical Design ..... 9
7 Module Pins ..... 17
8 SDRAM DIMM Block Diagrams ..... 19
9 DIMM Post-Register Timing ..... 26
9.1 Registered Mode 26
9.2 Buffered Mode 27
10 DIMM PCB Layout and Signal Routing ..... 28
10.1 Printed Circuit Board 28
10.2 DIMM PCB and final assembly labeling requirements 30
10.2.1 DIMM Naming Convention 30
10.2.2 Printed Circuit Board Labeling 30
10.3 Component Types and Placement 31
10.4 Signal Groups 32
10.5 Signal Topology and Length Restrictions 32
10.5.1 Routing Rules 32
10.5.2 Topology Diagram Explanation and Examples 33
10.5.3 Topology for Clock: CK[3:0] 35
10.5.4 Topology for Data: DQ[63:0] & CB[7:0] 39
11 SDRAM Component Specifications ..... 50
12 EEPROM Component Specifications ..... 51
13 Register Component Specifications ..... 52
14 PLL Component Specifications ..... 58

# 1 LIST OF TABLES

TABLE 1: RELATED DOCUMENTS 7
TABLE 2: SDRAM MODULE CONFIGURATIONS 8
TABLE 3: DIMM ENVIRONMENTAL REQUIREMENTS 8
TABLE 4: DIMM DIMENSIONS AND TOLERANCES 9
TABLE 5: REGISTERED DIMM MODULE PINOUT 17
TABLE 6: PIN DESCRIPTIONS 18
TABLE 7: REGISTERED / BUFFERED MODE OPERATION 18
TABLE 8: EXAMPLE OF REGISTERED MODE TIMING 26
TABLE 9: EXAMPLE OF BUFFERED MODE TIMING 27
TABLE 10: PCB CALCULATED PARAMETERS 28
TABLE 11: SIGNAL TOPOLOGY CATEGORIES 32
TABLE 12: TRACE LENGTH AND COMPONENT VALUE TABLE FOR DIMM CONNECTOR TO PLL CLOCK-IN TOPOLOGIES 37
TABLE 13: TRACE LENGTH TABLE FOR CLOCK TOPOLOGIES 38
TABLE 14: TRACE LENGTH TABLE FOR DATA TOPOLOGIES 39
TABLE 15: TRACE LENGTH TABLE FOR DATA MASK TOPOLOGIES (2/4 LOADS) 40
TABLE 16: TRACE LENGTH TABLE FOR DATA MASK TOPOLOGIES (1/2/3/6 LOADS) 41
TABLE 17: TRACE LENGTH TABLE FOR CHIP SELECT TOPOLOGIES (S0, S1) 42
TABLE 18: TRACE LENGTH FOR CHIP SELECT TOPOLOGIES (S0, S1, S2, S3) 43
TABLE 19: TRACE LENGTH TABLE FOR ADDRESS AND CONTROL SIGNALS 44
TABLE 20: TRACE LENGTH TABLE FOR ADDRESS AND CONTROL SIGNALS CONTD. 44
TABLE 21: TRACE LENGTH TABLES FOR CLOCK ENABLE TOPOLOGIES 45
TABLE 22: TRACE LENGTH TABLES FOR CLOCK ENABLE TOPOLOGIES 46
TABLE 23: TRACE LENGTH TABLE FOR ADDRESS AND CONTROL SIGNALS 47
TABLE 24: RESISTANCE VALUES IN THE ADDRESS AND CONTROL SIGNAL TOPOLOGIES 48
TABLE 25: TRACE LENGTH TABLE FOR WRITE ENABLE 49
TABLE 26: STACKED COMPONENT PIN CAPACITANCE 50
TABLE 27: DIMM REGISTER USE 52
TABLE 28: REGISTER SPECIFICATION PARAMETRICS 52
TABLE 29: 16835 I-V DATA 55
TABLE 30: 162835 I-V DATA 57
TABLE 31: PLL COMPONENT SPECIFICATIONS 58
TABLE 32: DIMM PLL USE 59
TABLE 33: PLL OUTPUT I-V DATA 61

# 2 LIST OF FIGURES

FIGURE 1: DIMM MECHANICAL DRAWING (1 OF 5) 12
FIGURE 2: DIMM MECHANICAL DRAWING (2 OF 5) 13
FIGURE 3: DIMM MECHANICAL DRAWING (3 OF 5) 14
FIGURE 4: DIMM MECHANICAL DRAWING (4 OF 5) 15
FIGURE 5: DIMM MECHANICAL DRAWING (5 OF 5) 16
FIGURE 6: 64MBYTE 72-BIT ECC SDRAM DIMM BLOCK DIAGRAM (1 ROW X8 SDRAMS) 19
FIGURE 7: 64MBYTE 72-BIT ECC SDRAM DIMM BLOCK DIAGRAM (1 ROW X8 SDRAMS) 20
FIGURE 8: 72-BIT ECC UNSTACKED SDRAM DIMM BLOCK DIAGRAM (1 ROW X4 SDRAMS) 21
FIGURE 9: 72-BIT ECC STACKED SDRAM DIMM BLOCK DIAGRAM (2 ROWS X4 SDRAMS) 22
FIGURE 10: REGISTER WIRING ON 64MBYTE DIMMS 23
FIGURE 11: REGISTER WIRING FOR DIMM USING 18 SDRAMS 23
FIGURE 12: REGISTER WIRING FOR STACKED DIMM USING 36 SDRAMS 24
FIGURE 13: STACKED SDRAM COMPONENT PINOUT 24
FIGURE 14: CLOCK LOADING TABLE & WIRING DIAGRAM 25
FIGURE 15: EXAMPLE 6-LAYER STACKUP FOR 6 MIL TRACES 28
FIGURE 16: EXAMPLE 6-LAYER STACKUP FOR 4 MIL TRACES 29
FIGURE 17: EXAMPLE 256MBYTE COMPONENT PLACEMENT 31
FIGURE 18: EXAMPLE TOPOLOGY 34
FIGURE 19: DIMM CLOCK REFERENCE AND TIMING (NOT TO SCALE) 36
FIGURE 20: SIGNAL ROUTING TOPOLOGIES FOR CLOCKS PRE-PLL 37
FIGURE 21: SIGNAL ROUTING TOPOLOGIES FOR CLOCKS POST-PLL 38
FIGURE 22: SIGNAL ROUTING TOPOLOGIES FOR DATA 39
FIGURE 23: SIGNAL ROUTING TOPOLOGIES FOR DATA MASK (1/2/4 LOADS) 40
FIGURE 24: SIGNAL ROUTING TOPOLOGIES FOR DATA MASK (3/6 LOADS) 41
FIGURE 25: SIGNAL ROUTING TOPOLOGIES FOR CHIP SELECT (64MB) 42
FIGURE 26: SIGNAL ROUTING TOPOLOGIES FOR CHIP SELECT (> 64MB DIMM) 43
FIGURE 27: SIGNAL ROUTING TOPOLOGIES FOR CLOCK ENABLE (64MB) 44
FIGURE 28: SIGNAL ROUTING TOPOLOGIES FOR CLOCK ENABLE (UNSTACKED DIMM) 45
FIGURE 29: SIGNAL ROUTING TOPOLOGIES FOR CLOCK ENABLE (STACKED DIMM) 46
FIGURE 30: SIGNAL ROUTING TOPOLOGIES FOR ADDRESS AND CONTROL SIGNALS 47
FIGURE 31: SIGNAL ROUTING TOPOLOGIES FOR WRITE ENABLE (STACKED DIMM) 49
FIGURE 32: I-V CHARACTERISTICS FOR 16835 REGISTER OUTPUT – PULL DOWN 54
FIGURE 33: I-V CHARACTERISTICS FOR 16835 REGISTER OUTPUT – PULL UP 54
FIGURE 34: I-V CHARACTERISTICS FOR 162835 REGISTER OUTPUT – PULL DOWN 56
FIGURE 35: I-V CHARACTERISTICS FOR 162835 REGISTER OUTPUT – PULL UP 56
FIGURE 36: I-V CHARACTERISTICS FOR PLL OUTPUT – PULL UP 60
FIGURE 37: I-V CHARACTERISTICS FOR PLL OUTPUT – PULL DOWN 60

# 3 REVISION HISTORY

**Revision 0.8: December 1997**

- Added post register timing information
- Add PLL critical specifications
- Add register critical specifications
- Corrected register part numbers
- Updated post register timing information
- Added new 256MB Topology information
- Added preliminary information on the 64MB DIMM without the PLL
- Added preliminary information on adapting the spec for 512MB DIMM

**Revision 1.0: February 1998**

- Updated Introduction section
- Updated information for the 64MB DIMM without the PLL
- Updated all topology and component value tables
- Corrected PLL part numbers
- Modified PLL component requirements to support SSC synthesizers
- Added VI curves for the Register and PLL

**Revision 1.1: August 1998**

- Updated Introduction section
- Updated information for the 512MB and 1024MB DIMM designs
- Added Buffered mode documentation
- Renumbered Chapters
- Updated Chapter 10:
    - clock distribution tuning methodology
    - register offset timing
    - New clock topologies for 128MB design
    - New C1 spec capacitance, and C3 recommended tuning capacitance
- Updated Chapter 13:
    - removed manufacturer references for registers
    - added detailed register specifications
    - modified and consolidated IBIS I/V curves
- Updated Chapter 14:
    - removed manufacturer references for PLL components
    - added detailed PLL specifications
    - modified IBIS I/V curves to reflect min-max I/V limits

**Revision 1.2: October 1998**

- Added Test conditions in Register and PLL specifications
- Modified Environmental Requirements
- Added UL Requirements
- Updated stacked SDRAM component pin capacitance values

# 4 Introduction

This document defines the electrical and mechanical requirements for the 168-pin, 3.3 volt, 72-bit wide, PC SDRAM Registered DIMM. It is intended to serve as a guide to the DIMM designer, as well as the system integrator of the DIMM. This DIMM supports two modes of operation: (a) Buffered mode at 66* MHz or (b) Registered mode at 100 MHz. The PC SDRAM Registered DIMM is intended for use as main memory when installed on personal computer motherboards.

***Note: all references to 66 MHz imply 66.67 MHz (15ns clock period).**

A reference design example is presented in this document. The reference design is intended to provide an initial basis for a registered DIMM design. Modifications to this reference design may be required to meet all system timing, signal integrity and thermal requirements for 66 MHz or 100 MHz support. All registered DIMM implementations must use simulations and lab verification to insure proper timing requirements and signal integrity in the design.

The 256MB, 512MB and 1GB registered DIMMs are implemented using a stacked SDRAM package approach. Other SDRAM packaging implementations may be used.

## 4.1 Related Documents

**Table 1: Related Documents**

| Title | Rev |
|---|---|
| Intel PC SDRAM Specification | Latest Revision |
| Intel PC SDRAM SPD Data Structure Specification | Latest Revision |

## 4.2 DIMM Configurations

SDRAM DIMM configurations are defined in the following table:

**Table 2: SDRAM Module Configurations**

| Config # | DIMM Capacity | DIMM Organization | SDRAM density | SDRAM Organization | # of SDRAMs | # Rows of SDRAM | # Banks in SDRAM | # Address bits row/bank/col |
|---|---|---|---|---|---|---|---|---|
| 1 | 64 MB | 8M X 72 | 64Mbit | 8M X 8 | 9 | 1 | 4 | 12/2/9 |
| 2 | 128 MB | 16M X 72 | 64Mbit | 16M X 4 | 18 | 1 | 4 | 12/2/10 |
| 3 | 256 MB | 32M X 72 | 64Mbit | 16M X 4 | 36 | 2 | 4 | 12/2/10 |
| 4 | 256MB | 32M X 72 | 128Mbit | 32M X 4 | 18 | 1 | 4 | 12/2/11 |
| 5 | 512MB | 64M X 72 | 128Mbit | 32M x 4 | 36 | 2 | 4 | 12/2/11 |
| 6 | 512MB | 64M X 72 | 256Mbit | 64M x 4 | 18 | 1 | 4 | 13/2/11 |
| 7 | 1024 MB | 128M X 72 | 256Mbit | 64M x 4 | 36 | 2 | 4 | 13/2/11 |

# 5 Environmental Requirements

The Registered SDRAM DIMM shall be designed to operate within a personal computer cabinet in an office environment with limited capacity for heating and air conditioning. The temperature and humidity limits are listed below.

**Table 3: DIMM Environmental Requirements**

| Parameter | Range |
|---|---|
| Operating Temperature | System Operating Conditions[1]:<br>0-55 deg C ambient<br>500 MB/sec sustained READ<br>0 LFM airflow |
| Operating Humidity | 10% to 90% relative humidity |
| Storage Temperature | -50 $^{o}$C to + 100 $^{o}$C |
| Storage Humidity | 5% to 95% without condensation |
| Altitude (operating & storage) | -500 ft. to 10,000 ft. |

1 Actual system operating conditions may vary, depending upon airflow, maximum allowed memory bandwidth, and ambient temperature.

## 5.1 Safety - UL Rating

Printed circuit board to have a flammability rating of 94V-0. Markings to include UL tractability requirements per UL Recognized Component Directory.

# 6 Mechanical Design

The following table and mechanical drawings give the specific dimensions and tolerances for a 168-pin Registered DIMM.

**Table 4: DIMM Dimensions and Tolerances**

| DIMM Dimensions and Tolerances | | | | | |
|---|---|---|---|---|---|
| **SYMBOL** | **DEFINITION** | **MIN** | **NOM** | **MAX** | **NOTES** |
| A | Overall module height measured from Datum -B-. | | 38.12 mm | 43.18 mm | Nominal is 38.10 mm. (1.5”). Max is 43.18 (1.7”). |
| A1 | The distance from Datum -B- to the centerline of the PWB alignment holes. | 3.00 mm BASIC | | | These holes are not used by the next level of assembly. The dimensions are supplied for information only. If the holes are used in manufacturing they should be tightly toleranced. The recommended positional tolerance is 0.10 mm. |
| A2 | The distance from Datum -B- to the centerline of the latch holes. | 17.80 mm BASIC | | | |
| A3 | The distance from Datum -B- to the lower edge of the Component Area. | 20.80 mm | | | This distance applies to the Component Area in the latch hole area. |
| A4 | The distance from Datum -B- to the lower edge of the Component Area on the front side of the PWB. | 4.00 mm | | | |
| A5 | The distance from Datum -B- to the lower edge of the Component Area on the back side of the PWB. | 4.00 mm | | | |
| A6 | The distance from Datum -B- to the leading edge of the contact. | 0.05 mm | | 0.35 mm | The minimum distance prevents contact edge burrs. |
| B | The width of the plated input/output contact measured at the lateral midpoint of the contact. | 0.95 mm | 1.00 mm | 1.05 mm | |
| D1 | The overall length of the PWB. | 133.22 mm | 133.37 mm | 133.52 mm | |
| D2 | The longitudinal distance between the PWB machining alignment hole centers. | 126.20 mm | 127.35 | 128.50 mm | These holes are optional and may or may not be present. If they are present, they must be located as defined. |

| DIMM Dimensions and Tolerances | | | | | |
|---|---|---|---|---|---|
| **SYMBOL** | **DEFINITION** | **MIN** | **NOM** | **MAX** | **NOTES** |
| E | The pitch or distance between centerlines of the contacts | | 1.27 mm BASIC | | |
| e1 | The distance between the centerlines of Contact 1 and 84. | | 115.57 mm | | |
| e2 | The distance between the centerlines of Contact 85 and 168. | | 115.57 mm | | |
| e3 | The distance between the centerlines of Contact 1 and the contact located at the immediate left of the left key zone when viewing contact 1 side. | | 11.43 mm | | The distance between the centerlines of contact 1 and 10. |
| e4 | The distance between the centerlines of the contact at the immediate right of the left key zone and the contact at the immediate left of the center key zone when viewing contact 1 side. | | 36.83 mm | | The distance between the centerlines of contact 11 and 40. |
| e5 | The distance between the centerlines of the contact located at the immediate right of the center key zone and contact 84. | | 54.61 mm | | The distance between the centerlines of contact 41 and 84. |
| H | The diameter of the PWB machined alignment holes. | 2.90 mm | 3.00 mm | 3.10 mm | The machined alignment holes are optional. |
| L | The distance from Datum -B- to the top edge of the plated contact. | 2.30 mm | 2.50 mm | 2.70 mm | |
| N | The total number of contacts. | | 168 | | |
| T | The thickness of the PCB including the contact metalization and plating. | 1.17 mm | 1.27 mm | 1.37 mm | |
| T1 | The overall thickness of the PWB with the components mounted. The overall thickness is measured from the highest component on the front side to the highest component on the backside. | | | 8.13 mm | |
| Aaa | The positional tolerance for the overall body length D1. | aaa = 0.15 mm @ Maximum Material Condition | | | |
| Bbb | The straightness tolerance for the card thickness including the metalized contacts. This callout applies to the zone defined by A4, A5 and D1. | | 0.40 mm | | bbb = 0.3% x D1 rounded to a two decimal place hard metric value. |
| | The positional tolerance for | | | | |

| DIMM Dimensions and Tolerances | | | | | |
|---|---|---|---|---|---|
| **SYMBOL** | **DEFINITION** | **MIN** | **NOM** | **MAX** | **NOTES** |
| Ccc | the pattern of contacts with regard to primary Datum -A-. | | ccc = 0.10 mm @ Least Material Condition | | |
| Ddd | The positional tolerance for the individual contact width b with regard to the theoretical centerline of the contact defined by basic dimension e. | | ddd = 0.05 mm @ Least Material Condition | | |

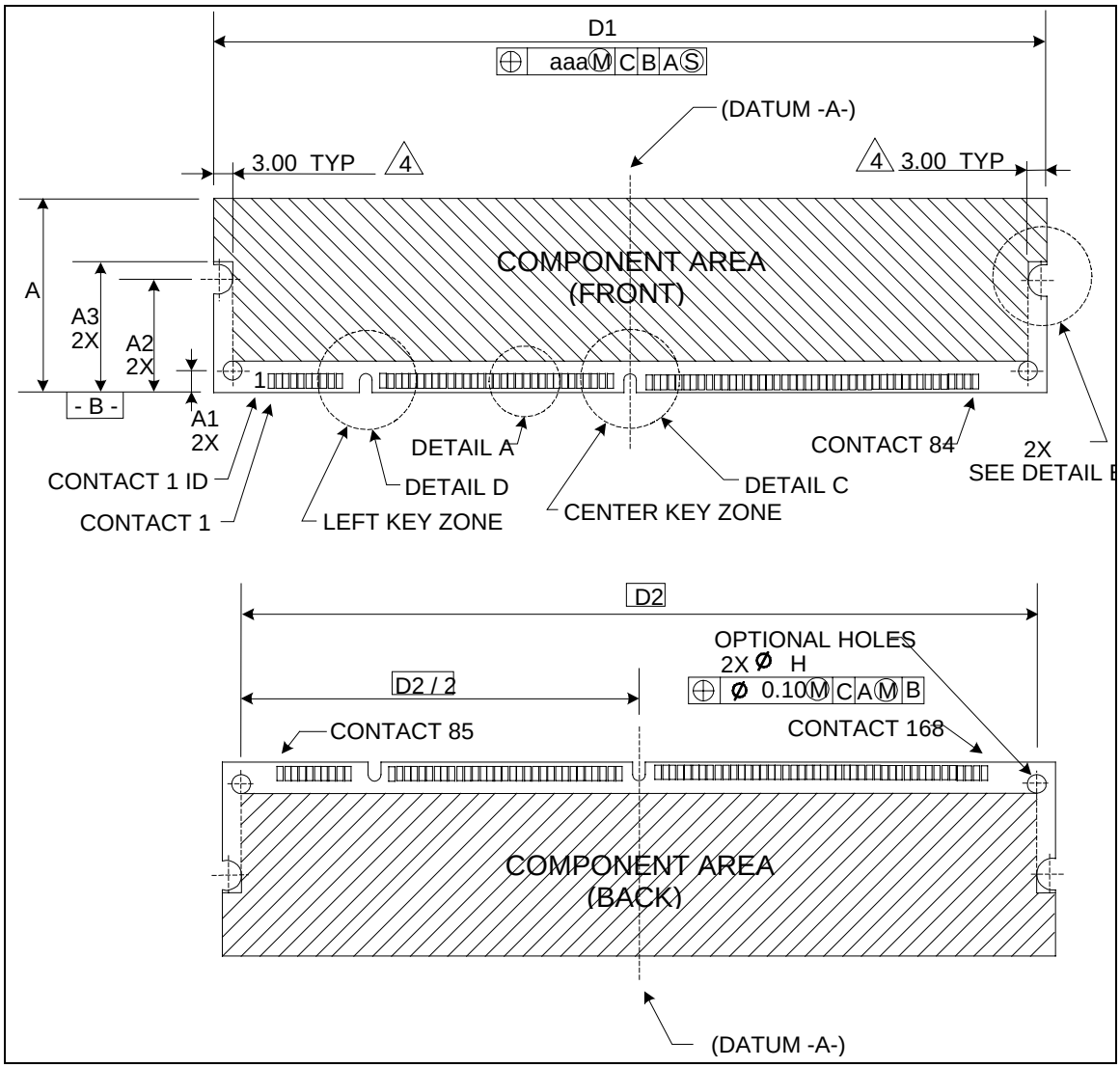



**Figure 1: DIMM Mechanical Drawing (1 of 5)**

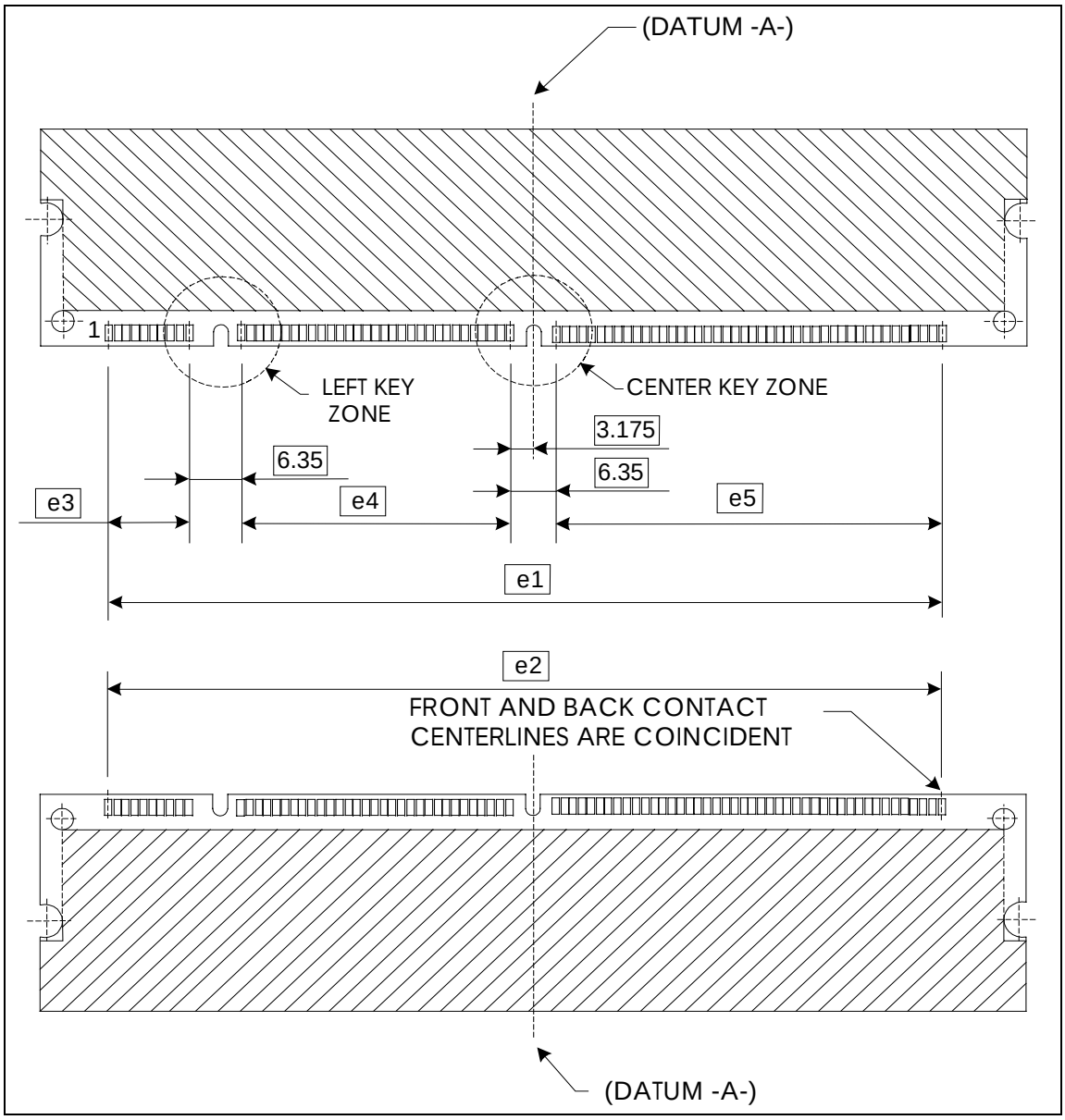



**Figure 2: DIMM Mechanical Drawing (2 of 5)**

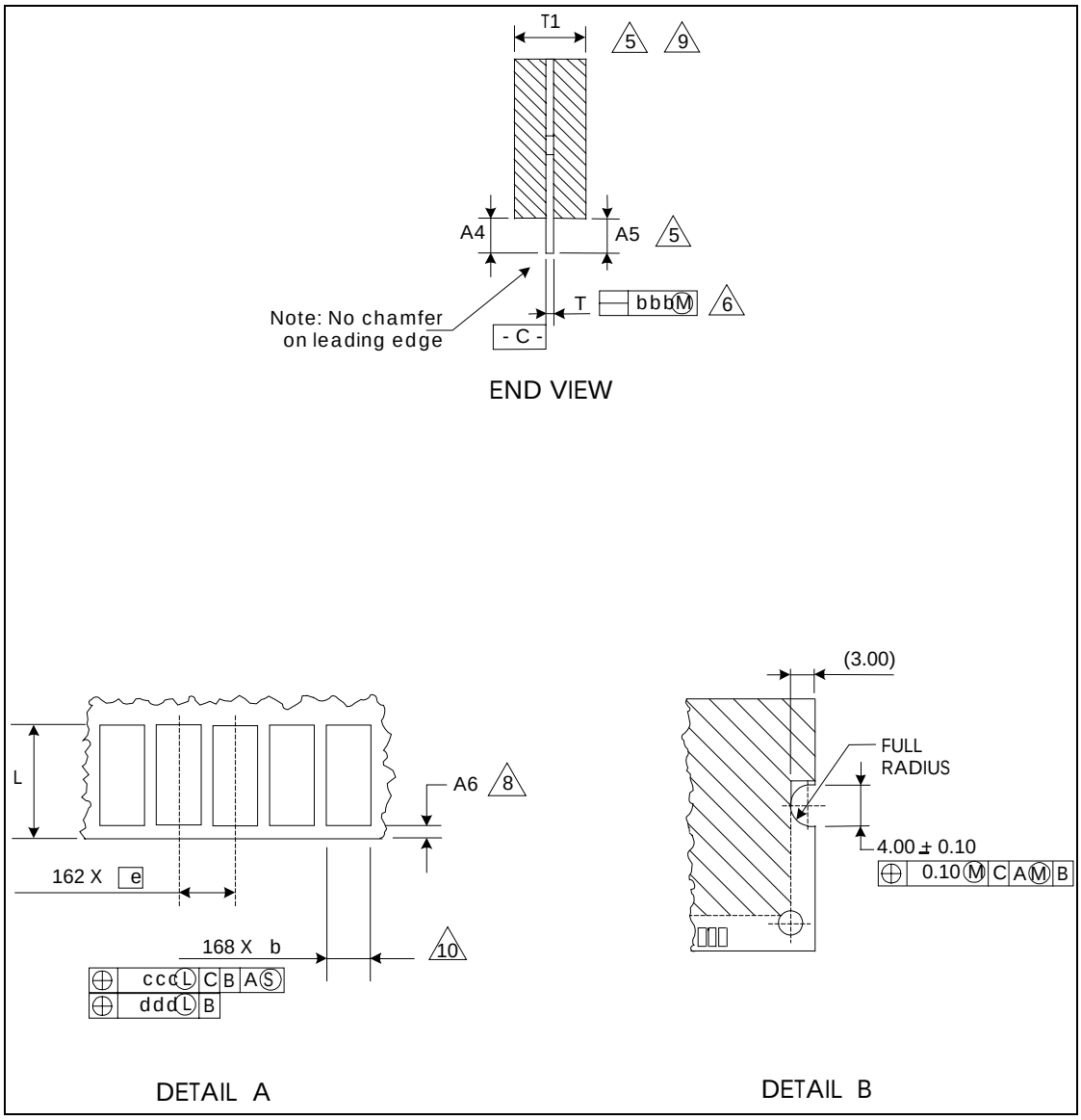



**Figure 3: DIMM Mechanical Drawing (3 of 5)**

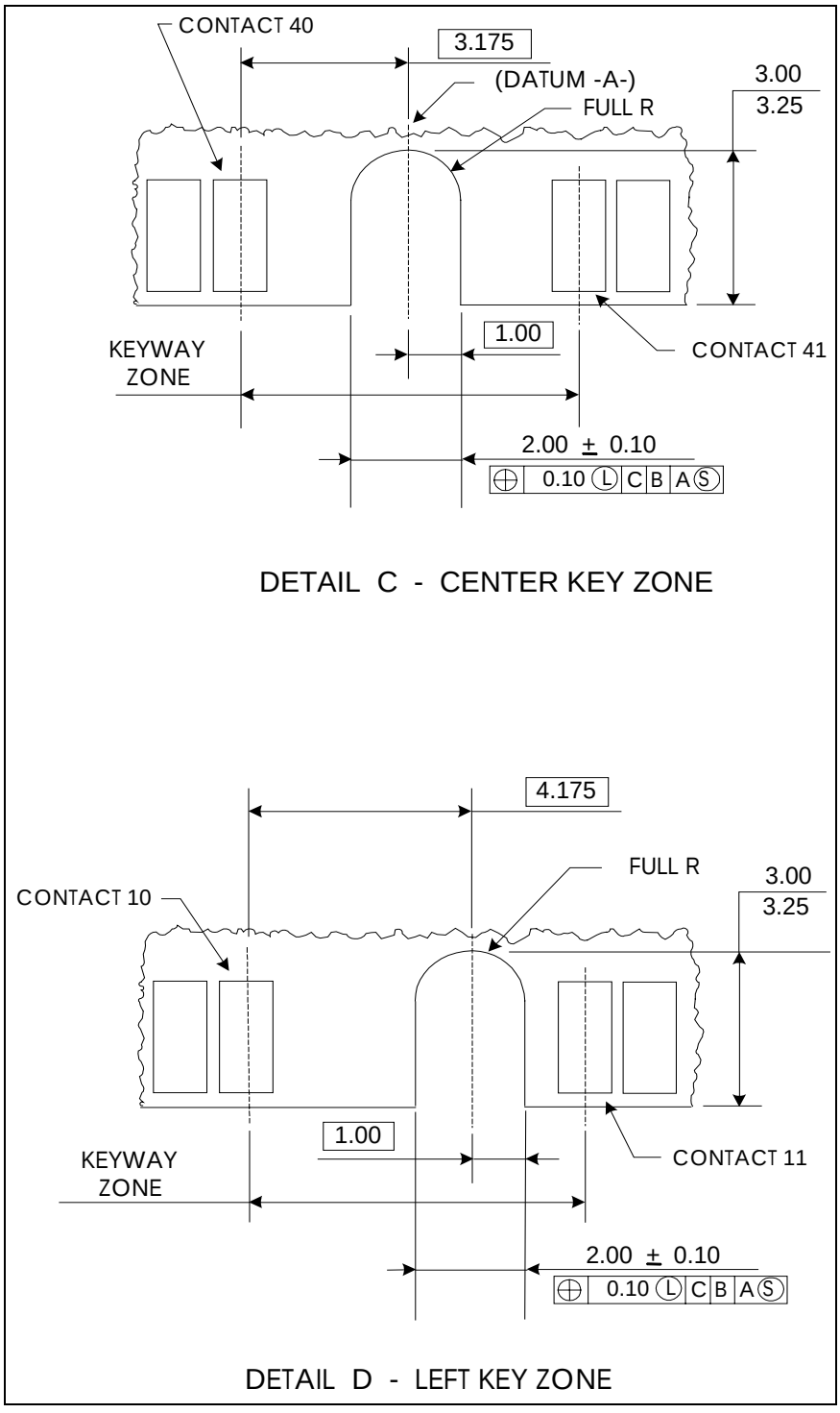



**Figure 4: DIMM Mechanical Drawing (4 of 5)**

NOTES

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1994.

2 TOLERANCES ON ALL DIMENSIONS +/- 0.13 UNLESS OTHERWISE SPECIFIED.

3 ALL DIMENSIONS ARE IN MILLIMETERS.

4 3.00 mm TYPICAL APPLIES TO BOTH 4.00 mm WIDE NOTCH LENGTH AND COMPONENT KEEPOUT AREA.

5 DIMENSION APPLICABLE WHEN COMPONENTS MOUNTED ON BOTH SIDES.

6 CARD THICKNESS APPLIES ACROSS THE CONTACTS AND INCLUDES PLATING AND/OR METALIZATION. STRAIGHTNESS CALLOUT APPLIES TO ZONE DEFINED BY A4, A5, AND D1.

7 N IS THE TOTAL NUMBER OF CIRCUIT CONTACTS (PINS, LEADS, TABS OR PADS).

8 LEADING EDGE OF CONTACT ZONE SHALL BE FREE OF BURRS AND EXTERNAL TIE BARS.

9 THE MAXIMUM THICKNESS OVERALL SHALL NOT EXCEED 8.13 mm.

APPLICATION NOTES:

10 PLATING FOR CONTACT PADS: GOLD PLATING 0.75 MICROMETER MINIMUM OVER NI PLATING 2 MICROMETERS MINIMUM.

11 FOR OPTIMUM PERFORMANCE, IT IS RECOMMENDED THAT THE TIEBAR BE OFFSET FROM THE CENTERLINE OF THE PAD. ALSO, THE TIEBAR MAY BE AN INTERNAL LAYER, SO THE REMNANT CANNOT CAUSE CONTACT DAMAGE.

**Figure 5: DIMM Mechanical Drawing (5 of 5)**

# 7 Module Pins

The following table provides the 168-pin 72-bit registered DIMM module connector pinout. Note that the eight error detection and correction bits CB(0:7) are actually NC for the 64-bit pinout.

**Table 5: Registered DIMM Module Pinout**

| Pin# | Signal Name | Pin# | Signal Name | Pin# | Signal Name | Pin# | Signal Name |
|---|---|---|---|---|---|---|---|
| 1 | Vss | 43 | Vss | 85 | Vss | 127 | Vss |
| 2 | DQ0 | 44 | DU | 86 | DQ32 | 128 | CKE0 |
| 3 | DQ1 | 45 | /S2 | 87 | DQ33 | 129 | /S3 |
| 4 | DQ2 | 46 | DQMB2 | 88 | DQ34 | 130 | DQMB6 |
| 5 | DQ3 | 47 | DQMB3 | 89 | DQ35 | 131 | DQMB7 |
| 6 | Vcc | 48 | DU | 90 | Vcc | 132 | A13 |
| 7 | DQ4 | 49 | Vcc | 91 | DQ36 | 133 | Vcc |
| 8 | DQ5 | 50 | NC | 92 | DQ37 | 134 | NC |
| 9 | DQ6 | 51 | NC | 93 | DQ38 | 135 | NC |
| 10 | DQ7 | 52 | CB2 | 94 | DQ39 | 136 | CB6 |
| 11 | DQ8 | 53 | CB3 | 95 | DQ40 | 137 | CB7 |
| 12 | Vss | 54 | Vss | 96 | Vss | 138 | Vss |
| 13 | DQ9 | 55 | DQ16 | 97 | DQ41 | 139 | DQ48 |
| 14 | DQ10 | 56 | DQ17 | 98 | DQ42 | 140 | DQ49 |
| 15 | DQ11 | 57 | DQ18 | 99 | DQ43 | 141 | DQ50 |
| 16 | DQ12 | 58 | DQ19 | 100 | DQ44 | 142 | DQ51 |
| 17 | DQ13 | 59 | Vcc | 101 | DQ45 | 143 | Vcc |
| 18 | Vcc | 60 | DQ20 | 102 | Vcc | 144 | DQ52 |
| 19 | DQ14 | 61 | NC | 103 | DQ46 | 145 | NC |
| 20 | DQ15 | 62 | Vref, NC | 104 | DQ47 | 146 | Vref, NC |
| 21 | CB0 | 63 | CKE1 | 105 | CB4 | 147 | REGE |
| 22 | CB1 | 64 | Vss | 106 | CB5 | 148 | Vss |
| 23 | Vss | 65 | DQ21 | 107 | Vss | 149 | DQ53 |
| 24 | NC | 66 | DQ22 | 108 | NC | 150 | DQ54 |
| 25 | NC | 67 | DQ23 | 109 | NC | 151 | DQ55 |
| 26 | Vcc | 68 | Vss | 110 | Vcc | 152 | Vss |
| 27 | /WE | 69 | DQ24 | 111 | /CAS | 153 | DQ56 |
| 28 | DQMB0 | 70 | DQ25 | 112 | DQMB4 | 154 | DQ57 |
| 29 | DQMB1 | 71 | DQ26 | 113 | DQMB5 | 155 | DQ58 |
| 30 | /S0 | 72 | DQ27 | 114 | /S1 | 156 | DQ59 |
| 31 | DU | 73 | Vcc | 115 | /RAS | 157 | Vcc |
| 32 | Vss | 74 | DQ28 | 116 | Vss | 158 | DQ60 |
| 33 | A0 | 75 | DQ29 | 117 | A1 | 159 | DQ61 |
| 34 | A2 | 76 | DQ30 | 118 | A3 | 160 | DQ62 |
| 35 | A4 | 77 | DQ31 | 119 | A5 | 161 | DQ63 |
| 36 | A6 | 78 | Vss | 120 | A7 | 162 | Vss |
| 37 | A8 | 79 | CK2 | 121 | A9 | 163 | CK3 |
| 38 | A10 (AP) | 80 | NC | 122 | BA0 | 164 | NC |
| 39 | BA1 | 81 | WP | 123 | A11 | 165 | SA0 |
| 40 | Vcc | 82 | SDA | 124 | Vcc | 166 | SA1 |
| 41 | Vcc | 83 | SCL | 125 | CK1 | 167 | SA2 |
| 42 | CK0 | 84 | Vcc | 126 | A12 | 168 | Vcc |

**Note: NC = Not Connected; DU = Don't Use**

Note: DIMM signals BA0, BA1, A12 and above may be connected to the A12, A13, A14 address lines and above respectively on the motherboard.

## Table 6: Pin Descriptions

| Pin Name | Desription | Pin Name | Description |
|---|---|---|---|
| CK(0:3) | Clock Inputs | DQ(0:63) | Data Input/Output |
| CKE(0:1) | Clock Enables | CB(0:7) | ECC Data Input/Output |
| /RAS | Row Address Strobe | DQMB(0:7) | Data Mask |
| /CAS | Column Address Strobe | Vcc | Power (3.3V) |
| /WE | Write Enable | Vss | Ground |
| /S(0:3) | Chip Selects | NC | No Connect |
| A(0:9,11:13) | Address Inputs | SCL | Serial Presence Detect Clock Input |
| A10/AP | Address Input/Autoprecharge | SDA | Serial Presence Detect Data Input/Output |
| BA0-BA1 | SDRAM Bank Address | SA(0:2) | Serial Presence Detect Address Inputs |
| REGE | Register Enable | WP | Write Protect for SPD on DIMM |
| DU | Don't Use - leave as NC | NC | No Connect |

All pin functions are described in the "Intel PC SDRAM Specification" with the exception of REGE.

REGE is the Register Enable pin which permits the DIMM to operate in "buffered" mode (inputs re-driven asynchronously) and "registered" mode (signals re-driven to SDRAMs when clock rises, and held valid until next rising clock). **To conform to this design guide, REGE must select the operating mode according to the following function table.**

## Table 7: Registered / Buffered Mode Operation

| REGE Input | DIMM Mode |
|---|---|
| Low | Buffered [1] |
| High | Registered |

1 Note: All references to Buffered mode in this document are for operation at 66.67 MHz ( 15 nS period).

# 8 SDRAM DIMM Block Diagrams

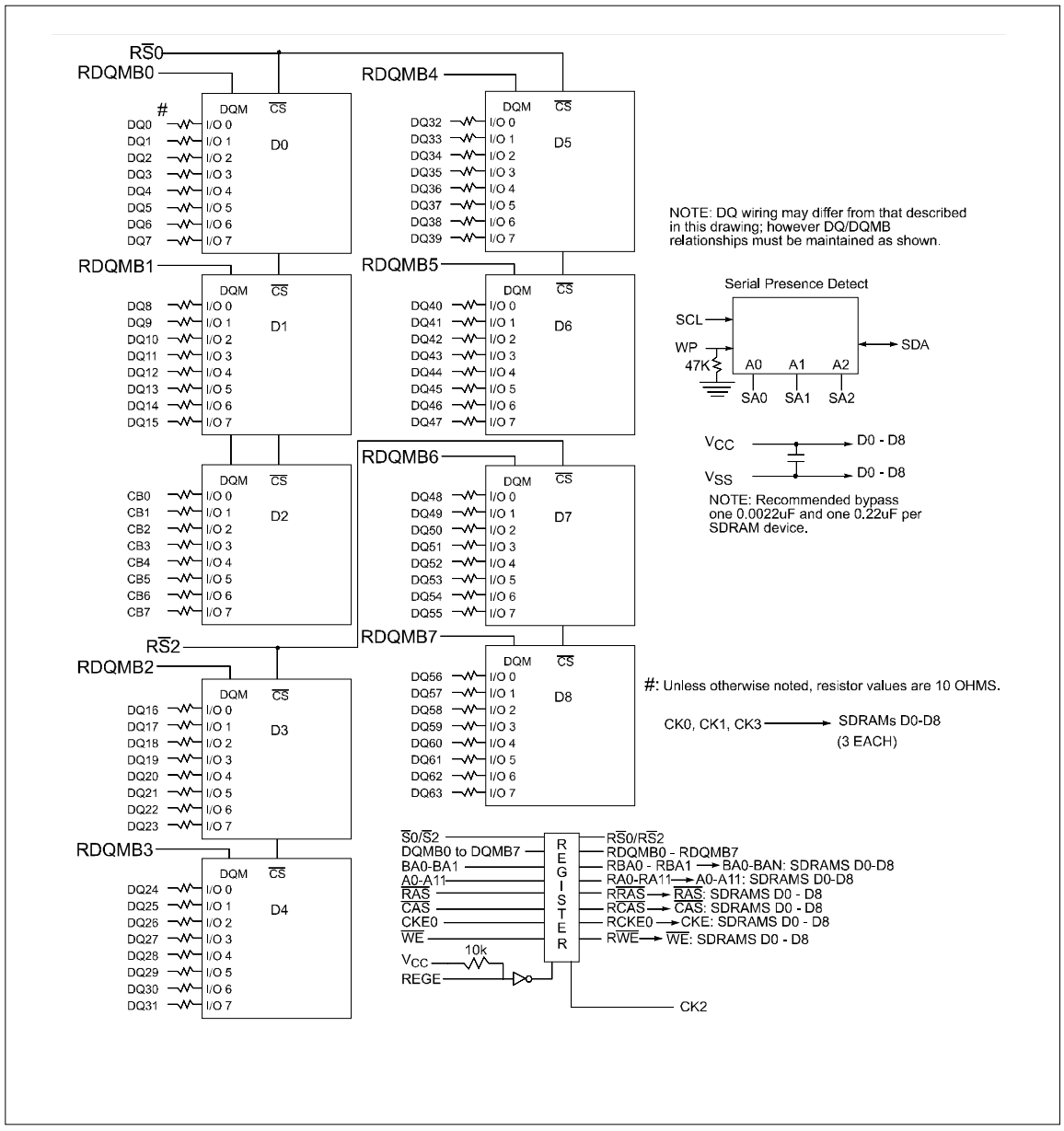



**Figure 6: 64MByte 72-Bit ECC SDRAM DIMM Block Diagram (1 row x8 SDRAMs)**

**Non-PLL Implementation**

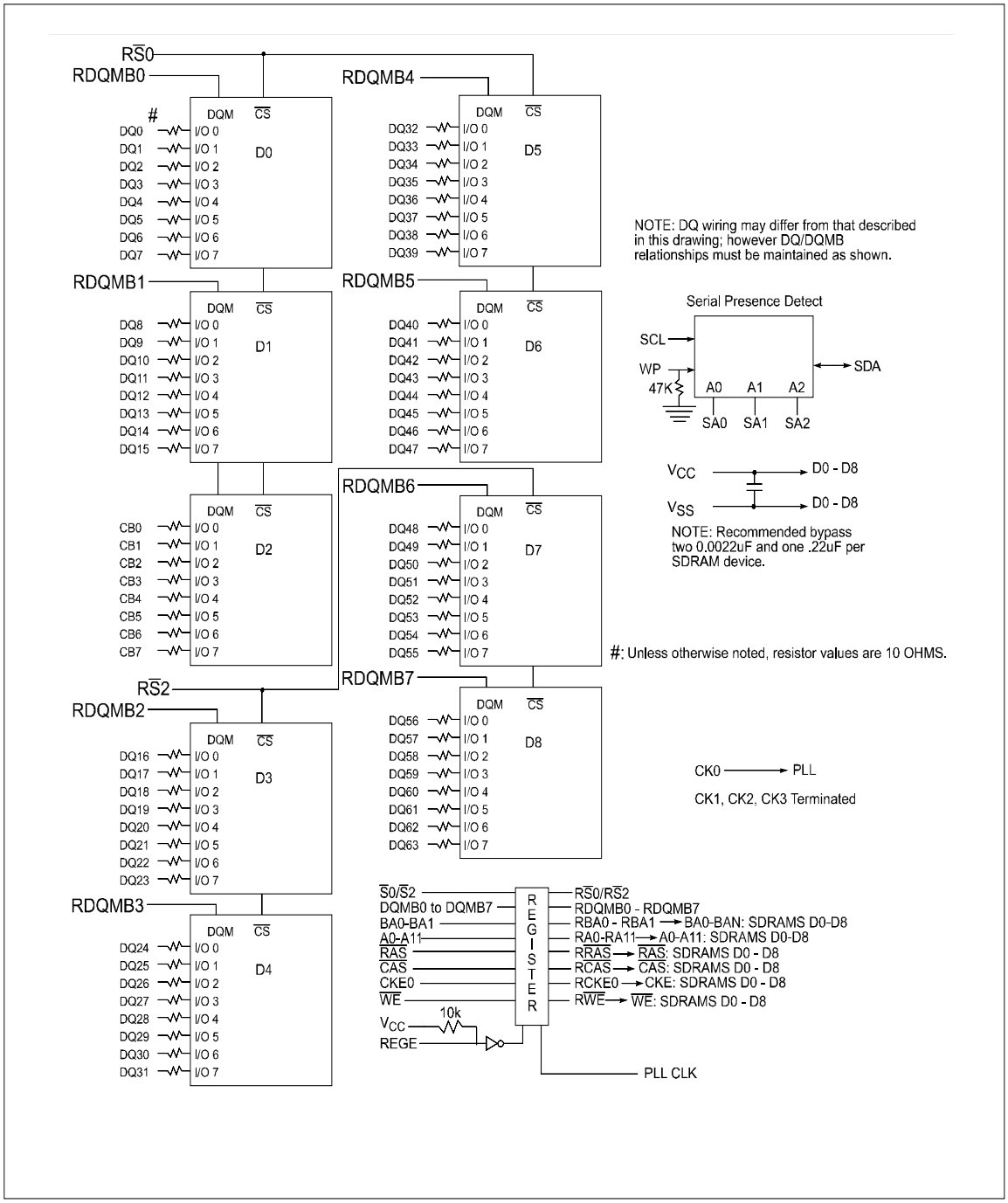



**Figure 7: 64MByte 72-Bit ECC SDRAM DIMM Block Diagram (1 row x8 SDRAMs)**

**PLL Implementation**

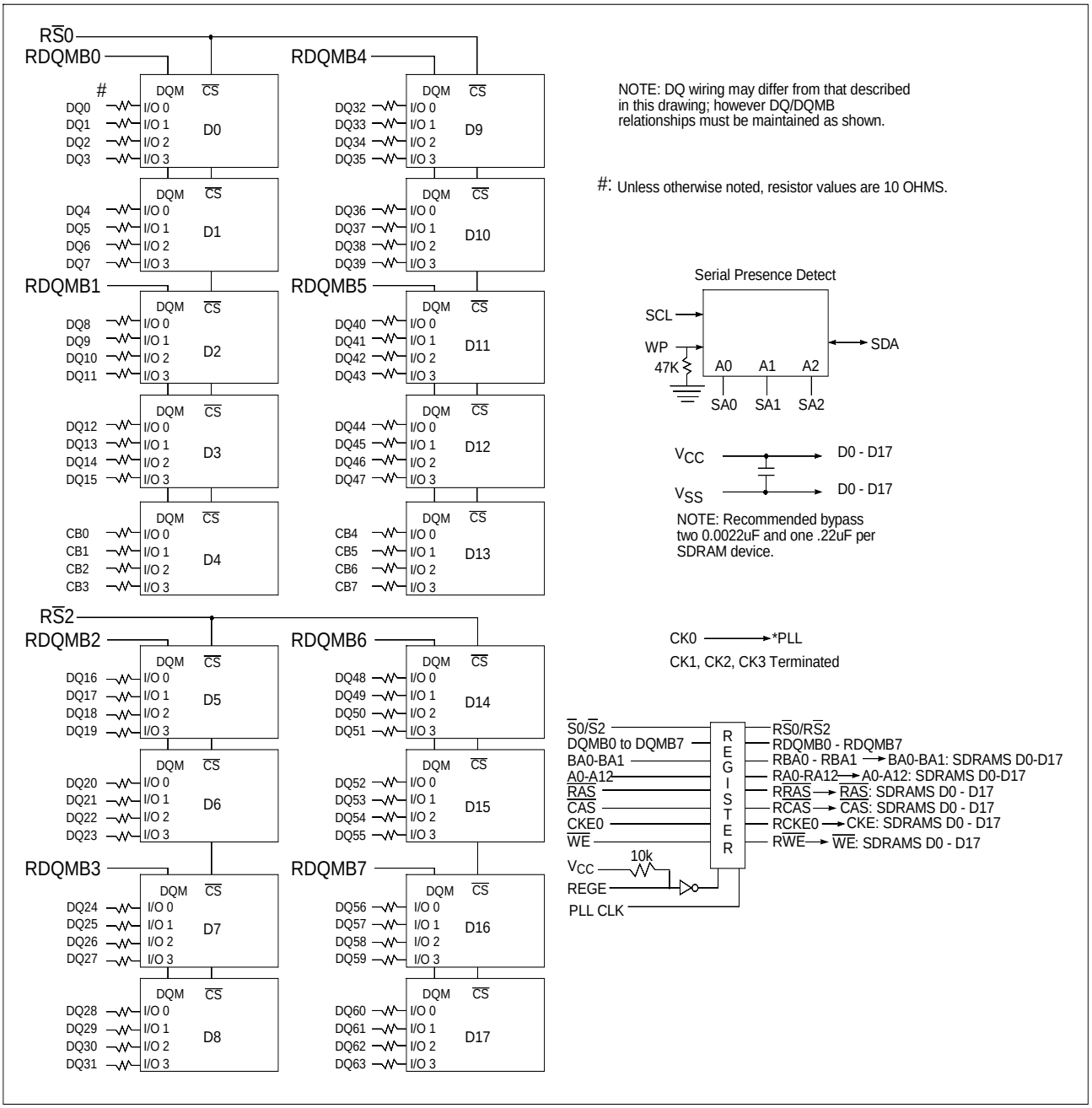



**Figure 8: 72-Bit ECC Unstacked SDRAM DIMM Block Diagram (1 row x4 SDRAMs)**

128MB using 16Mx4 (64Mbit) SDRAMs
256MB using 32Mx4 (128Mbit) SDRAMs
512MB using 64Mx4 (256Mbit) SDRAMs

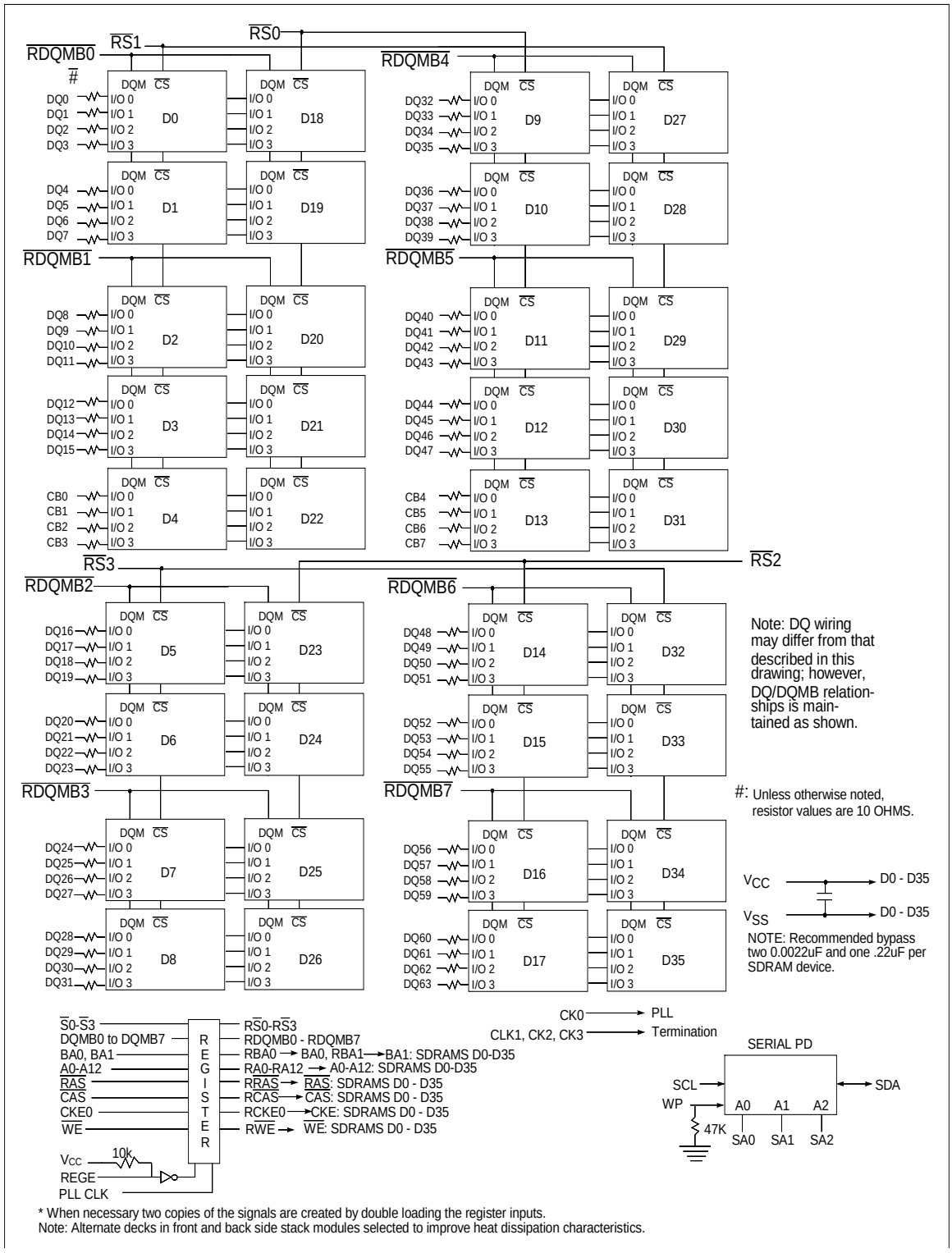



**Figure 9: 72-Bit ECC Stacked SDRAM DIMM Block Diagram (2 rows x4 SDRAMs)**

256MB using 16Mx4 (64Mbit) SDRAMs
512MB using 32Mx4 (128Mbit) SDRAMs
1GB using 64Mx4 (256Mbit) SDRAMs

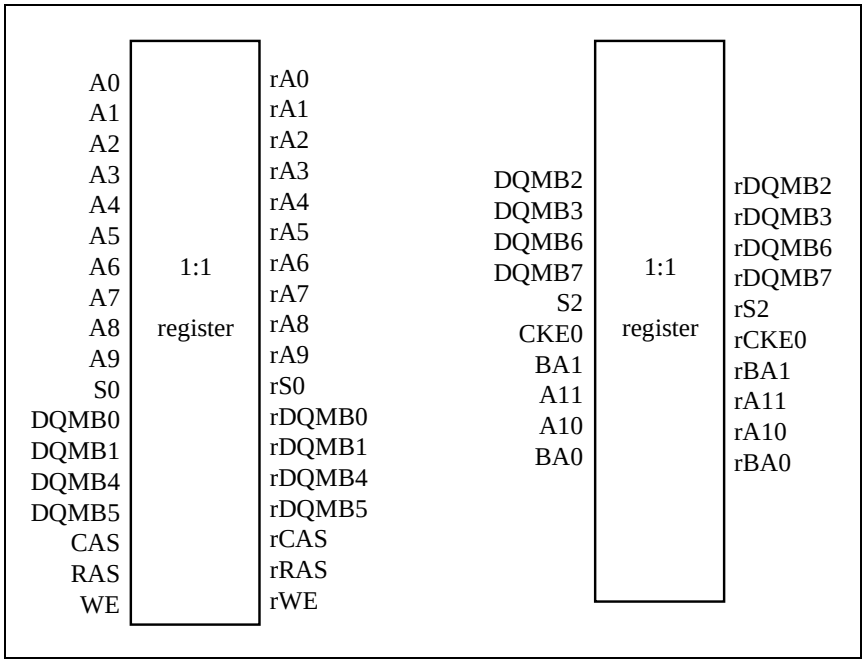



**Figure 10: Register Wiring on 64MByte DIMMs**

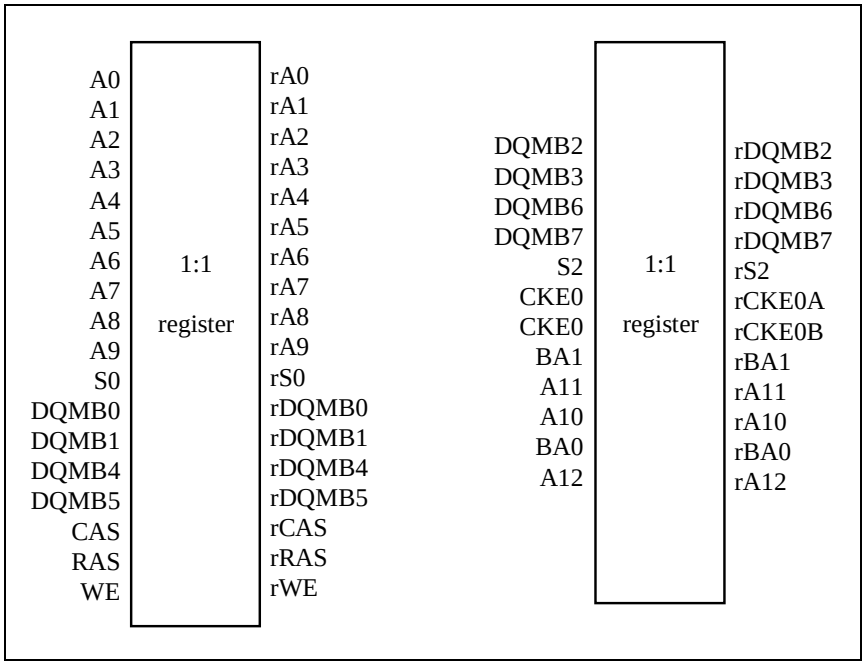



**Figure 11: Register Wiring for DIMM using 18 SDRAMs**

**(128MB, 256MB, 512MB)**

Note: A12 is used for 256Mbit SDRAMs only.

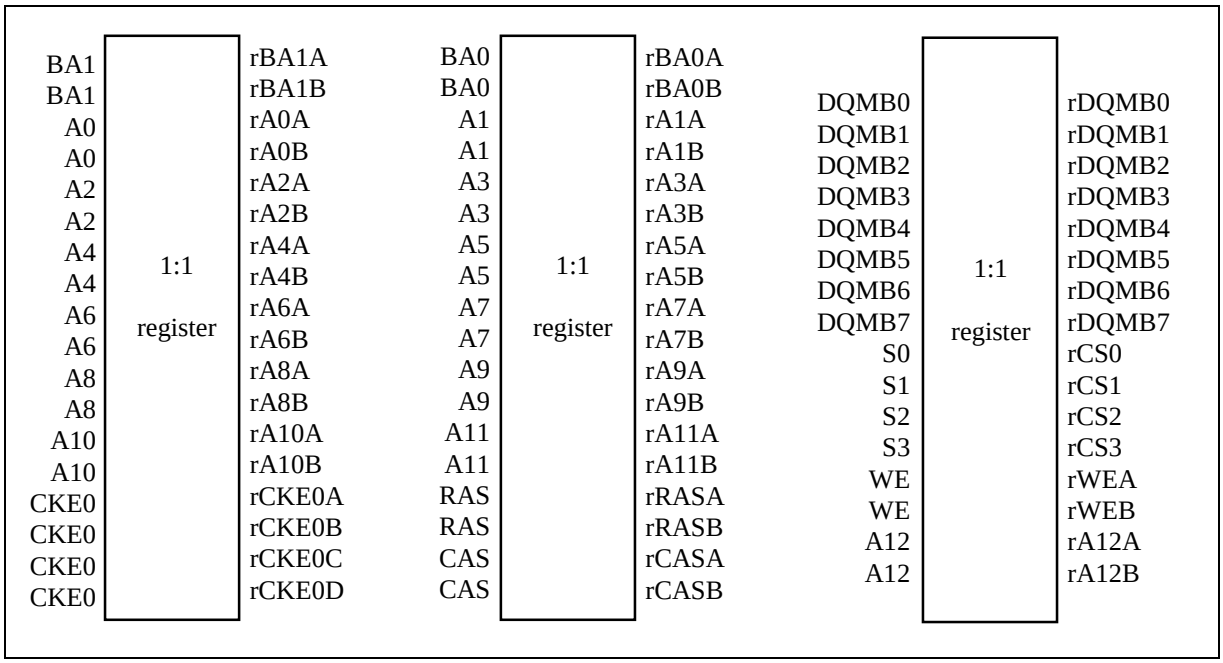



**Figure 12: Register Wiring for stacked DIMM using 36 SDRAMs**

**(256MB, 512MB & 1GB)**

**Note**: A12 is used for 256Mbit SDRAMs only.

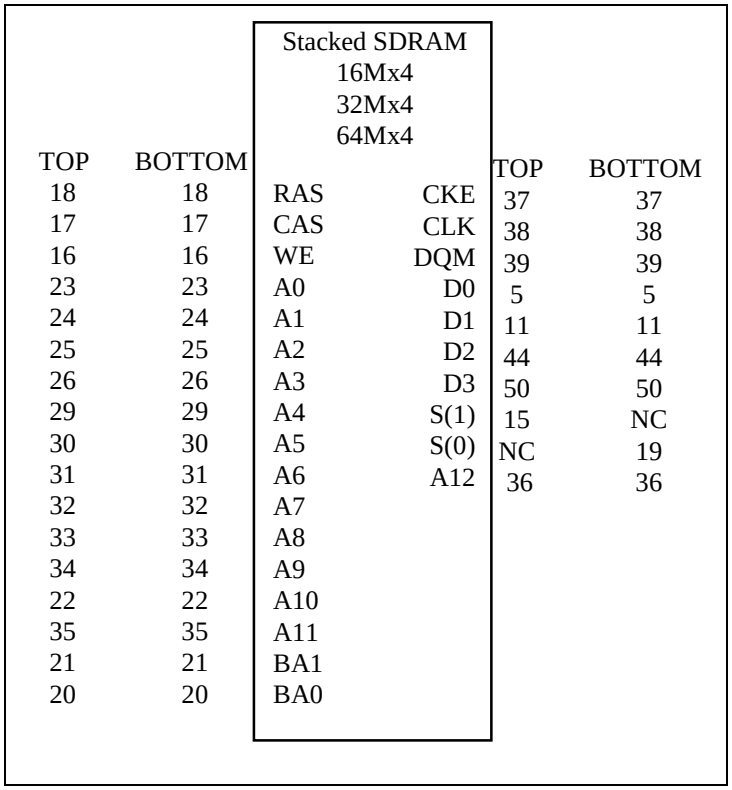


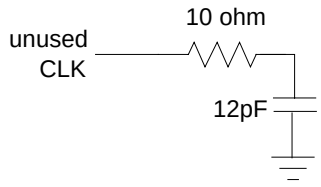

**Figure 13: Stacked SDRAM Component Pinout**

## Clock Loading Table:

| DIMM config | # of Banks on DIMM | Total # of SDRAMs | CLK Loading | | | |
|---|---|---|---|---|---|---|
| | | | CK0 | CK1 | CK2 | CK3 |
| 64MB wo/PLL | 1 | 9 | SDRAM (3x) | SDRAM (3x) | Reg. (2x) | SDRAM (3x) |
| 64MB w/PLL | 1 | 9 | PLL | * | * | * |
| unstacked DIMM | 1 | 18 | PLL | * | * | * |
| stacked DIMM | 2 | 36 | PLL | * | * | * |

* Use termination R/C

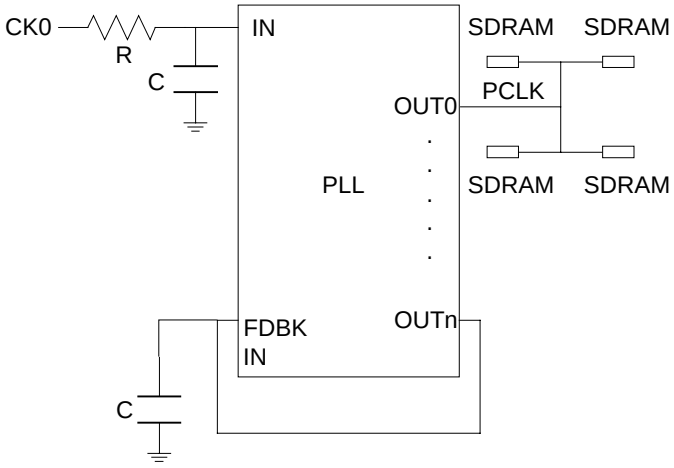
## Termination R/C for CK signals not connected to SDRAMs:




NOTES:
1) PLL outputs (PCLK) must be wired to assure tracking within +/-50ps at the load (SDRAM, register or padding capacitor).

2) The clock skew of the non-PLL DIMM input clocks must be less than 500 ps as measured at the SDRAM clock inputs. (This is a system level requirement added for clarification).

## Clock Net Wiring (CK0):




NOTES:
1) Only one PLL output is shown. Any additional PLL outputs will be wired in a similar manner.

2) Max of 4 SDRAM loads should be placed on each PLL output. If less than 4 loads - adjust line lengths to compensate for lighter loading.

**Figure 14: Clock Loading Table & Wiring Diagram**

# 9 DIMM Post-Register Timing

## 9.1 Registered Mode

The post register timing in the registered mode configuration is very critical. As an example, the timing analysis for the unstacked DIMM is shown below. This is an example only, and is not to be used for all DIMMs:

**Table 8: Example of Registered Mode Timing**

| Property | Time (ns) Set-up | | Property | Time (ns) Hold |
|---|---|---|---|---|
| tco.REG.max | 3.00 | | tco.REG.min | 1.50 |
| tflight.max | 3.43 | | tflight.min | 2.66 |
| tsso.brd.max | 0.30 | | tsso.brd.min | 0.00 |
| Tskew | 0.35 | | tskew | -.35 |
| Tjitter | 0.30 | | tjitter | NA |
| tsu.SDRAM | 2.00 | | thold.SDRAM | -1.00 |
| Total | 9.38 | | Total | 2.81 |
| Period | 10.00 | | Period | NA |
| Margin | 0.62 | | Margin | 2.81 |
| tskew.behind | 0.20 | | tskew.behind | -.30 |
| **Margin** | 0.82 | | **Margin** | 2.51 |

Tco.REG.max: The maximum time for the signal to exit the register. This is measured into a 0pF load.
Tflight.max: The maximum time for the signal to propagate from the register to the SDRAM.
Tsso.brd.max: The time the flight time is extended due to simultaneous switching outputs and crosstalk from other signals.
Tskew: The skew of the input clocks to the register and the SDRAM (PLL skew + trace skew)
Tjitter: The jitter of the input clocks to the register and the SDRAM (PLL jitter + PLL SSC induced skew).
Tsu.DRAM: The setup time required for the SDRAM inputs.
Tskew.behind: The input clocks to the registers are purposely skewed to aid in the setup time of the signals into the SDRAM (250 ps +/- 50 ps).

Tco.REG.min: The minimum time for the signal to exit the register. This is measured into a 0pF load.
Tflight.min: The minimum time for the signal to propagate from the register to the SDRAM.
Thold.DRAM: The hold time required for the SDRAM inputs.

## 9.2 Buffered Mode

The Table below shows the post register timing analysis for the unstacked DIMM in buffered mode. This is an example only, and is not to be used for all DIMMs.

**Table 9: Example of Buffered Mode Timing**

| Property | Time (ns) Set-up | | Property | Time (ns) Hold |
|---|---|---|---|---|
| tpd.BUF.max | 1.96 | | tpd.BUF.min | 0.91 |
| tflight.max | 3.43 | | tflight.min | 2.66 |
| tsso.brd.max | 0.30 | | tsso.brd.min | 0.0 |
| tsu.SDRAM | 2.00 | | thold.SDRAM | -1.00 |
| Total | 7.69 | | Total | 2.57 |
| Period | 15.00 | | Period | NA |
| Margin | 7.31 | | Margin | 2.57 |
| | | | | |

Tpd.BUF.max: The maximum time for the signal to exit the register with REGE in a low state. This is measured into a 0pF load.
Tflight.max: The maximum time for the signal to propagate from the register to the SDRAM.
Tsso.brd.max: The time the flight time is extended due to simultaneous switching outputs and crosstalk from other signals.
Tsu.DRAM: The setup time required for the SDRAM inputs.
Tpd.BUF.min: The minimum time for the signal to exit the register with REGE in a low state. This is measured into a 0pF load.
Tflight.min: The minimum time for the signal to propagate from the register to the SDRAM.
Thold.DRAM: The hold time required for the SDRAM inputs.

Note: The margin shown for the buffered mode DIMM is derived from post register timing only. For a complete system level timing analysis the designer must add/subtract to/from this margin other parameters such as, system to DIMM flight time, clock skew, clock jitter, external register clock to output delay, etc.

# 10 DIMM PCB Layout and Signal Routing

## 10.1 Printed Circuit Board

The DIMM printed circuit board should be a six layer design using glass epoxy material. PCBs must have both a full ground plane layer and full power plane layer. The PCB stackup must be designed to achieve the following calculated board characteristics (using either 4 or 6 mil wide traces):

**Table 10: PCB Calculated Parameters**

| Parameter | Min | Max |
|---|---|---|
| Trace velocity: $S_0$ [ns/ft] (outer layers) | 1.6 | 2.2 |
| Trace velocity: $S_0$ [ns/ft] (inner layers) | 2.0 | 2.2 |
| Trace impedance: $Z_0$ [Ω] (all layers) | 58.5 | 71.5 |

**Required Dielectric: 4.2 to 4.8**

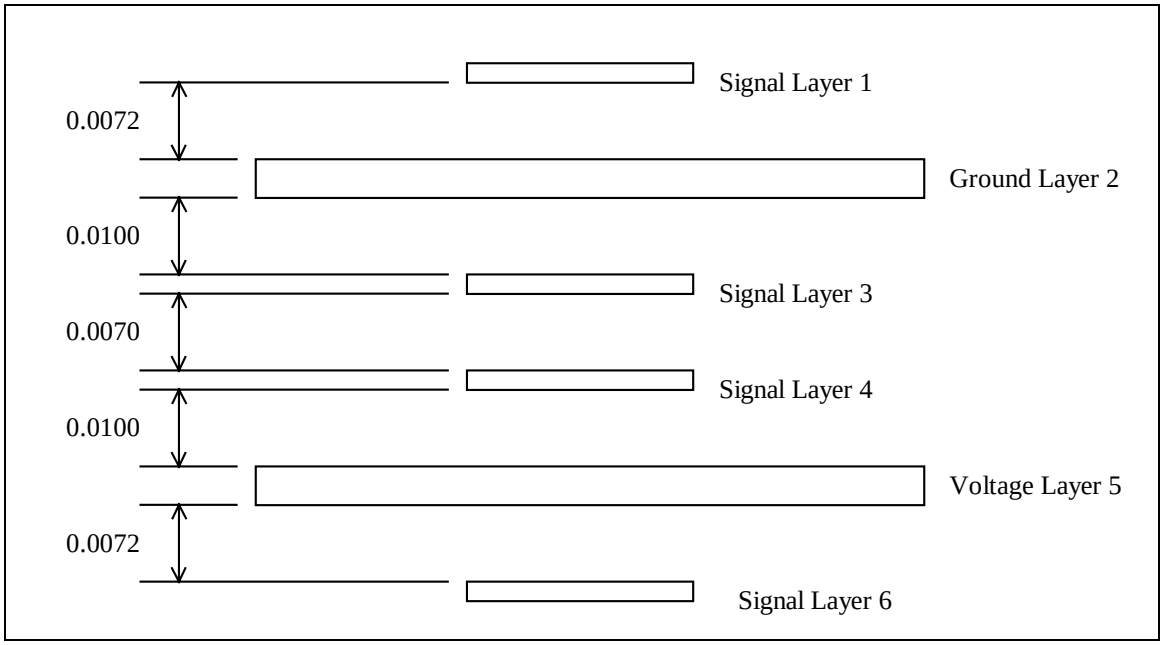



**Figure 15: Example 6-Layer Stackup for 6 mil Traces**

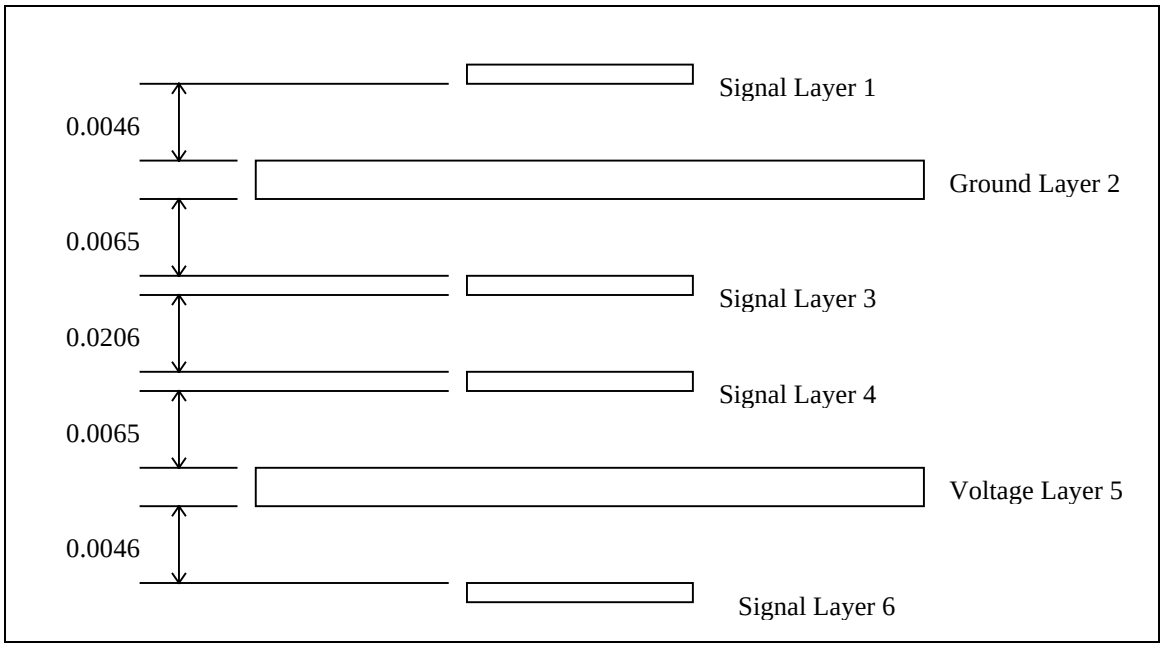



**Figure 16: Example 6-Layer Stackup for 4 mil Traces**

The PCB edge connector contacts shall be gold plated per Figure 5 note 10. Note: The PCB connector edge will not be chamfered.

## 10.2 DIMM PCB and final assembly labeling requirements

### 10.2.1 DIMM Naming Convention

In order to be able to visually identify the critical parameters of a given DIMM, the following naming convention will be used.

On component or sticker on DIMM (supplier option):

**PCX-abc-defR (**use minimum 8 point font)

Where X=Mhz
a = CL value
b = trcd value
c = trp value
d = tac value
e = spd rev #
f = Rev. 1.2 Conformance

The manufacturer's name and DIMM assembly part number shall also appear on the DIMM. All performance parametrics are referenced to the component.

Example: PC100-322-622R
is 100Mhz, CL=3, trcd=2, trp=2, tac=6, 2= spd rev 1.2, 2= Rev. 1.2 Conformance, R= registered DIMM

### 10.2.2 Printed Circuit Board Labeling

The printed circuit board is required to have the following labeling contained in etch or silkscreen:

1. Flammability indicator (see Safety - UL Rating). Also see the section 5.1 for UL Requirements.

## 10.3 Component Types and Placement

Components shall be of surface mount type, and will be mounted on both sides of the PCB. Components shall be positioned on the PCB to meet the min and max trace lengths required for SDRAM data signals. Bypass capacitors for SDRAM devices must be located as near as practical to the device power pins. In two bank SDRAM designs, location of the second SDRAM bank devices will be stacked on top of the first bank SDRAM devices.

The following diagram illustrates the one suggested placement for x4 (stacked) SDRAM devices. Exact spacing numbers are not provided, but are left up to the DIMM manufacturer to determine based on manufacturing constraints and signal routing constraints imposed by this design guide.

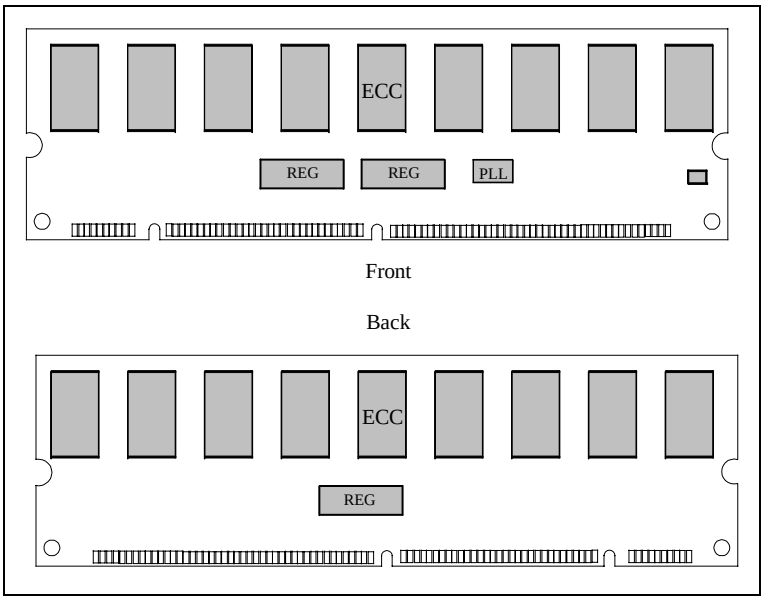



**Figure 17: Example 256MByte Component Placement**

## 10.4 Signal Groups

The SDRAM timing-critical signals have been categorized into seven groups. The signals are divided into groups whose members have identical loadings and routing topologies. The following table summarizes the signal groups by listing the signals contained in each. The following sections will describe routing restrictions associated with each signal group.

**Table 11: Signal Topology Categories**

| Signal Group | Signals In Group |
|---|---|
| Clock | CK [3:0] |
| | |
| Data | DQ [63:0] |
| | CB [7:0] |
| | |
| Data Mask | DQMB [0,2-4,6,7] |
| | |
| Data Mask | DQMB [1,5] |
| | |
| Chip Select | S# [3:0] |
| | |
| Clock Enable | CKE# [0] |
| | |
| Address/Control | A [12:0] |
| | BA [0,1] |
| | RAS# |
| | CAS# |
| | WE# |
| | |

## 10.5 Signal Topology and Length Restrictions

In order to meet signal quality and setup/hold time requirements for the memory interface certain routing topologies and trace length requirements must be met. The signal topology requirements are shown pictorially in the following pages. Each topology diagram is accompanied by a trace length table that lists either the minimum and maximum lengths allowed for each trace segment or the min and max lengths for the entire net.

### 10.5.1 Routing Rules

**General Info:**

- The recommended trace width and spacing values for the Clock traces are 6 mil trace width and 12 mil minimum spacing between adjacent traces, or 4 mil trace width and 8 mil spacing.
- The recommended trace width and spacing values for signal traces ( except clocks ) are 6 mil trace width and 10 mil spacing between adjacent traces, or 4 mil trace width and 6 mil spacing.
- Clocks must be routed with at least 90% of the total trace length in the inner layers. Maximum parallel overlap between clocks and signals in layers 3 and 4 must be restricted to less than .250".
- No test points are required.

### 10.5.2 Topology Diagram Explanation and Examples

A reference design example is included in this document. The reference design is intended to provide an initial basis for a registered DIMM design. For any design, a full simulation of all signal integrity and timing is required to verify the functionality of the DIMM. The following topologies are a representation of the reference design, and are not meant to be inclusive for all solutions.

The routing topology diagrams in this section should be used to determine individual signal topologies on a DIMM for any supported configuration.

**The way that these diagrams should be read is the following:**

- Only the cylinders labeled with length designators represent actual physical trace segments. All other lines should be considered zero in length.

Please see the following page for an example of how to use the topology diagrams.

**** With the exception of the clock topologies, all references to 64MByte DIMM topologies refer to both the PLL and non-PLL versions of the DIMMs.**

**Example:** For an 256MByte, double-sided, ECC DIMM that uses 64Mbit 16Mx4 SDRAM devices, the resulting topology for Data, would be the following:

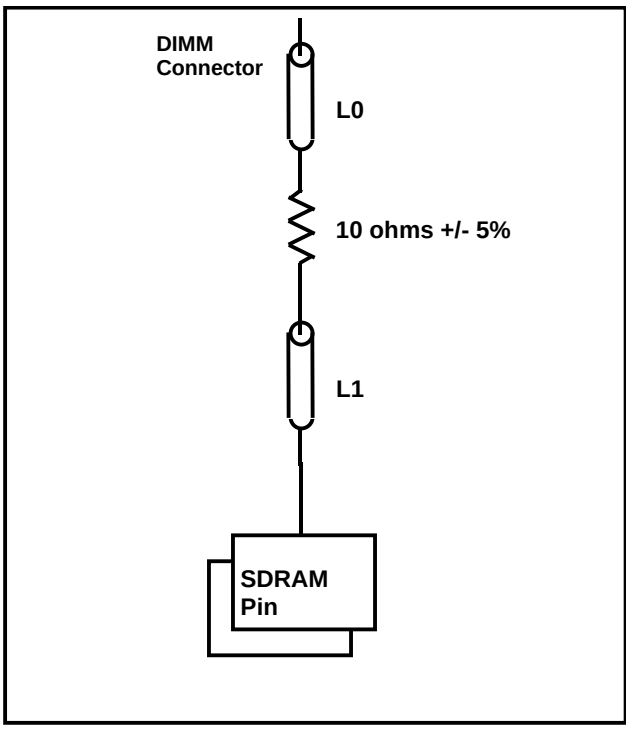



**Figure 18: Example Topology**

Once the topology has been determined, the permitted segment length ranges for that topology can be read from the table below each topology diagram. It is important to note that some configurations will require more than one topology diagram to account for different numbers of loads on copies of the same signal. For all of the topologies listed in the following pages, one load is defined as one SDRAM input.

### 10.5.3 Topology for Clock: CK[3:0]

Special attention must be given to the routing of the clock signals to ensure adequate signal quality, rise/fall time, minimum skew between DIMM clocks and predictable interface to the outside world (memory controller). The accompanying topology diagrams and Tables with trace length definitions and resistor and capacitor values are provided to this end. These guidelines must be used in conjunction with simulation of the final design to achieve optimum results.

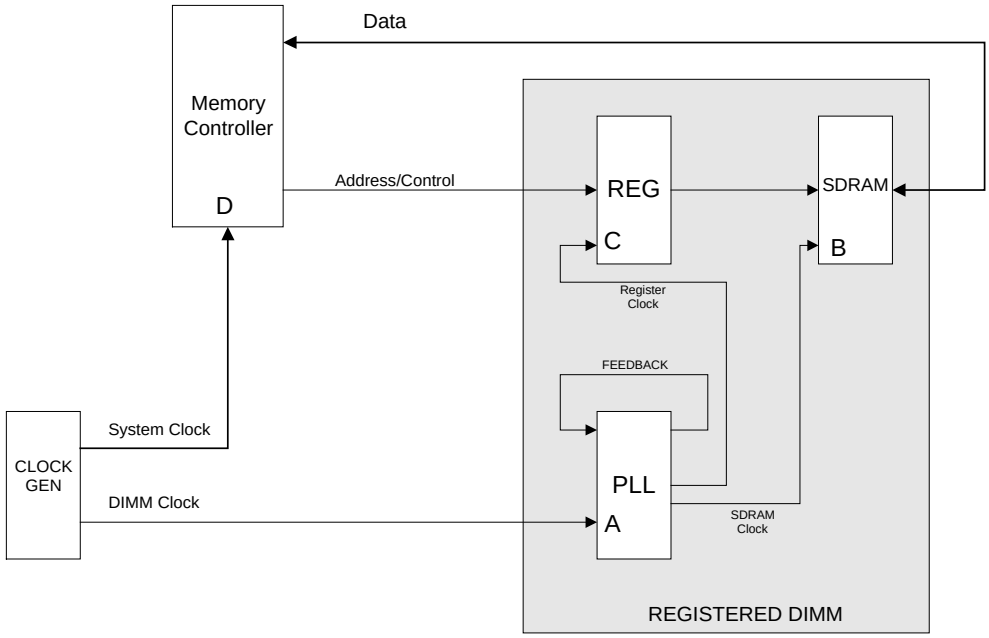
In DIMM versions which include the PLL, SDRAM clocks, register clocks, and external system clocks are referenced to the rising edge of the input clock to the PLL. The block and timing diagrams in Figure 19 show the points of reference and phase relationship of all pertinent clocks.

The SDRAM clocks are in phase with the rising edge of the input clock to the PLL; the register clocks have intentionally been skewed by 250 psec to allow more address and control signal setup time at the SDRAM. This decision was based on simulation results. The +/- 50 psec skew shown on the SDRAM and register clocks accounts for trace length and PWB variations. The phase relationship between the system clock and the input clock to the PLL is system dependent.

In systems which use the 440BX or 440GX memory controller, the system clock at the input of the memory controller lags the SDRAM clock by 2.14 +/- 0.41 nsec. This skew is required to maintain compatibility with the PC 100 unbuffered DIMM.

The PLL feedback loop capacitance (C3) is dependent on the PLL used, and should be chosen to minimize the PLL phase error. A nominal value of 12 pF is shown on Table 12.

The capacitance at the input of the PLL (C1) is chosen as 12 pF, to approximately match the clock loading on the PC 100 unbuffered DIMM and provide a uniform system load interface.



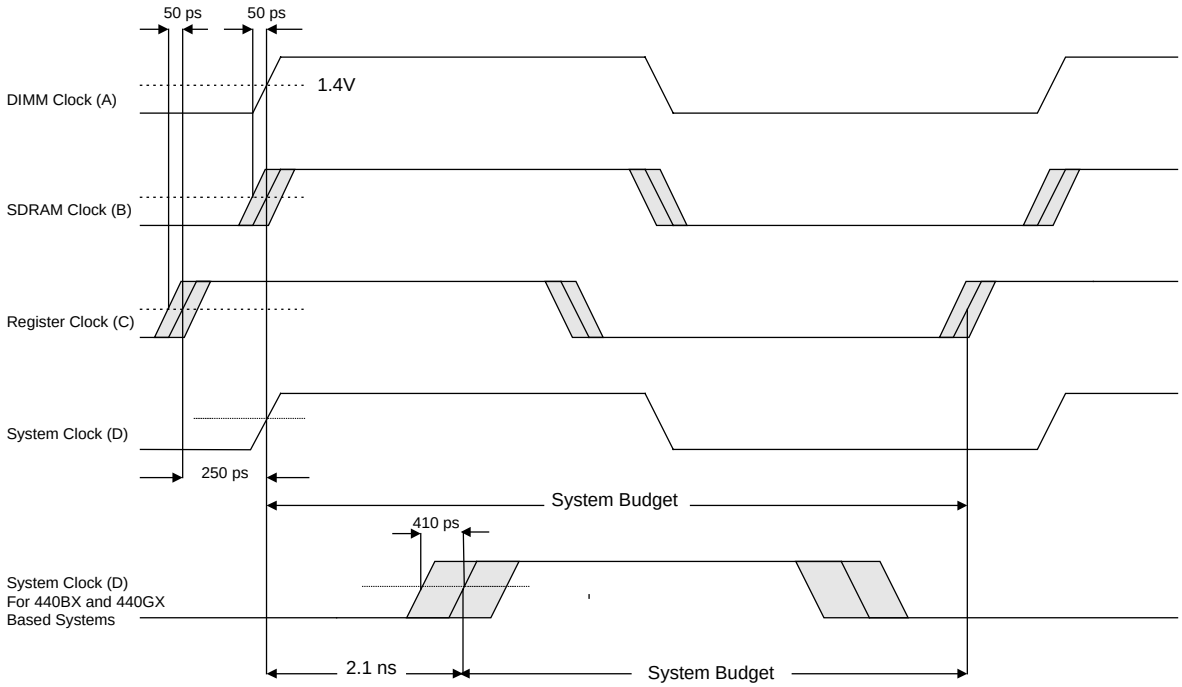




**Figure 19: DIMM clock reference and timing (not to scale)**

The following figure illustrates the recommended clock topologies, and the accompanying table lists required trace segment lengths and added capacitance values and tolerances.

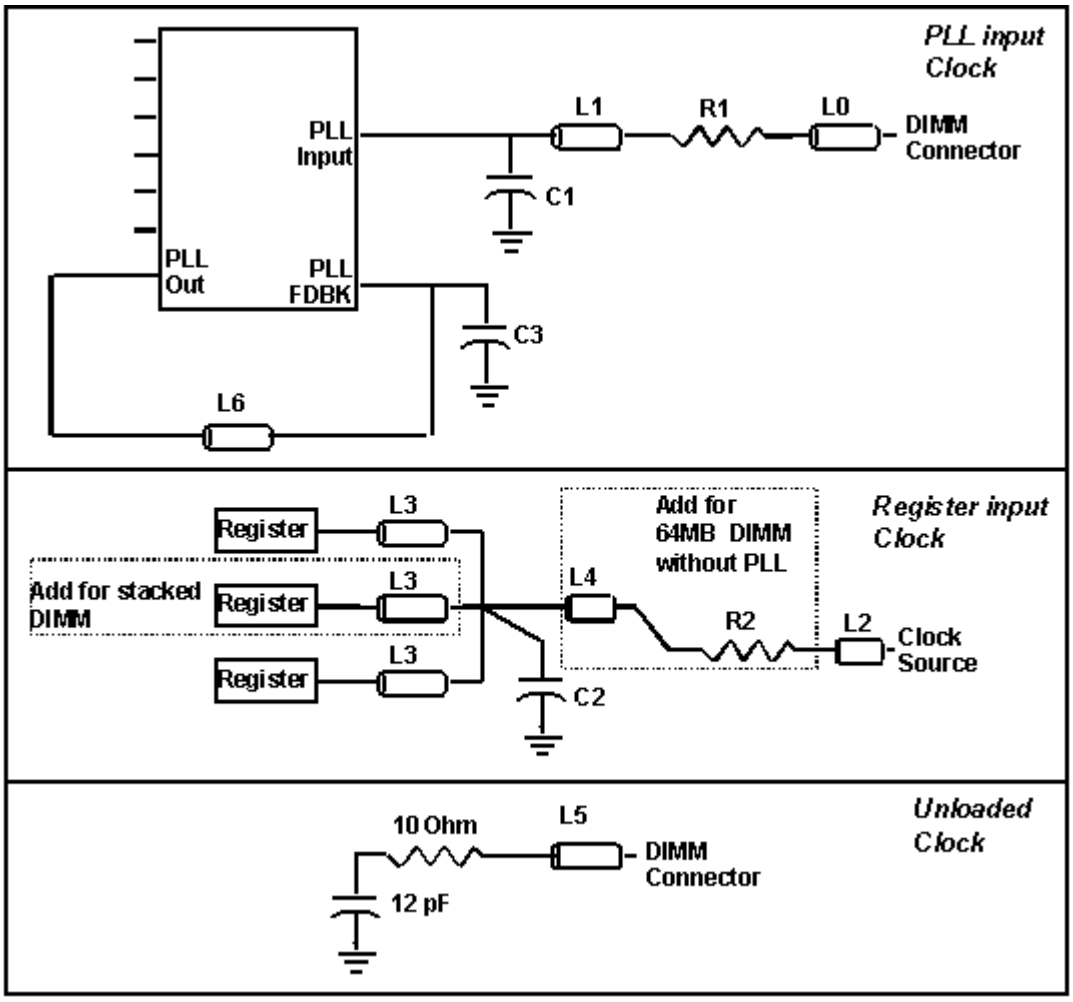



**Figure 20: Signal routing topologies for Clocks pre-PLL**

**Table 12: Trace Length and component value Table for DIMM connector to PLL Clock-in Topologies**

| DIMM Config | L0 | L1 | L2 | L3 | L4 | L5 | L6 | R1 ohms | R2 ohms | C1 pF | C2 pF | C3 pF |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 64MB* | 0.178 | 1.785 | 1.645 | 2.500 | NA | 0.150 | 3.000 | 10 | NA | 12 | NA | 12[3] |
| 64MB | NA | NA | 0.141 | 0.757 | 2.472 | NA | NA | NA | 25.5 | NA | 2.7 | NA |
| Unstacked DIMM using x4 SDRAMs | 0.286 | 2.514 | 1.311 | 0.381 | NA | 0.214 | 3.091 | 10 | NA | 12 | NA | 12[3] |
| Stacked DIMM | 0.126 | 2.637 | 1.096 | 0.850 | NA | 0.145 | 3.102 | 10 | NA | 12 | NA | 12[3] |

1 All distances are given in inches and must be kept within a tolerance of +/- 0.01 inches
2 All capacitances are given in picoFarads and must be kept within a tolerance of +/- 5%
* 64MB with PLL
3 Feedback capacitance values(C3) stated are to be considered a starting point only. The actual values will depend upon the PLL chosen.

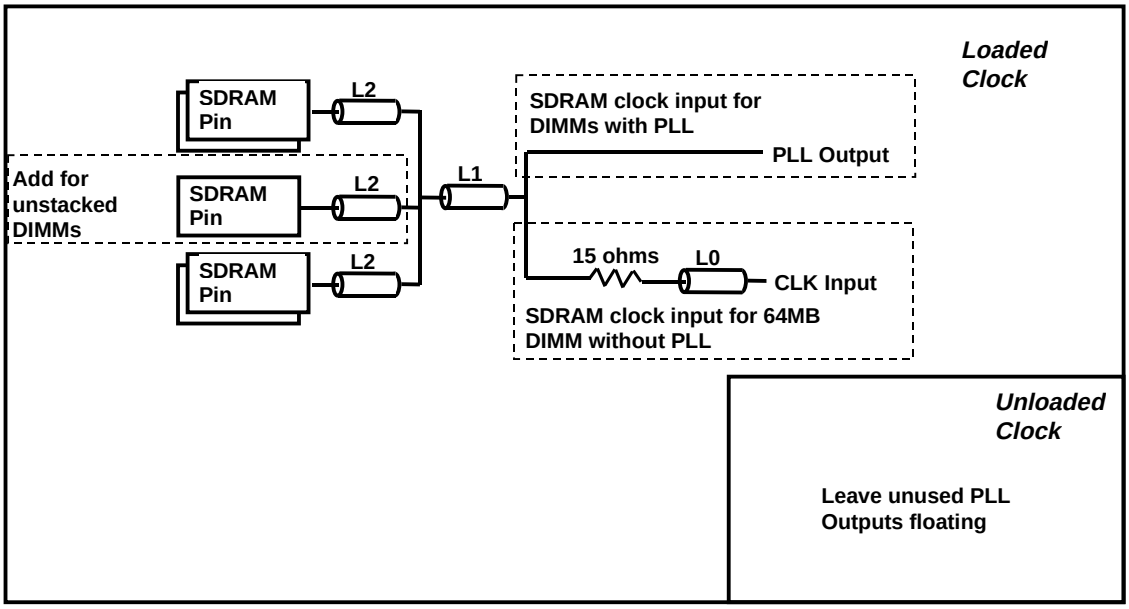



**Figure 21: Signal routing topologies for Clocks post-PLL**

**Table 13: Trace Length Table for Clock Topologies**

| DIMM Config | # of loads | L0 Min | L0 Max | L1 Min | L1 Max | L2 | Total Length |
|---|---|---|---|---|---|---|---|
| 64MB* | 3 | NA | NA | 1.856 | 1.860 | 1.270 | 3.128 |
| 64MB | 3 | 0.134 | 0.189 | 1.901 | 1.957 | 1.270 | 3.361 |
| Unstacked DIMM using x4 SDRAMs | 3 | NA | NA | 3.079 | 3.082 | 0.375 | 3.455 |
| Stacked DIMM | 4 | NA | NA | 3.444 | 3.446 | 0.200 | 3.645 |

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches
2 All capacitances are given in picoFarads and should be kept within a tolerance of +/- 5%
* 64MB with PLL

### 10.5.4 Topology for Data: DQ[63:0] & CB[7:0]

The table defines the line length ranges allowed for these signals. For the purpose of specifying trace segment lengths, the data lines have been broken down into two subcategories based on the location of their edge connector pins. These two data "zones" have lengths specified that make the data lines connecting toward the outside edge shorter in min and max length. This is done to allow the opportunity to pair the necessarily longer data line traces on the motherboard with traces that can be made shorter on the DIMMs, and the necessarily longer DIMM traces with the potentially shorter traces on the motherboard.

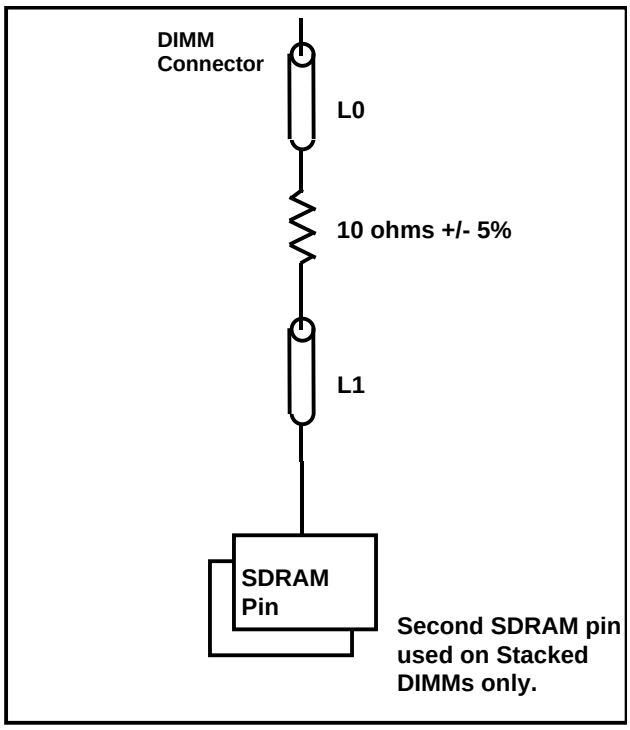



**Figure 22: Signal routing topologies for Data**

**Data Zone I : DQ [63-56, 39-24, 7-0]**
**Data Zone II : DQ [55-40, 23-8] ; CB [7-0]**

**Table 14: Trace Length Table for Data Topologies**

| DIMM Size | # of loads | Zone | L0 Min | L0 Max | L1 Min | L1 Max | Total Min | Total Max |
|---|---|---|---|---|---|---|---|---|
| 64MB | 1 | I | 0.126 | 0.154 | 0.834 | 0.861 | 0.982 | 1.000 |
| 64MB | 1 | II | 0.127 | 0.163 | 0.850 | 1.000 | 1.000 | 1.249 |
| Unstacked DIMM using x4 SDRAMs | 1 | I | 0.126 | 0.153 | 0.950 | 0.952 | 1.076 | 1.103 |
| Unstacked DIMM using x4 SDRAMs | 1 | II | 0.126 | 0.162 | 1.210 | 1.542 | 1.338 | 1.675 |
| Stacked DIMM | 2 | I | 0.127 | 0.148 | 0.973 | 1.048 | 1.115 | 1.183 |
| Stacked DIMM | 2 | II | 0.126 | 0.345 | 1.139 | 1.518 | 1.424 | 1.702 |

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches
2 Total Min and Total Max refer to the min and max respectively of L0 + L1.

#### 10.5.4.1 Topology for Data Mask (1/2/4 Loads): DQMB[7,6,4-2,0]

These signals are routed using a " Y" topology on any layer. The tables define the line length ranges allowed for these signals.

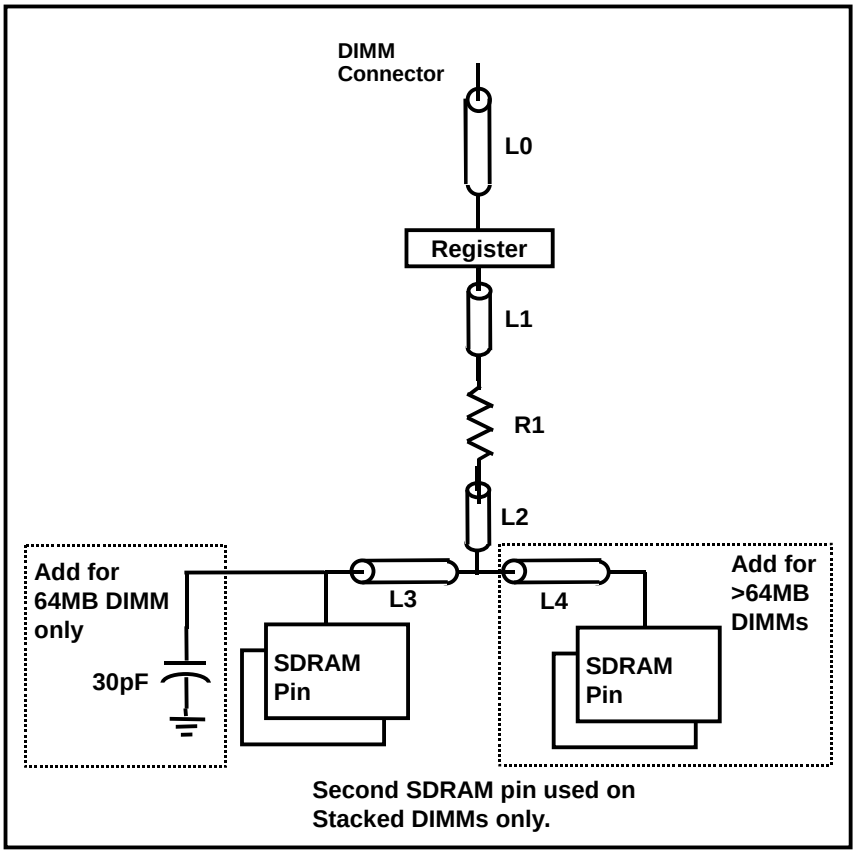



**Figure 23: Signal routing topologies for Data Mask (1/2/4 Loads)**

**Table 15: Trace Length Table for Data Mask Topologies (2/4 Loads)**

| DIMM config | # Loads | L0 Min | L0 Max | L1 Min | L1 Max | L2 Min | L2 Max | L3 Min | L3 Max | L4 Min | L4 Max | Total Min | Total Max | R1 ohms |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 64MB | 1 | 0.268 | 0.343 | 0.113 | 0.167 | 0.799 | 1.702 | 0 | -- | NA | NA | 1.274 | 2.109 | 33 |
| Unstacked DIMM using x4 SDRAMs | 2 | 0.219 | 0.539 | 0.138 | 0.174 | 3.185 | 4.229 | 0.304 | -- | 0.524 | -- | 3.862 | 5.339 | 75 |
| Stacked DIMM | 4 | 0.190 | 1.219 | 0.111 | 0.266 | 2.844 | 3.202 | 0.238 | -- | 0.470 | -- | 3.563 | 4.756 | 10 |

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches

#### 10.5.4.2 Topology for Data Mask (3/6 Loads): DQMB[5,1]

These signals are routed using a star topology on any layer. The tables define the line length ranges allowed for these signals.

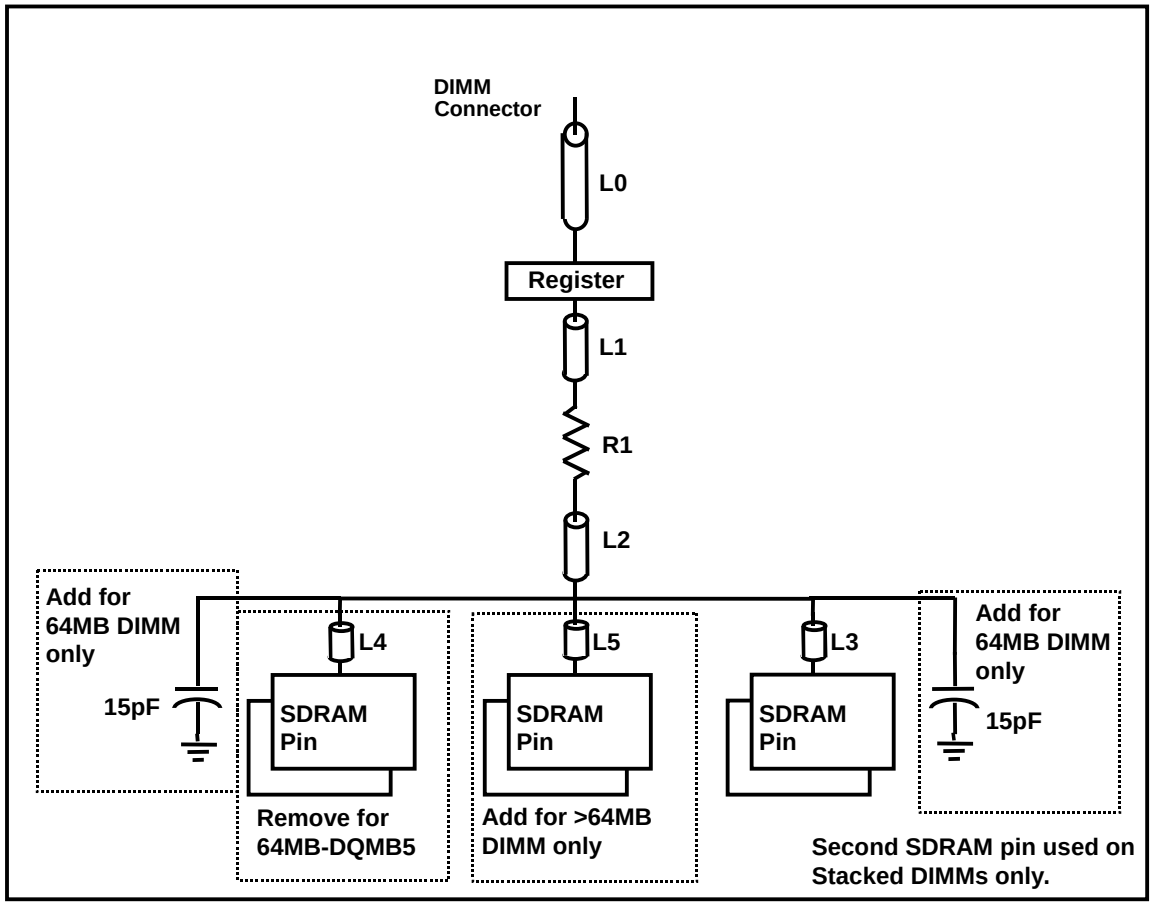



**Figure 24: Signal routing topologies for Data Mask (3/6 Loads)**

**Table 16: Trace Length Table for Data Mask Topologies (1/2/3/6 Loads)**

| DIMM config | # Loads | L0 Min | L0 Max | L1 Min | L1 Max | L2 Min | L2 Max | L3 Min | L3 Max | L4 Min | L4 Max | L5 Min | L5 Max | R1 ohms |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 64MB | 1-2 | 0.333 | -- | 0.127 | -- | 0.060 | -- | 0.800 | -- | 1.087 | -- | NA | NA | 24.9 |
| Unstacked DIMM using x4 SDRAMs | 3 | 0.214 | 0.233 | 0.135 | 0.141 | 3.723 | 3.730 | 0.584 | 0.657 | 0.584 | 0.657 | 0.056 | 0.061 | 75 |
| Stacked DIMM | 6 | 1.098 | 1.219 | 0.111 | 0.139 | 2.576 | 2.662 | 0.441 | 0.705 | 0.441 | 0.705 | 0.441 | 0.705 | 10 |

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches

#### 10.5.4.3 Topology for Chip Select: CS#[3:0]

This signal is routed using a balanced "comb" topology on any layer. The table below defines the line length ranges allowed for these signals. Once each segment length is decided upon, the other traces with the same length designator must lie within +/-10% of that length. For example, if L2 to one device is 500 mils, then L2 to all other devices must fall within 450 to 550 mils.

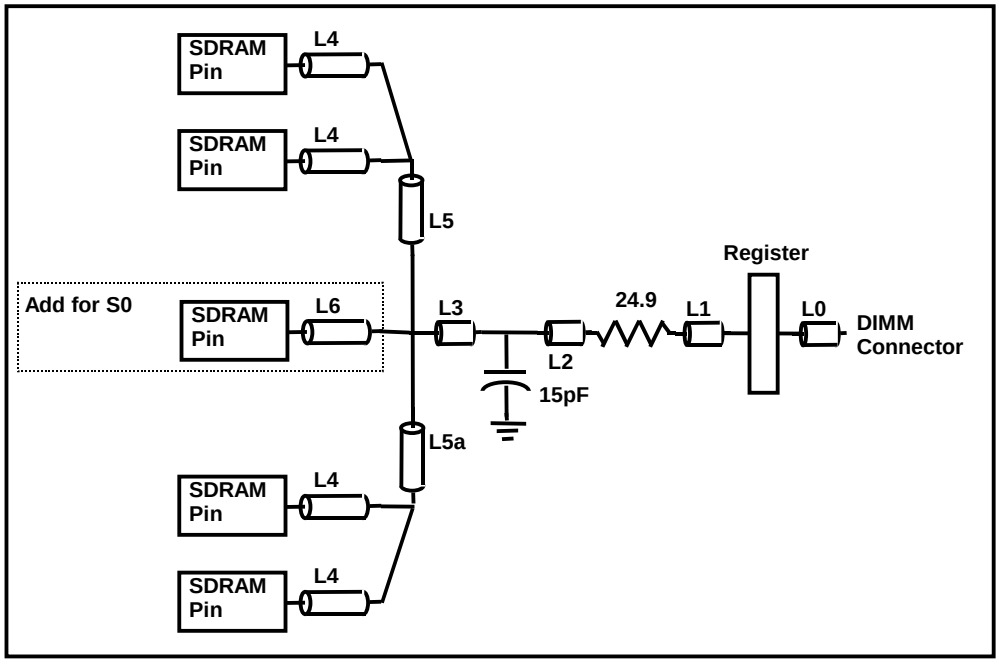



**Figure 25: Signal routing topologies for Chip Select (64MB)**

**Table 17: Trace Length Table for Chip Select Topologies (S0, S1)**

| Comp Width | # of loads | L0 | L1 | L2 | L3 | L4 Min | L4 Max | L5 | L5a | L6 |
|---|---|---|---|---|---|---|---|---|---|---|
| 64MB | 5 S0 | 0.329 | 0.124 | 0.402 | 0.657 | 0.134 | 0.350 | 0.684 | 0 | 1.313 |
| 64MB | 4 S2 | 0.276 | 0.124 | 1.187 | 0.370 | 0.134 | 0.350 | 0.238 | 0.443 | NA |

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches

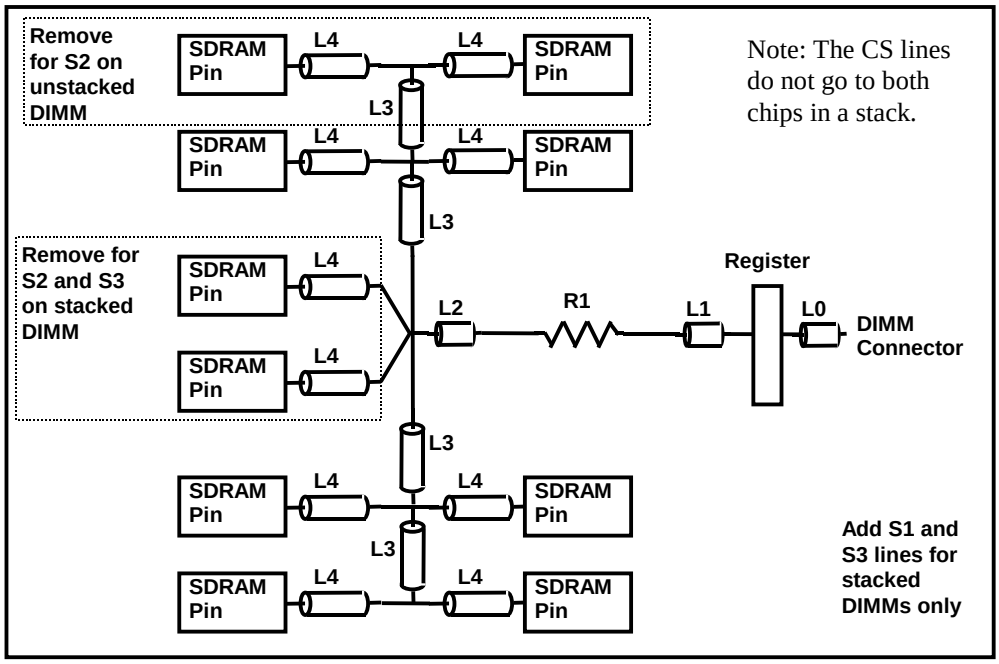



**Figure 26: Signal routing topologies for Chip Select (> 64MB DIMM)**

**Table 18: Trace Length for Chip Select Topologies (S0, S1, S2, S3)**

| Comp Width | # of loads | L0 Min | L0 Max | L1 Min | L1 Max | L2 Min | L2 Max | L3 Min | L3 Max | L4 Min | L4 Max | R1 Ohm |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unstacked DIMM using x4 SDRAMs | 10 S0 | 0.293 | -- | 0.122 | -- | 1.960 | -- | 0.557 | 0.629 | 0.221 | 0.257 | 45.3 |
| Unstacked DIMM using x4 SDRAMs | 8 S2 | 0.478 | -- | 0.134 | -- | 3.086 | -- | 0.530 | 0.742 | 0.123 | 0.370 | 45.3 |
| Stacked DIMM | 10 S0,S1 | 1.040 | 1.208 | 0.186 | 0.229 | 1.694 | 1.903 | 0.430 | 0.674 | 0.077 | 0.208 | 10 |
| Stacked DIMM | 8 S2,S3 | 0.213 | 0.235 | 0.150 | 0.180 | 2.028 | 2.032 | 0.175 | 0.595 | 0.092 | 0.106 | 10 |

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches

#### 10.5.4.4 Topology for Clock Enable: CKE#[0]

This signal is routed using a balanced "comb" topology on any layer. The table below defines the line length ranges allowed for each trace segment.

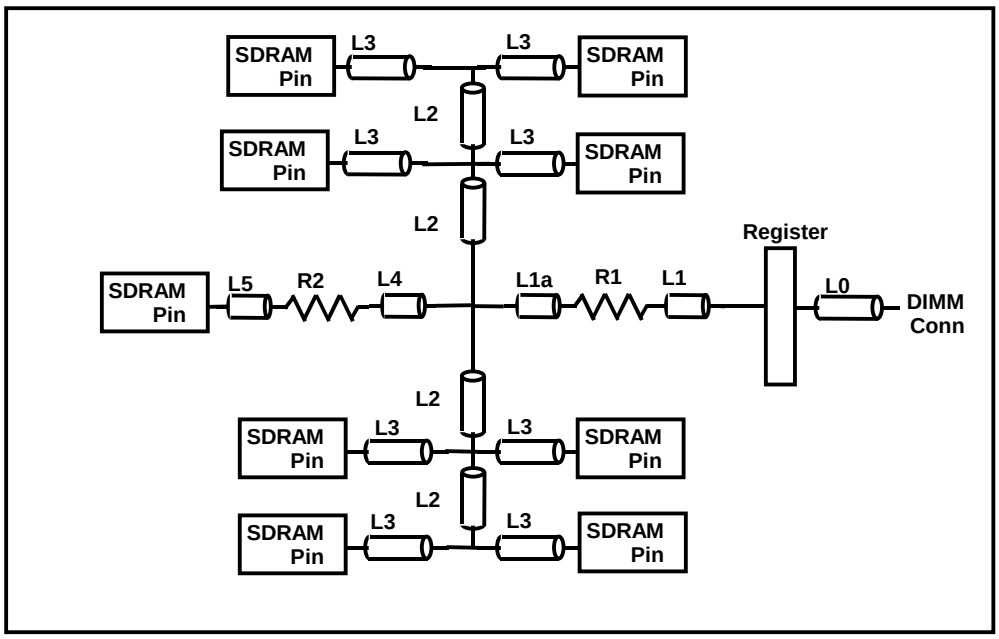



**Figure 27: Signal routing topologies for Clock Enable (64MB)**

**Table 19: Trace Length Table for Address and Control Signals**

| DIMM config | # loads | L0 Min | L0 Max | L1 Min | L1 Max | L1a Min | L1a Max | L2 Min | L2 Max | L3 Min | L3 Max |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 64MB | 9 | 0.289 | 0.686 | 0.110 | 0.172 | 0.576 | 1.212 | 0.661 | 1.401 | 0.125 | 0.375 |

**Table 20: Trace Length Table for Address and Control Signals contd.**

| DIMM config | L4 Min | L4 Max | L5 Min | L5 Max | R1 ohms | R2 ohms |
|---|---|---|---|---|---|---|
| 64MB | 0.058 | 0.181 | 0.127 | 0.272 | 0 | 100 |

1. All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches

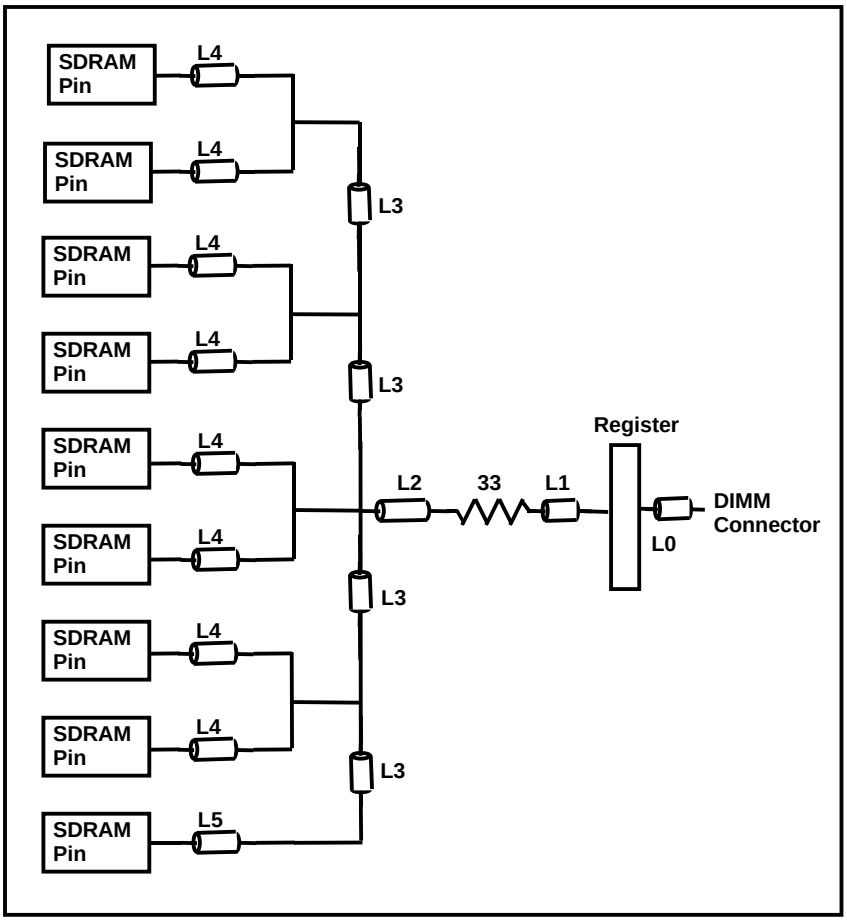



**Figure 28: Signal routing topologies for Clock Enable (Unstacked DIMM)**

**Table 21: Trace Length Tables for Clock Enable Topologies**

| DIMM config | # Loads | L0 Min | L0 Max | L1 Min | L1 Max | L2 Min | L2 Max | L3 Min | L3 Max | L4 Min | L4 Max | L5 Min | L5 Max |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unstacked DIMM using x4 SDRAMs | 9 | 0.138 | -- | 0.149 | 0.313 | 2.045 | 2.983 | 0.365 | 0.711 | 0.185 | 0.317 | 0.069 | 0.105 |

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches

Note: The CKE0 line is double loaded before the register, so the above diagram is repeated twice to route the CKE0 line to all 18 SDRAM.

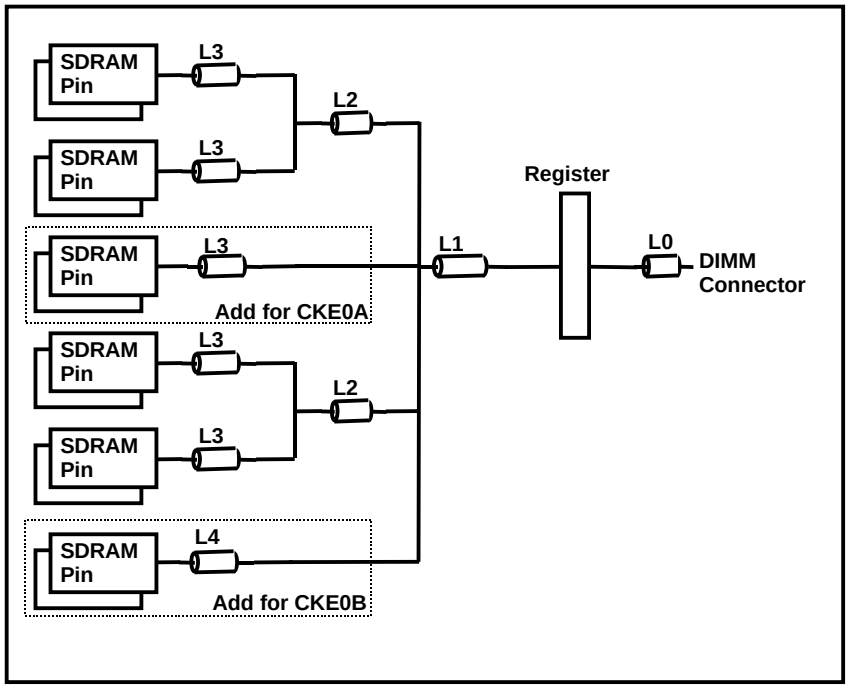



**Figure 29: Signal routing topologies for Clock Enable (stacked DIMM)**

Note: The CKE signal is routed to 4 register inputs, and the above topology is repeated 4 times (A-D).

**Table 22: Trace Length Tables for Clock Enable Topologies**

| DIMM config | # Loads | L0 | L0 | L1 | L1 | L2 | L2 | L3 | L3 | L4 |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Stacked DIMM | 8-10 | 0.753 | 0.968 | 2.579 | 3.261 | 0.172 | 0.563 | 0.084 | 0.323 | 0.464 |

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches

Note: The controller will need to drive both Chip Selects along with CKE0 simultaneously to place the 256MB DIMM in self refresh.

#### 10.5.4.5 Address/Control: MAx, BAx, SRAS#, SCAS#, WE#(*)

These signals are routed using a balanced, double-sided "comb" topology on any layer. The table below defines the line length ranges allowed for these signals.

(*) topology applies to WE# for 64 MB and Unstacked DIMMs designs only.

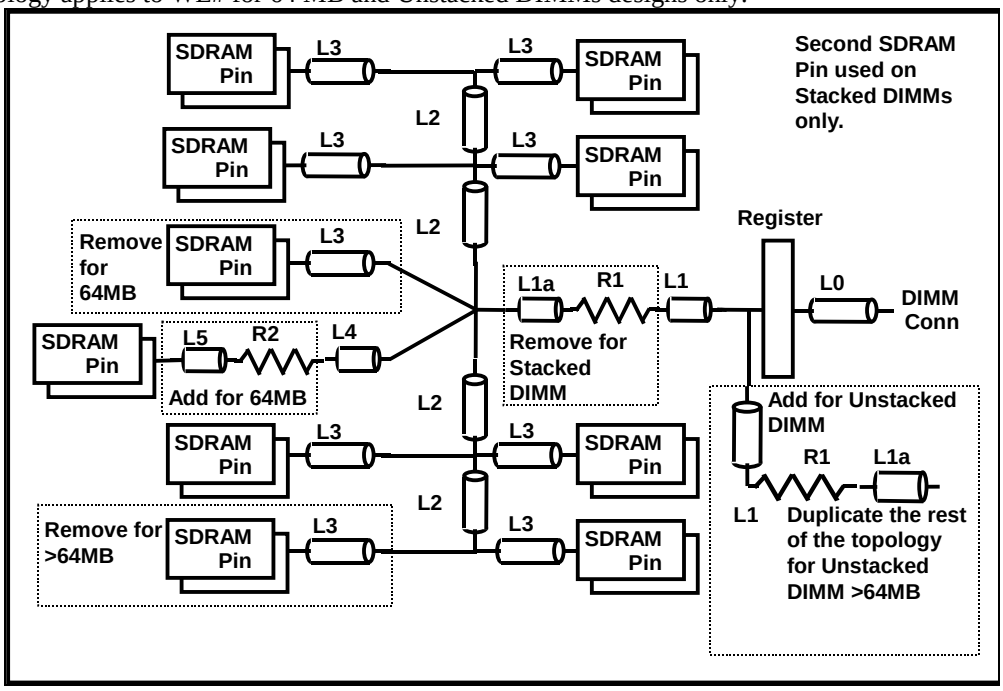



**Figure 30: Signal routing topologies for Address and Control Signals**

Note: The above signals are double loaded on the input to the register, so the above topology is repeated twice for the stacked DIMM.

**Table 23: Trace Length Table for Address and Control Signals**

| DIMM config | # loads | L0 Min | L0 Max | L1 Min | L1 Max | L1a Min | L1a Max | L2 Min | L2 Max | L3 Min | L3 Max | L4 Min | L4 Max | L5 Min | L5 Max |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 64MB | 9 | 0.289 | 0.686 | 0.110 | 0.172 | 0.576 | 1.212 | 0.661 | 1.401 | 0.125 | 0.375 | 0.058 | 0.181 | 0.127 | 0.272 |
| Unstacked DIMM using x4 SDRAMs | 18 | 0.138 | 0.242 | 0.149 | 0.313 | 1.857 | 2.983 | 0.335 | 0.758 | 0.069 | 0.358 | 0.155 | 0.358 | NA | NA |
| Stacked DIMM | 36 | 0.255 | 0.534 | 2.011 | 2.930 | NA | NA | 0.475 | 0.664 | 0.093 | 0.347 | 0.093 | 0.347 | NA | NA |

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches

**Table 24: Resistance values in the Address and Control Signal topologies**

| DIMM config | R1 | R2 |
|---|---|---|
| 64MB | 0 | 100 |
| Unstacked DIMM using x4 SDRAMs | 33 | NA |
| Stacked DIMM | NA | NA |

#### 10.5.4.6 Stacked DIMM WE# Topology

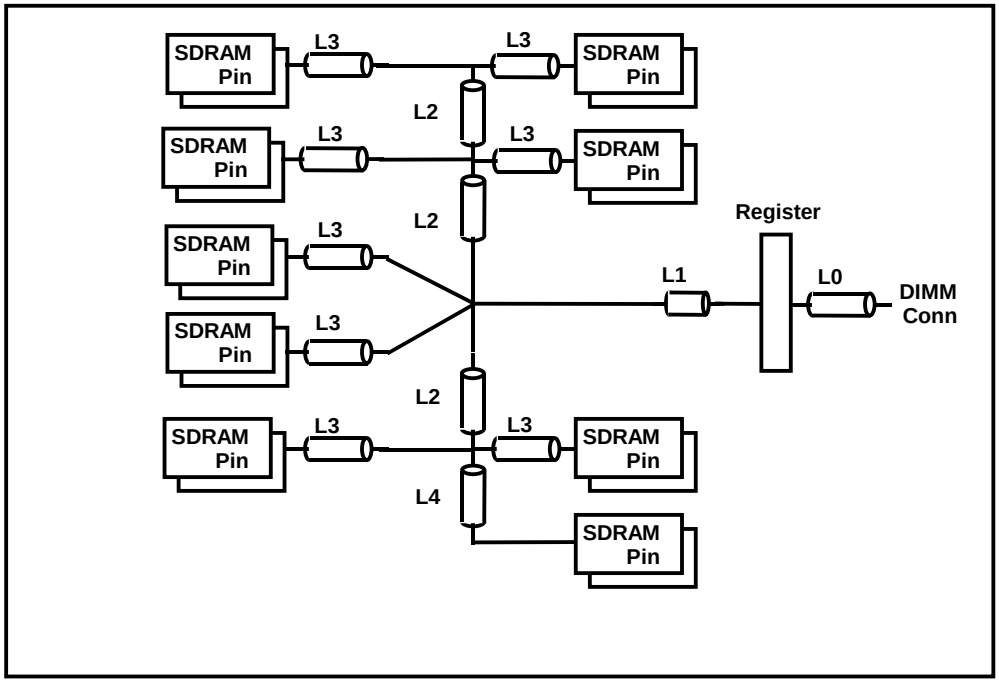



**Figure 31: Signal routing topologies for Write Enable (stacked DIMM)**

Note: The above signals are double loaded on the input to the register, so the above topology is repeated twice for the stacked DIMM.

**Table 25: Trace Length Table for Write Enable**

| DIMM config | # loads | L0 Min | L0 Max | L1 Min | L1 Max | L2 Min | L2 Max | L3 Min | L3 Max | L4 Min | L4 Max |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Stacked DIMM | 36 | 1.255 | 1.255 | 1.943 | 1.943 | 0.255 | 0.501 | 0.076 | 0.252 | 0.768 | 0.768 |

All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches

# 11 SDRAM Component Specifications

The 100 MHz SDRAM components used with this DIMM design spec MUST adhere to the latest revision of the Intel "PC SDRAM" Specification for operation of 100 MHz SDRAM devices. Please reference this document for all technical specifications and requirements for such devices. Any violation of the requirements of the Intel PC SDRAM component spec constitute a violation of this document as well.

The following table lists additional min/max package parasitic and die capacitance assumptions used for simulations of the stacked x4 designs. These assumptions include the package parasitics as well as the min and max values from the Intel 'PC SDRAM' spec.

**Table 26: Stacked Component Pin Capacitance**

| Signal | Min Total Capacitance (pF) | Max Total Capacitance (pF) |
|---|---|---|
| DQ | 8.4 | 13.4 |
| Clk | 5.4 | 8.4 |
| S | 5.1 | 7.6 |
| All other Address & Control signals | 5.4 | 10.4 |

# 12 EEPROM Component Specifications

The Serial Presence Detect function MUST be implemented on the PC SDRAM Registered DIMM. The component used and the data contents must adhere to the most recent version of the Intel PC SDRAM Serial Presence Detect Specification. Please reference to that document for all technical specifications and requirements of the serial presence detect devices. Any violation of the requirements of the Intel PC SDRAM Serial Presence Detect specification constitutes a violation of this document as well.

# 13 Register Component Specifications

The following components are recommended for registers for the 100 MHz registered DIMM:

| Part Number | |
|---|---|
| 162835 | 18Bit, 1:1 Register (w/internal damping resistors) |
| 16835 | 18Bit, 1:1 Register |

Below is a chart explaining which registers are used on which DIMMs.

**Table 27: DIMM Register Use**

| DIMM | REGISTER | QTY |
|---|---|---|
| Stacked DIMM | 162835 | 3 |
| Unstacked DIMM | 16835 | 2 |
| 64MB w/PLL | 162835 | 2 |
| 64MB wo/PLL | 162835 | 2 |

The following specifications for the registers are critical for proper operation for the registered DIMM.

**Table 28: Register Specification Parametrics**

| Device | Type | Parameter | Symbol | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| 16835 | 162835 | Reg Clk Input Capacitance | Cin | 3.30 | 6.00 | pF | 10MHz |
| 16835 | 162835 | Max clock frequency | | 150 | | MHz | |
| 16835 | 162835 | Output edge rate | | 1.00 | 2.50 | volts/nsec | Cload=50pF, Vcc=3.3+/-0.165 V, Between 1.2 and 1.8 V |
| | 162835 | Propagation Delay Time-Reg Mode | Tco | 1.9 | 4.5 | nsec | Cload=50pF, Vcc=3.3+/-0.165 V, CLK to any Y |
| 16835 | | Propagation Delay Time-Reg Mode | Tco | 1.7 | 4.5 | nsec | Cload=50pF, Vcc=3.3+/-0.165 V, CLK to any Y |
| | 162835 | Propagation Delay Time-Reg Mode | Tco | 1.4 | 2.9 | nsec | Cload=0pF, Vcc=3.3+/-0.165 V, CLK to any Y |
| 16835 | | Propagation Delay Time-Reg Mode | Tco | 1.5 | 3.0 | nsec | Cload=0pF, Vcc=3.3+/-0.165 V, CLK to any Y |
| 16835 | 162835 | Propagation Delay Time-Buffer Mode | Tpd | 0.9 | 2.0 | nsec | Cload=0pF, Vcc=3.3+/-0.165 V, input to any Y |
| 16835 | 162835 | Propagation Delay Time-Buffer Mode | Tpd | 1.0 | 4.5 | nsec | Cload=50pF, Vcc=3.3+/-0.165 V, input to any Y |
| 16835 | 162835 | Max allowable SSO delay[1] | | | 300.0 | psec | Cload=50pF, any output combination, Vcc=3.3+/-0.165 V |

| Device | Type | Parameter | Symbol | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| 16835 | 162835 | Setup Time | Tsu | 1.7 | | nsec | Vcc=3.3+/-0.165 V, any input |
| 16835 | 162835 | Hold Time | Th | 0.7 | | nsec | Vcc=3.3+/-0.165 V, any input |
| 16835 | 162835 | Operating Temperature Range | Tcase | 0 | 85 | deg C | |
| 16835 | 162835 | Input current | Iin | | 10.0 | uA | Vin=0 to 3.465V, Vcc=3.3+/-0.165 V |

1 SSO delay is the delay caused due to simultaneous switching outputs.

The following I-V characteristics must be met, along with the above parameters to comply with this document.

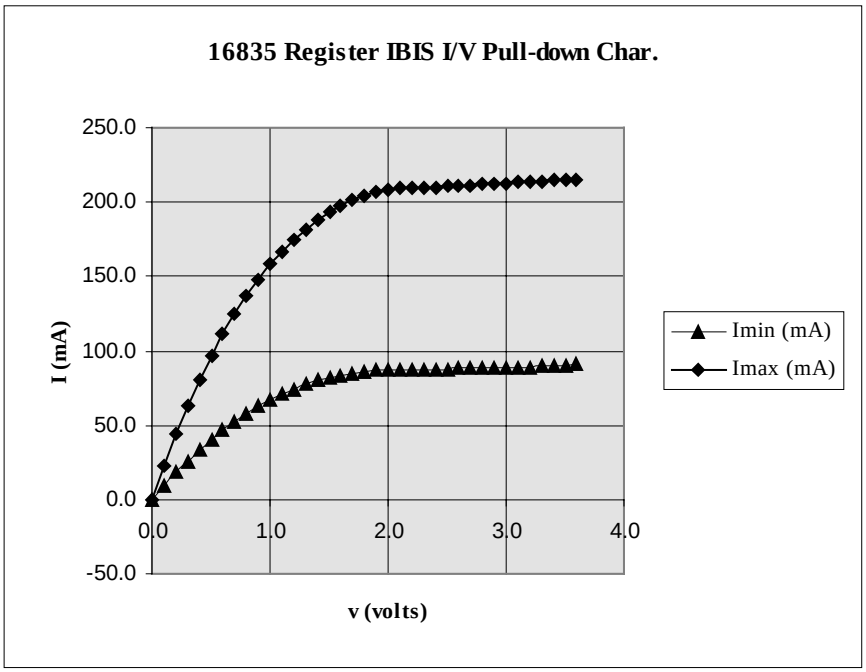



**Figure 32: I-V Characteristics for 16835 Register Output – Pull Down**

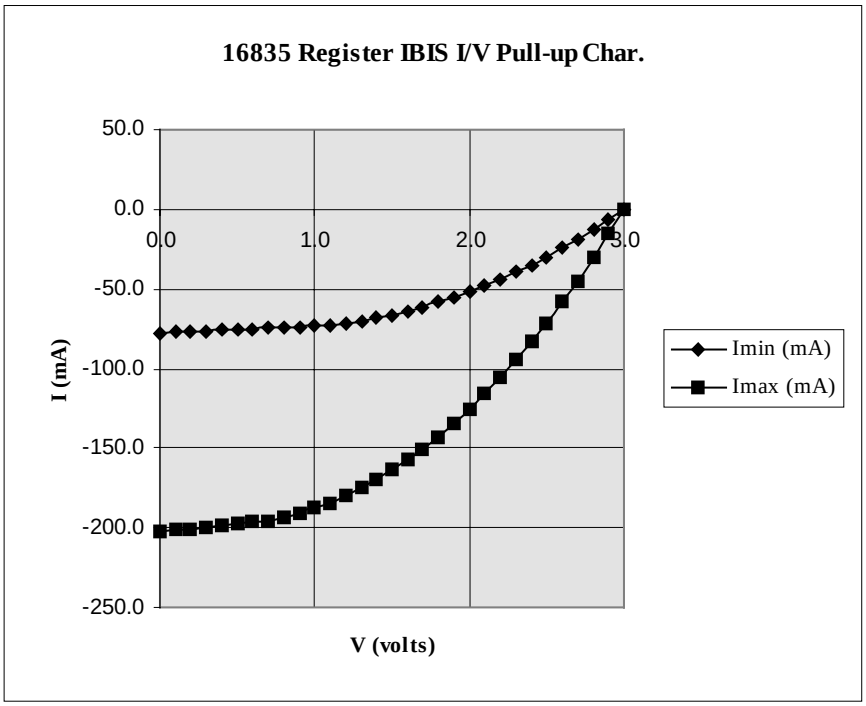



**Figure 33: I-V Characteristics for 16835 Register Output – Pull Up**

## Table 29: 16835 I-V Data

| Pulldown V (volts) | Imin (mA) | Imax (mA) | Pulllup V (volts) | Imin (mA) | Imax (mA) |
|---|---|---|---|---|---|
| 0.0 | 0.0 | 0.0 | 3.0 | 0.0 | 0.0 |
| 0.1 | 9.3 | 22.6 | 2.9 | -6.6 | -15.6 |
| 0.2 | 17.9 | 43.5 | 2.8 | -12.9 | -30.6 |
| 0.3 | 26.0 | 62.7 | 2.7 | -18.8 | -44.8 |
| 0.4 | 33.5 | 80.3 | 2.6 | -24.5 | -58.3 |
| 0.5 | 40.4 | 96.5 | 2.5 | -29.8 | -71.2 |
| 0.6 | 46.7 | 111.2 | 2.4 | -34.8 | -83.3 |
| 0.7 | 52.6 | 124.7 | 2.3 | -39.5 | -94.9 |
| 0.8 | 57.9 | 136.9 | 2.2 | -43.9 | -105.7 |
| 0.9 | 62.7 | 148.0 | 2.1 | -48.0 | -115.9 |
| 1.0 | 67.0 | 157.9 | 2.0 | -51.8 | -125.5 |
| 1.1 | 70.9 | 166.8 | 1.9 | -55.3 | -134.4 |
| 1.2 | 74.3 | 174.7 | 1.8 | -58.4 | -142.7 |
| 1.3 | 77.3 | 181.7 | 1.7 | -61.3 | -150.4 |
| 1.4 | 79.9 | 187.8 | 1.6 | -63.9 | -157.5 |
| 1.5 | 82.0 | 193.1 | 1.5 | -66.2 | -164.0 |
| 1.6 | 83.7 | 197.5 | 1.4 | -68.2 | -169.9 |
| 1.7 | 85.1 | 201.2 | 1.3 | -70.0 | -175.2 |
| 1.8 | 86.0 | 204.2 | 1.2 | -71.4 | -180.0 |
| 1.9 | 86.6 | 206.4 | 1.1 | -72.5 | -184.2 |
| 2.0 | 86.8 | 208.0 | 1.0 | -73.4 | -187.8 |
| 2.1 | 87.0 | 209.0 | 0.9 | -73.8 | -190.9 |
| 2.2 | 87.2 | 209.4 | 0.8 | -74.3 | -193.4 |
| 2.3 | 87.4 | 209.8 | 0.7 | -74.7 | -195.4 |
| 2.4 | 87.6 | 210.3 | 0.6 | -75.1 | -196.6 |
| 2.5 | 87.8 | 210.7 | 0.5 | -75.5 | -197.6 |
| 2.6 | 88.0 | 211.1 | 0.4 | -75.9 | -198.5 |
| 2.7 | 88.2 | 211.6 | 0.3 | -76.4 | -199.5 |
| 2.8 | 88.4 | 212.0 | 0.2 | -76.8 | -200.5 |
| 2.9 | 88.6 | 212.4 | 0.1 | -77.2 | -201.5 |
| 3.0 | 88.8 | 212.9 | 0.0 | -77.7 | -202.6 |
| 3.1 | 89.0 | 213.3 | | | |
| 3.2 | 89.2 | 213.8 | | | |
| 3.3 | 89.4 | 214.2 | | | |
| 3.4 | 89.6 | 214.6 | | | |
| 3.5 | 89.9 | 215.1 | | | |
| 3.6 | 90.7 | 215.5 | | | |

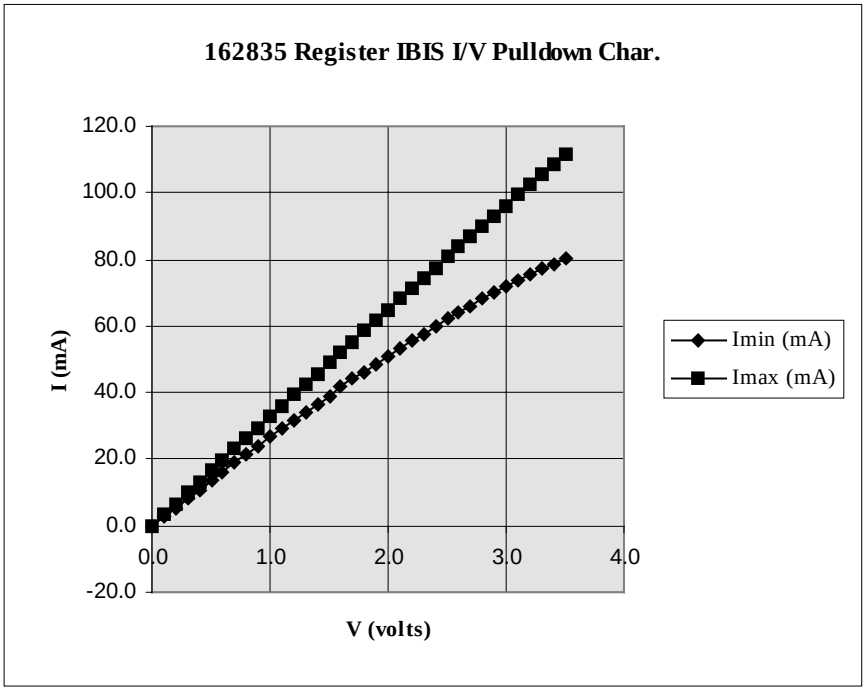



**Figure 34: I-V Characteristics for 162835 Register Output – Pull Down**

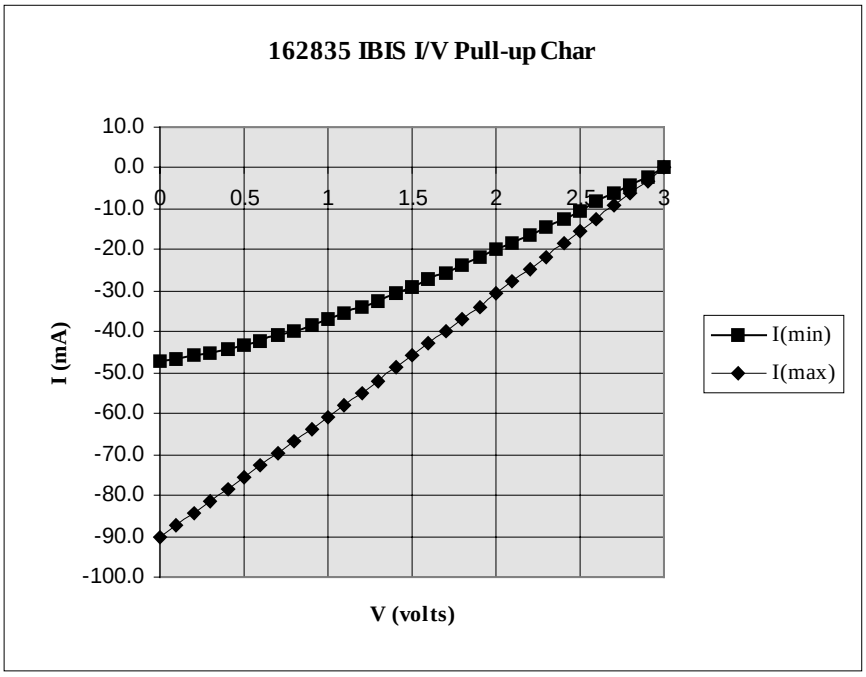



**Figure 35: I-V Characteristics for 162835 Register Output – Pull Up**

## Table 30: 162835 I-V Data

| Pulldown | | | Pulllup | | |
|---|---|---|---|---|---|
| V (volts) | Imin (mA) | Imax (mA) | V (volts) | Imax (mA) | Imin (mA) |
| 0.0 | 0.0 | 0.0 | 3.0 | 0.0 | 0.0 |
| 0.1 | 2.7 | 3.3 | 2.9 | -3.1 | -2.4 |
| 0.2 | 5.5 | 6.6 | 2.8 | -6.2 | -4.9 |
| 0.3 | 8.2 | 9.9 | 2.7 | -9.3 | -7.3 |
| 0.4 | 10.9 | 13.2 | 2.6 | -12.4 | -9.7 |
| 0.5 | 13.5 | 16.5 | 2.5 | -15.4 | -12.1 |
| 0.6 | 16.2 | 19.7 | 2.4 | -18.5 | -14.4 |
| 0.7 | 18.8 | 23.0 | 2.3 | -21.6 | -16.8 |
| 0.8 | 21.4 | 26.3 | 2.2 | -24.6 | -19.1 |
| 0.9 | 24.0 | 29.5 | 2.1 | -27.7 | -21.4 |
| 1.0 | 26.6 | 32.8 | 2.0 | -30.7 | -23.7 |
| 1.1 | 29.2 | 36.0 | 1.9 | -33.8 | -25.9 |
| 1.2 | 31.7 | 39.3 | 1.8 | -36.8 | -28.1 |
| 1.3 | 34.2 | 42.5 | 1.7 | -39.8 | -30.4 |
| 1.4 | 36.7 | 45.7 | 1.6 | -42.8 | -32.5 |
| 1.5 | 39.2 | 48.9 | 1.5 | -45.9 | -34.7 |
| 1.6 | 41.6 | 52.2 | 1.4 | -48.9 | -36.8 |
| 1.7 | 44.0 | 55.4 | 1.3 | -51.9 | -38.9 |
| 1.8 | 46.4 | 58.6 | 1.2 | -54.9 | -41.0 |
| 1.9 | 48.7 | 61.7 | 1.1 | -57.8 | -43.1 |
| 2.0 | 51.0 | 64.9 | 1.0 | -60.8 | -45.1 |
| 2.1 | 53.3 | 68.1 | 0.9 | -63.8 | -47.1 |
| 2.2 | 55.6 | 71.3 | 0.8 | -66.7 | -49.0 |
| 2.3 | 57.8 | 74.4 | 0.7 | -69.7 | -50.9 |
| 2.4 | 59.9 | 77.5 | 0.6 | -72.6 | -52.8 |
| 2.5 | 62.1 | 80.7 | 0.5 | -75.6 | -54.6 |
| 2.6 | 64.1 | 83.8 | 0.4 | -78.5 | -56.4 |
| 2.7 | 66.2 | 86.9 | 0.3 | -81.4 | -58.1 |
| 2.8 | 68.2 | 90.0 | 0.2 | -84.3 | -59.8 |
| 2.9 | 70.1 | 93.1 | 0.1 | -87.2 | -61.4 |
| 3.0 | 72.0 | 96.2 | 0.0 | -90.1 | -63.0 |
| 3.1 | 73.8 | 99.3 | | | |
| 3.2 | 75.5 | 102.4 | | | |
| 3.3 | 77.2 | 105.4 | | | |
| 3.4 | 78.7 | 108.4 | | | |
| 3.5 | 80.2 | 111.5 | | | |

# 14 PLL Component Specifications

The following components are recommended for the PLL for the 100 MHz registered DIMM:

| Part Number | |
|---|---|
| 2509 | 1:9 PLL Based Clock Driver |
| 2510 | 1:10 PLL Based Clock Driver |

The following specifications for the PLL are critical in proper operation for the registered DIMM.

### Table 31: PLL Component Specifications

| Parameter | Symbol | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| PLL Clk Input Capacitance | Cin | 2.50 | 6.00 | pF | 10MHz |
| PLL Feedback Input Capacitance | Cin | 2.50 | 6.00 | pF | 10MHz |
| Input clock rise/fall edge rate | | 1.00 | 2.50 | volts/nsec | |
| Output rise/fall edge rate | | 1.00 | 2.50 | volts/nsec | Cload=50pF, Vcc=3.3+/-0.165 V, Between 1.2 and 1.8 V |
| Input clock duty cycle | | 40 | 60 | % | |
| Output clock duty cycle | | 45 | 55 | % | |
| Operating Frequency Range | | 50 | 125 | MHz | |
| Operating temperature range | Tcase | 0 | 85 | deg C | |
| Operating Voltage range for specification | | 3.135 | 3.465 | volts | |
| Output stabilization time | | | 1 | msec | After power up |
| Analog power supply rejection | | 100 | | mV, pk-pk | DC to 10MHz |
| Output clock(n) to clock(n+1) jitter | | -100 | 100 | psec | with and w/o Spread Spectrum Clock (SSC) Input [1] |
| Output to output skew | Tskew | | 200 | psec | |
| SSC Induced skew | | -200 | 200 | psec | See below |
| Static Phase Error | Tspe | -150 | 150 | psec | 66 MHz<f<100 MHz, 0pF feedback load |
| Phase Error –Jitter | | -50 | 50 | psec | f>66 MHz |
| Input current | Iin | -5 | 5 | uA | |
| Power dissipation | | | 700 | mW | 55C free-air ambient |

1 SSC(Spread Spectrum Clock) Induced Skew: SSC clock synthesizers are commonly used on system motherboards to reduce EMI. The PLL used on PC100 registered DIMMs must be capable of meeting all of the above test parameters while supporting SSC synthesizers with the following parameters:

| | | Min | Max | Units | |
|---|---|---|---|---|---|
| SSC modulation frequency | | 30.00 | 50.00 | KHz | |
| SSC clock input frequency deviation | | 0.00 | 0.50 | % | ie freq range for 100 MHz is 99.5 to 100 MHz |

**-PLL designs should target the values below to meet the 200ps maximum of SSC induced skew:**

| | | Min | Max | Units | |
|---|---|---|---|---|---|
| PLL loop bandwidth | | 1.20 | | MHz | |
| Phase angle | | | -0.031 | degrees | |

Below is a chart explaining which PLLs are used on which DIMMs.

### Table 32: DIMM PLL Use

| DIMM | PLL |
|---|---|
| Stacked DIMM | 2510 |
| Unstacked DIMM | 2509 |
| 64MB w/PLL | 2509 |
| 64MB wo/PLL | NA |

The Output Buffers for all PLL's used for these designs must conform within the following Min/Max I/V Range:

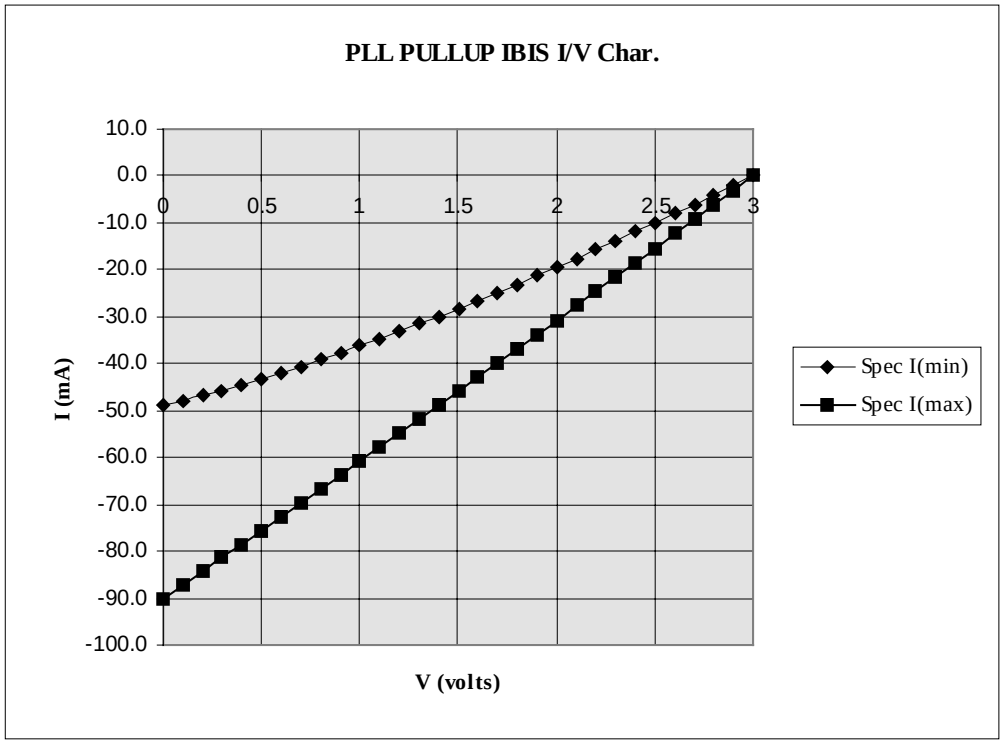



**Figure 36: I-V Characteristics for PLL Output – Pull up**

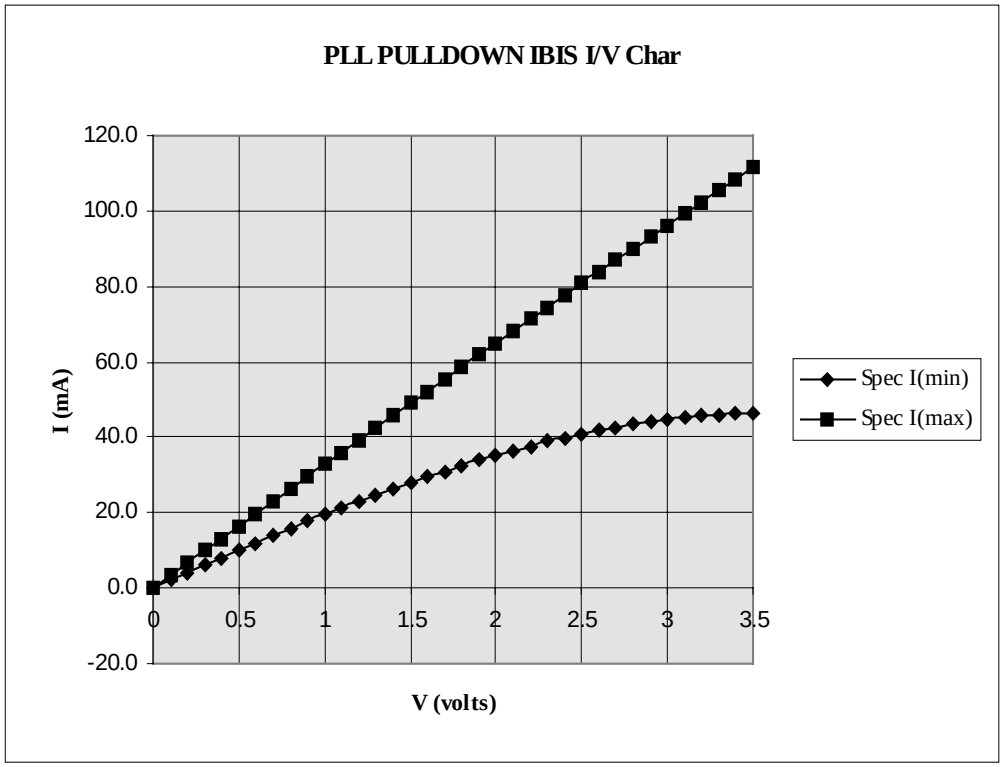



**Figure 37: I-V Characteristics for PLL Output – Pull Down**

The Output Buffer I/V data for all PLL's is listed for reference:

**Table 33: PLL Output I-V Data**

| Pulldown | | | Pullup | | |
|---|---|---|---|---|---|
| V(Volts) | Imin(mA) | Imax(mA) | V(Volts) | Imin(mA) | Imax(mA) |
| 0 | 0.0 | 0 | 3 | 0.0 | 0.0 |
| 0.1 | 2.1 | 3.30401 | 2.9 | -2.1 | -3.1 |
| 0.2 | 4.1 | 6.60266 | 2.8 | -4.1 | -6.2 |
| 0.3 | 6.2 | 9.89585 | 2.7 | -6.1 | -9.3 |
| 0.4 | 8.2 | 13.1835 | 2.6 | -8.0 | -12.4 |
| 0.5 | 10.1 | 16.4654 | 2.5 | -10.0 | -15.4 |
| 0.6 | 12.1 | 19.7415 | 2.4 | -11.9 | -18.5 |
| 0.7 | 14.0 | 23.0116 | 2.3 | -13.9 | -21.6 |
| 0.8 | 15.8 | 26.2757 | 2.2 | -15.7 | -24.6 |
| 0.9 | 17.7 | 29.5336 | 2.1 | -17.6 | -27.7 |
| 1 | 19.5 | 32.7852 | 2 | -19.4 | -30.7 |
| 1.1 | 21.3 | 36.0302 | 1.9 | -21.3 | -33.8 |
| 1.2 | 23.0 | 39.2687 | 1.8 | -23.1 | -36.8 |
| 1.3 | 24.7 | 42.5003 | 1.7 | -24.8 | -39.8 |
| 1.4 | 26.3 | 45.725 | 1.6 | -26.6 | -42.8 |
| 1.5 | 27.9 | 48.9426 | 1.5 | -28.3 | -45.9 |
| 1.6 | 29.5 | 52.1529 | 1.4 | -29.9 | -48.9 |
| 1.7 | 31.0 | 55.3557 | 1.3 | -31.6 | -51.9 |
| 1.8 | 32.4 | 58.5509 | 1.2 | -33.2 | -54.9 |
| 1.9 | 33.9 | 61.7382 | 1.1 | -34.7 | -57.8 |
| 2 | 35.2 | 64.9175 | 1 | -36.3 | -60.8 |
| 2.1 | 36.5 | 68.0885 | 0.9 | -37.7 | -63.8 |
| 2.2 | 37.7 | 71.2511 | 0.8 | -39.2 | -66.7 |
| 2.3 | 38.9 | 74.4049 | 0.7 | -40.6 | -69.7 |
| 2.4 | 39.9 | 77.5498 | 0.6 | -41.9 | -72.6 |
| 2.5 | 40.9 | 80.6855 | 0.5 | -43.2 | -75.6 |
| 2.6 | 41.9 | 83.8117 | 0.4 | -44.5 | -78.5 |
| 2.7 | 42.7 | 86.9282 | 0.3 | -45.7 | -81.4 |
| 2.8 | 43.4 | 90.0347 | 0.2 | -46.8 | -84.3 |
| 2.9 | 44.1 | 93.1308 | 0.1 | -47.9 | -87.2 |
| 3 | 44.7 | 96.2163 | 0 | -48.9 | -90.1 |
| 3.1 | 45.1 | 99.2909 | | | |
| 3.2 | 45.6 | 102.354 | | | |
| 3.3 | 45.9 | 105.406 | | | |
| 3.4 | 46.2 | 108.445 | | | |
| 3.5 | 46.5 | 111.472 | | | |