

# Intel 100 MHz Pentium(tm) II processor/440BX AGPset Uniprocessor Customer Reference Schematics Revision 1.0

**\*\* Please note that these schematics are subject to change.**

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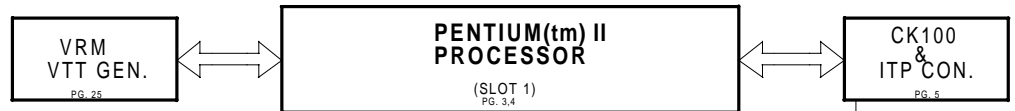
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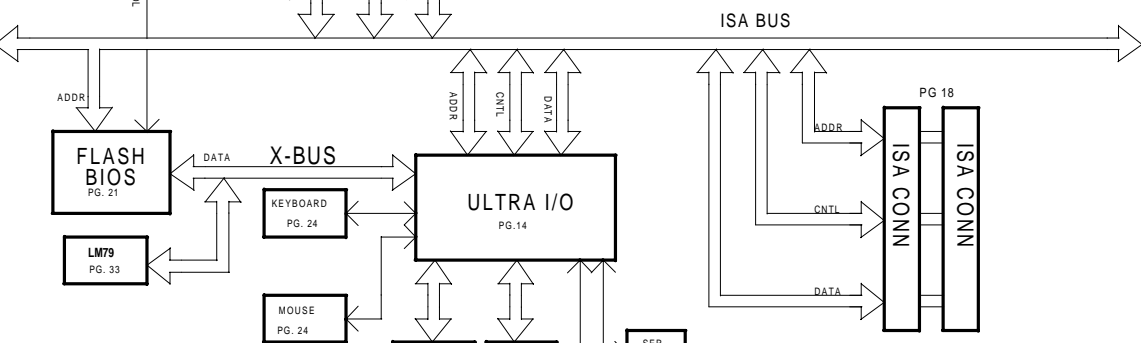
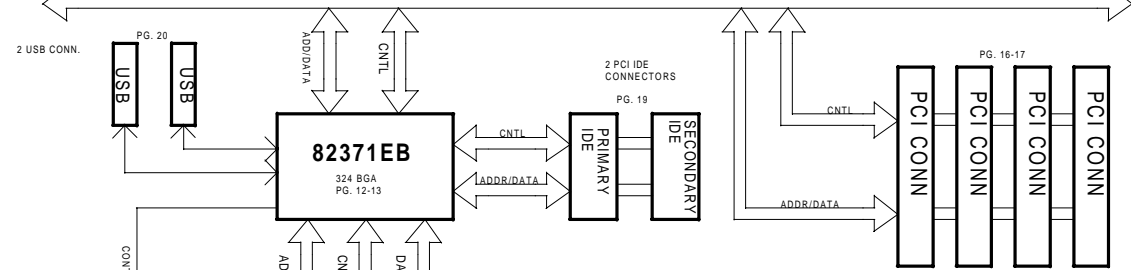
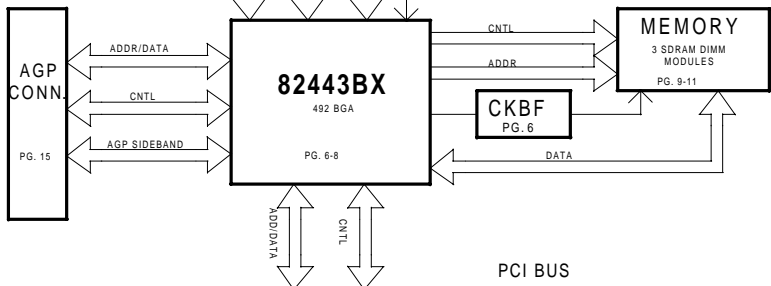
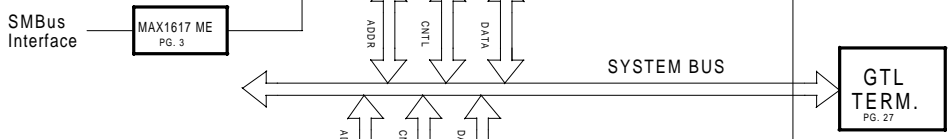
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| Title<br>Intel 100MHz Pentium(tm) II processor/440BX AGPset Uni-Processor Cover Sheet |  |               |
| Size<br>A   | Document Number<br>Intel(R) 440BX AGPset | Rev<br>1.0    |
| Date: Thursday, April 09, 1998  |  | Sheet 1 of 34 |



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|                         |           |
|-------------------------|-----------|
| RESET, POWER CONNECTORS | PG. 26    |
| ISA, PCI RESISTORS      | PG. 28-29 |
| DECOUPLING CAPACITORS   | PG. 30-32 |

| DEVICE TABLE        |                      |          |
|---------------------|----------------------|----------|
| DEVICE TYPE         | REFERENCE DESIGNATOR | PAGE #   |
| FUSES               | F1,F2,F3,F4          | 20,24    |
| ITP Connector       | J2                   | 5        |
| DIMM Sockets        | J4,J5,J6             | 9,10,11  |
| ISA Connectors      | J12, J13             | 18       |
| IDE Connectors      | J14, J15             | 19       |
| USB Connectors      | J16, J17             | 20       |
| VRM8.2              | J24                  | 25       |
| Slot 1 Connector    | J33 A,B              | 3,4      |
| AGP Connector       | J32                  | 15       |
| PCI Connectors      | J34-37               | 16,17    |
| BLM31A700S          | L1-L6,L7-L13         | 20,24    |
| CK100               | U1                   | 5        |
| 74LVC14 3VSB        | U5 A,B,C,D,E,F       | 13,26    |
| FDC37C932FR         | U6                   | 14       |
| 74AS07              | U7 A,B,C,D,E,F       | 15,26,29 |
| 74HC14              | U8 A,B,C,D,E,F       | 21,25,26 |
| E28F002BC-T(FLASH)  | U9                   | 21       |
| 74F07               | U12 A,B,C,D,E,F      | 25,26,29 |
| 74LVC3244           | U13                  | 25       |
| 74ALS08             | U16 A,B,C,D          | 26,29    |
| 74HC10 5VSB         | U17 A,B,C            | 13,26,29 |
| 82443BX             | U19-1,2,3            | 6,7,8    |
| CKBF                | U20                  | 6        |
| LM79                | U21                  | 33       |
| 74F07 5VSB          | U28 A,B,C,D,E,F      | 13,26,29 |
| 82371EB (PIIX4E)    | U23 A,B              | 12,13    |
| MAX1617 ME          | U24                  | 3        |
| 74HC112             | U27 A,B              | 13       |
| LT1585              | VR1                  | 25       |
| LT1575              | VR2                  | 25       |
| Crystal (14.318MHz) | Y1                   | 5        |
| Crystal(32.768KHz)  | Y2                   | 13       |

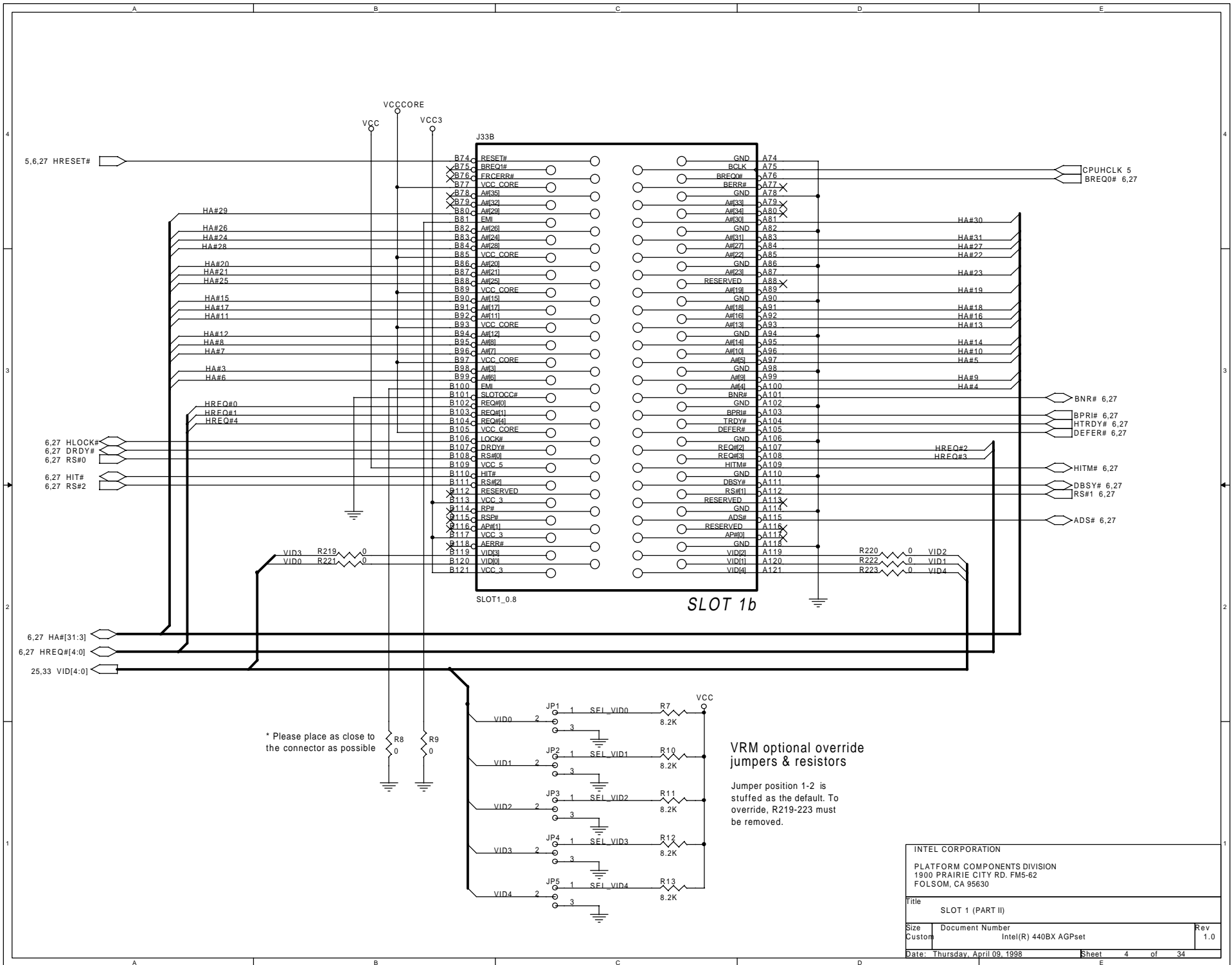
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Title  
 INTEL 100MHz Pentium(tm) II processor/440BX AGPset Block Diagram

Size Document Number  
 Custom Intel(R) 440BX AGPset Rev 1.0

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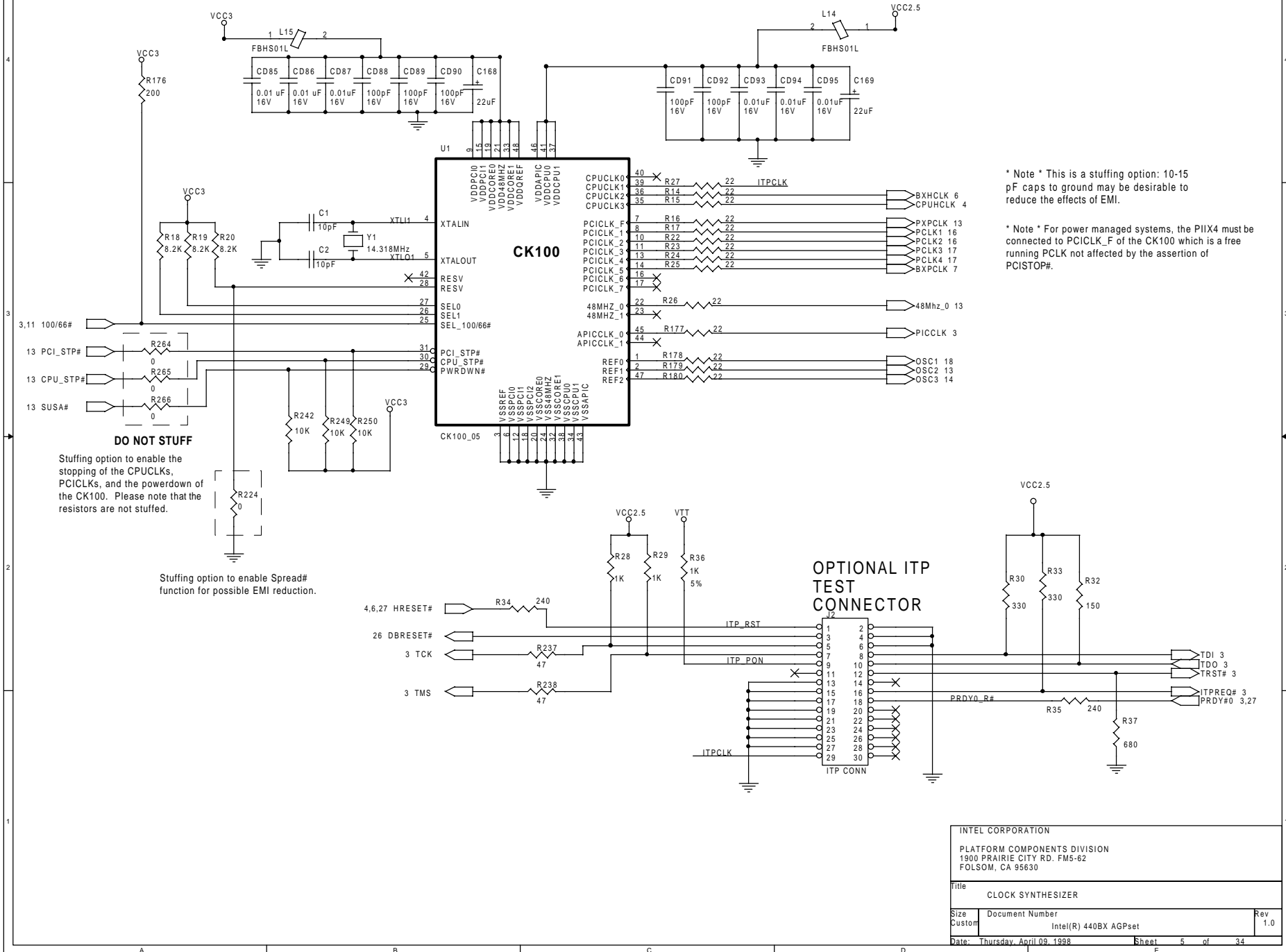


\* Please place as close to the connector as possible

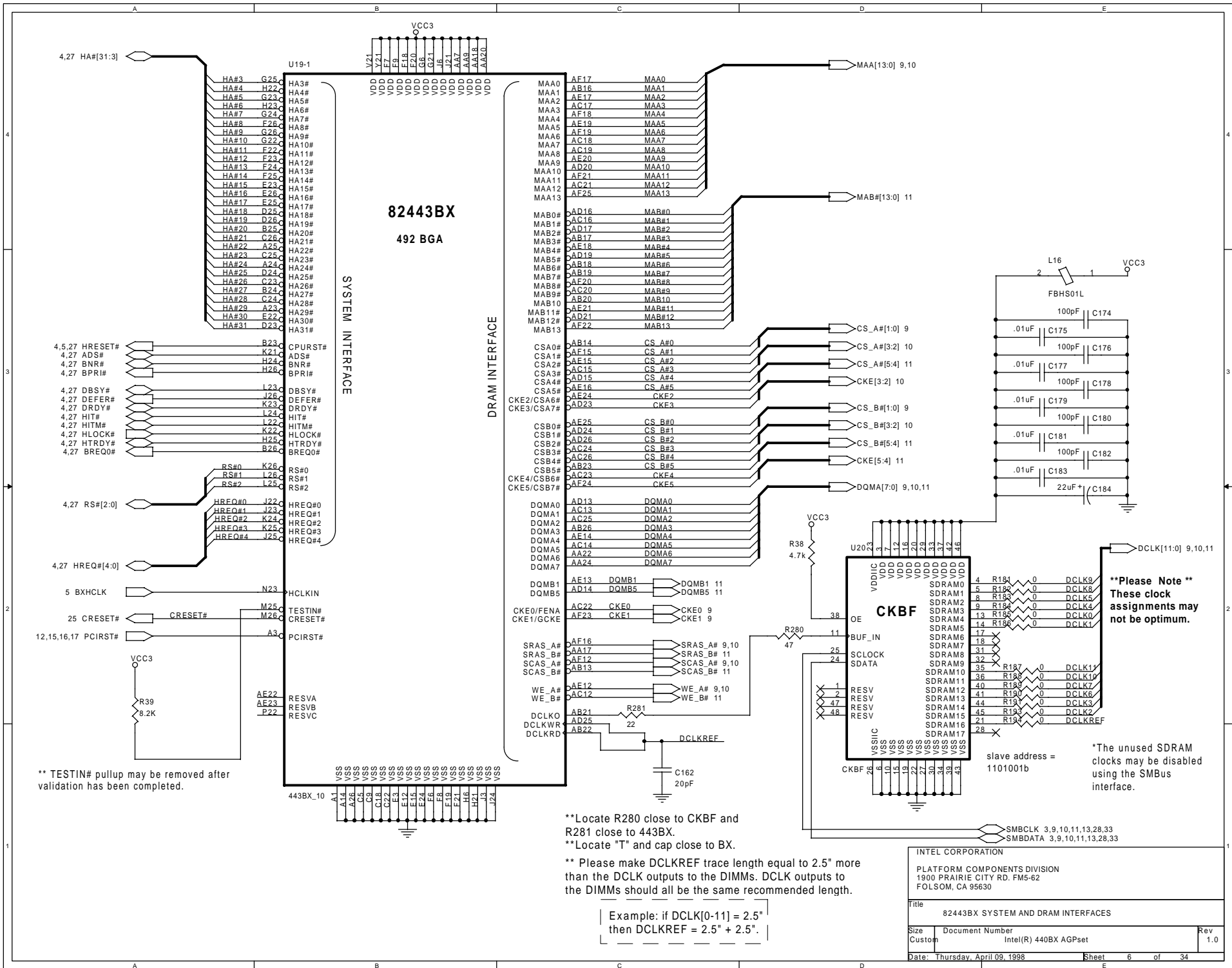
VRM optional override jumpers & resistors  
 Jumper position 1-2 is stuffed as the default. To override, R219-223 must be removed.

|                              |                          |               |
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| Title                        |                          |               |
| SLOT 1 (PART II)             |                          |               |
| Size                         | Document Number          | Rev           |
| Custom                       | Intel(R) 440BX AGPset    | 1.0           |
| Date:                        | Thursday, April 09, 1998 | Sheet 4 of 34 |

# CLOCK SYNTHESIZER



|                                |  |            |
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| Title<br>CLOCK SYNTHESIZER     |  |            |
| Size<br>Custom                 | Document Number<br>Intel(R) 440BX AGPset | Rev<br>1.0 |
| Date: Thursday, April 09, 1998 | Sheet                                    | 5 of 34    |



\*\* TESTIN# pullup may be removed after validation has been completed.

\*\*Locate R280 close to CKBF and R281 close to 443BX.  
 \*\*Locate "T" and cap close to BX.

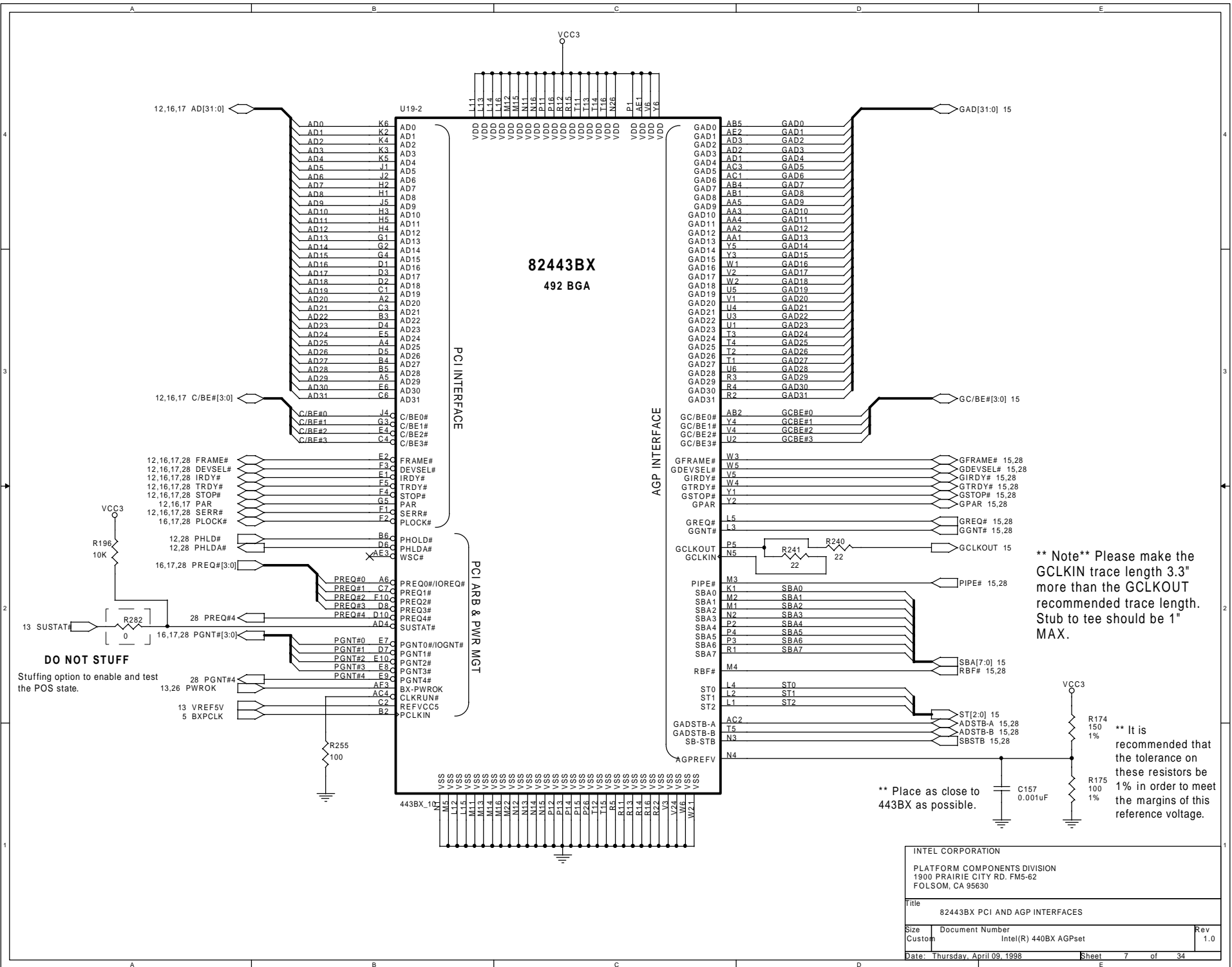
\*\* Please make DCLKREF trace length equal to 2.5" more than the DCLK outputs to the DIMMs. DCLK outputs to the DIMMs should all be the same recommended length.

Example: if DCLK[0-11] = 2.5"  
 then DCLKREF = 2.5" + 2.5".

**\*\*Please Note\*\***  
 These clock assignments may not be optimum.

\*The unused SDRAM clocks may be disabled using the SMBus interface.

|   |  |       |          |
|---|--|-------|----------|
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| FOLSOM, CA 95630                          |  |       |          |
| Title: 82443BX SYSTEM AND DRAM INTERFACES |  |       |          |
| Size: Custom                              | Document Number: Intel(R) 440BX AGPset |       | Rev: 1.0 |
| Date: Thursday, April 09, 1998            | Sheet: 6                               | of 34 |          |



**82443BX**  
492 BGA

PCI INTERFACE

AGP INTERFACE

PCI ARB & PWR MGT

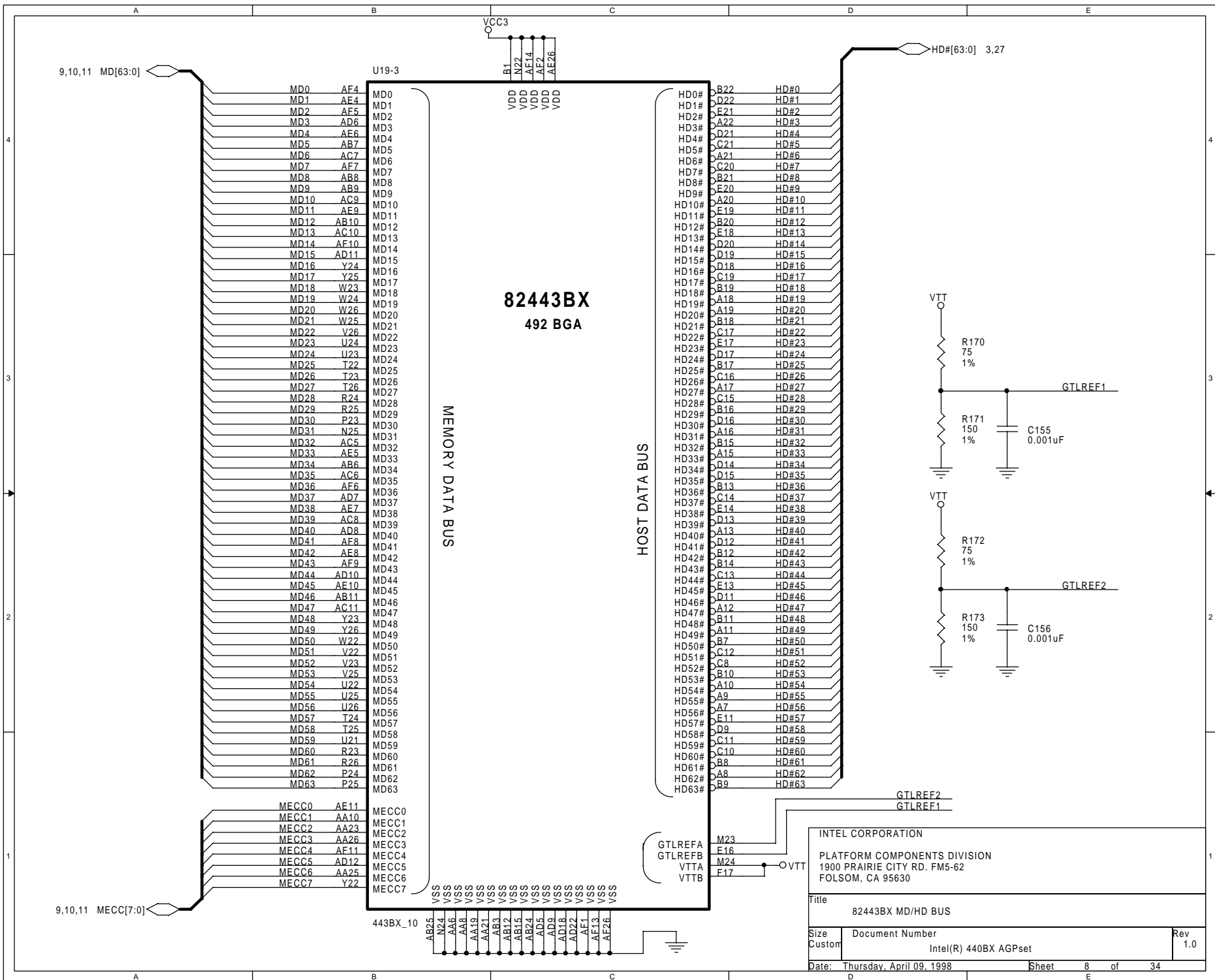
**\*\* Note\*\*** Please make the GCLKIN trace length 3.3" more than the GCLKOUT recommended trace length. Stub to tee should be 1" MAX.

**\*\* It is recommended that the tolerance on these resistors be 1% in order to meet the margins of this reference voltage.**

**\*\* Place as close to 443BX as possible.**

**DO NOT STUFF**  
Stuffing option to enable and test the POS state.

|                                |                          |       |         |
|--------------------------------|--------------------------|-------|---------|
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| Title                          |                          |       |         |
| 82443BX PCI AND AGP INTERFACES |                          |       |         |
| Size                           | Document Number          | Rev   |         |
| Custom                         | Intel(R) 440BX AGPset    | 1.0   |         |
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9,10,11 MD[63:0]

- MD0 AF4
- MD1 AF4
- MD2 AF5
- MD3 AD6
- MD4 AE6
- MD5 AB7
- MD6 AC7
- MD7 AF7
- MD8 AB8
- MD9 AB9
- MD10 AC9
- MD11 AE9
- MD12 AB10
- MD13 AC10
- MD14 AF10
- MD15 AD11
- MD16 Y24
- MD17 Y25
- MD18 W23
- MD19 W24
- MD20 W26
- MD21 W25
- MD22 V26
- MD23 U24
- MD24 U23
- MD25 T22
- MD26 T23
- MD27 T26
- MD28 R24
- MD29 R25
- MD30 P23
- MD31 N25
- MD32 AC5
- MD33 AE5
- MD34 AB6
- MD35 AC6
- MD36 AF6
- MD37 AD7
- MD38 AE7
- MD39 AC8
- MD40 AD8
- MD41 AE8
- MD42 AE8
- MD43 AF9
- MD44 AD10
- MD45 AE10
- MD46 AB11
- MD47 AC11
- MD48 Y23
- MD49 Y26
- MD50 W22
- MD51 V22
- MD52 V23
- MD53 V25
- MD54 U22
- MD55 U25
- MD56 U26
- MD57 T24
- MD58 T25
- MD59 U21
- MD60 R23
- MD61 R26
- MD62 P24
- MD63 P25

- MECC0 AE11
- MECC1 AA10
- MECC2 AA23
- MECC3 AA26
- MECC4 AF11
- MECC5 AD12
- MECC6 AA25
- MECC7 Y22

9,10,11 MECC[7:0]

**82443BX**  
492 BGA

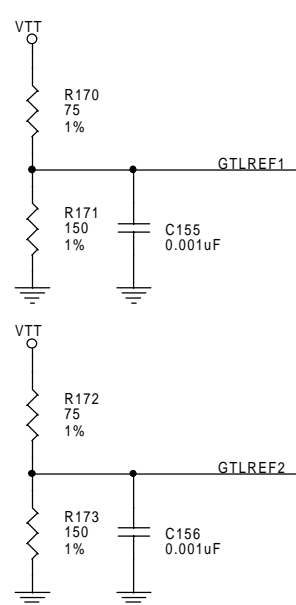
MEMORY DATA BUS

HOST DATA BUS

443BX\_10

- VSS AB25
- VSS N24
- VSS AA6
- VSS AA8
- VSS AA9
- VSS AA19
- VSS AA21
- VSS AB3
- VSS AB12
- VSS AB15
- VSS AB24
- VSS AD5
- VSS AD9
- VSS AD18
- VSS AD22
- VSS AF1
- VSS AF13
- VSS AF26
- VSS

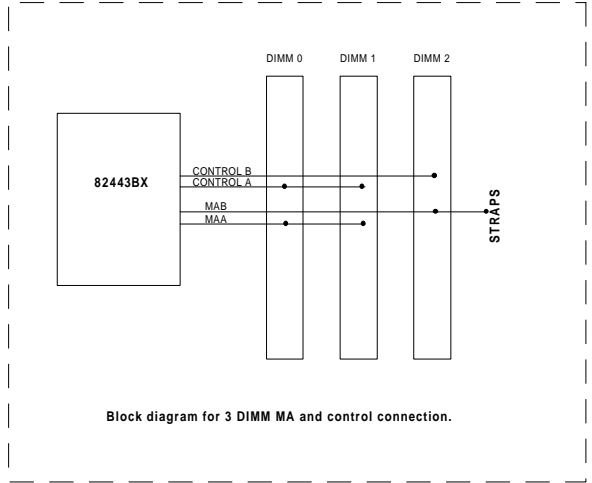
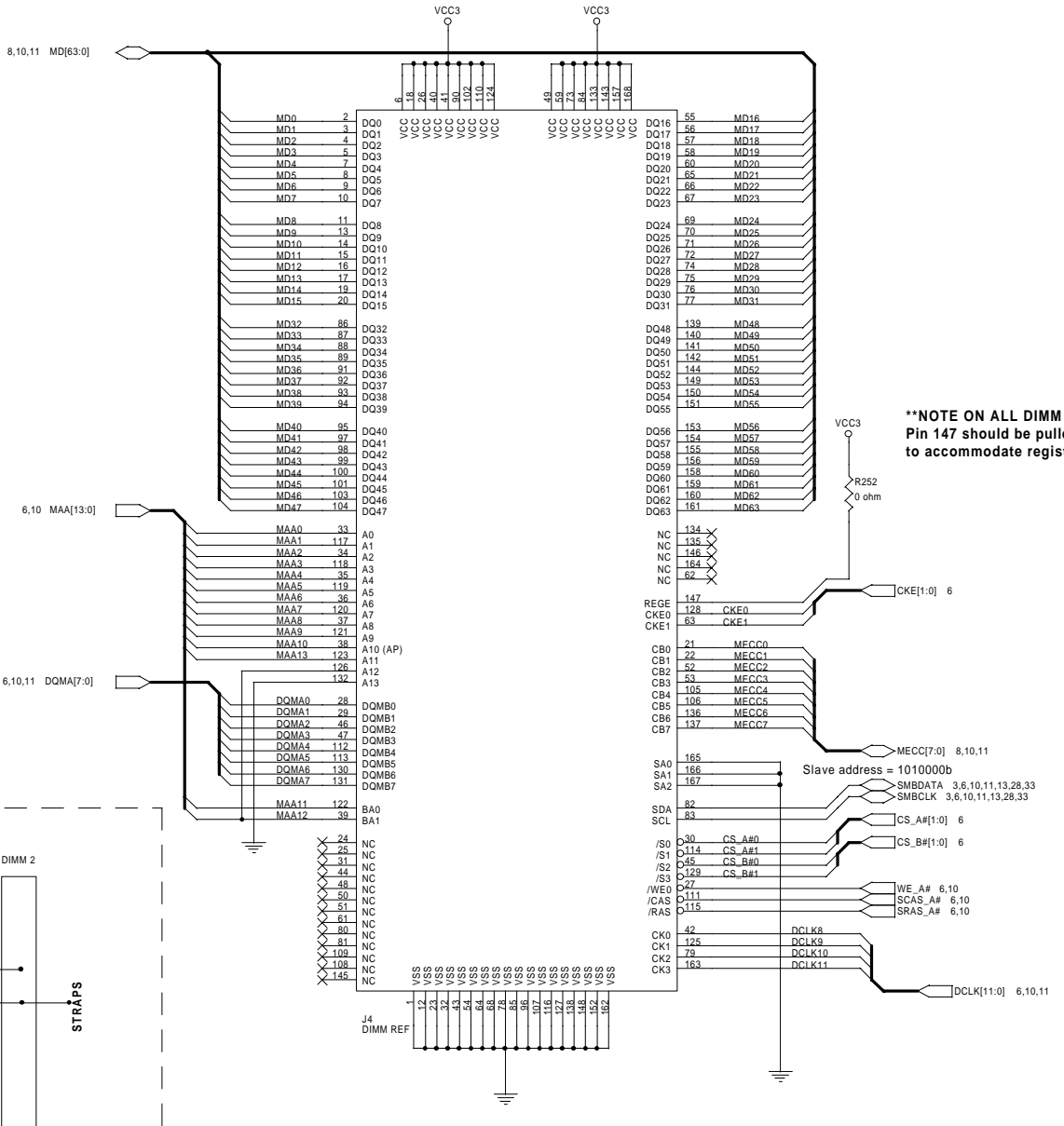
- VCC3
- B1
- N22
- AF14
- AF2
- AF26
- VDD
- VDD
- VDD
- VDD
- VDD



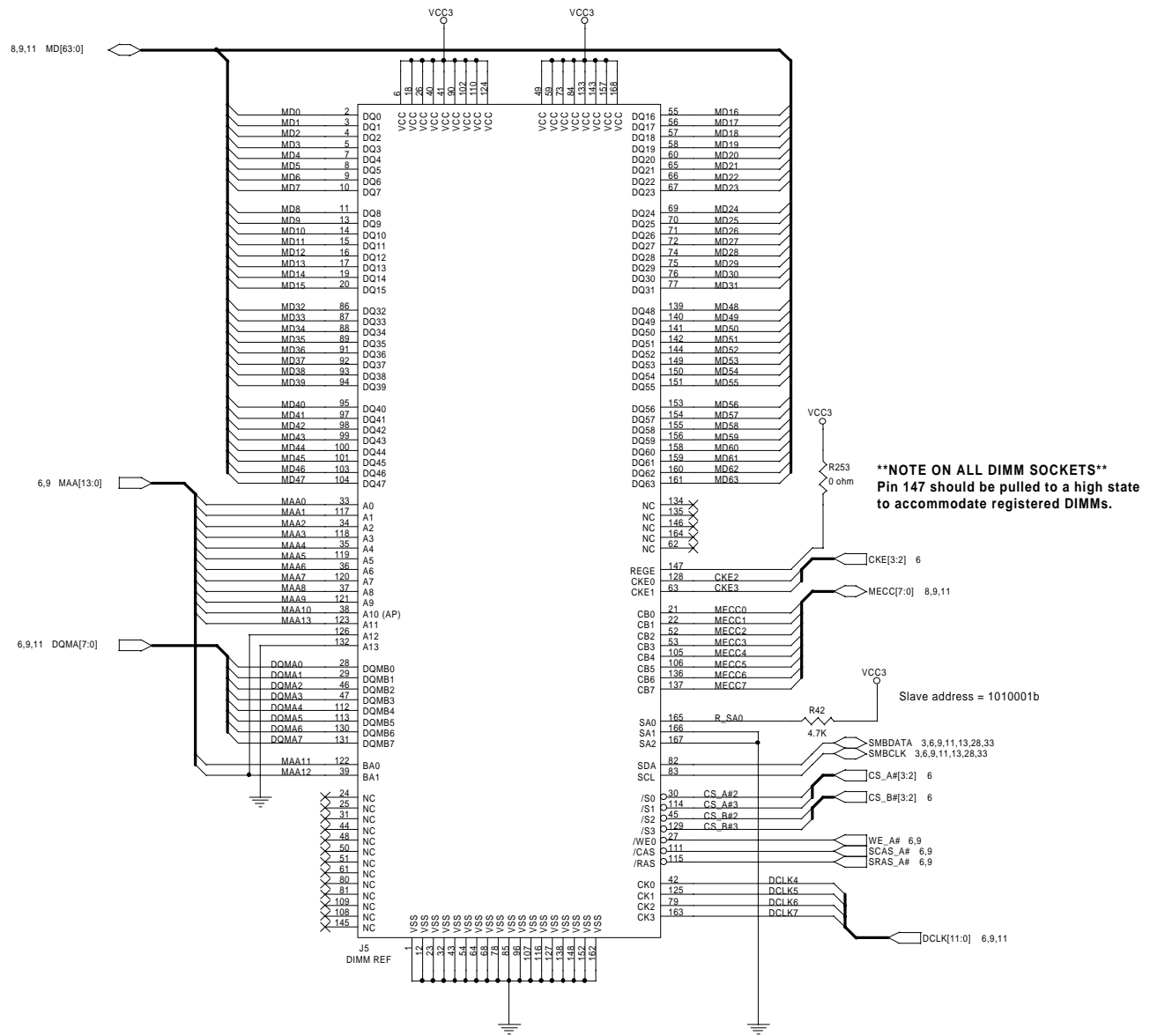
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| Title: 82443BX MD/HD BUS  |  |          |
| Size: Custom  | Document Number: Intel(R) 440BX AGPset | Rev: 1.0 |
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# DIMM SOCKET 0



# DIMM SOCKET 1

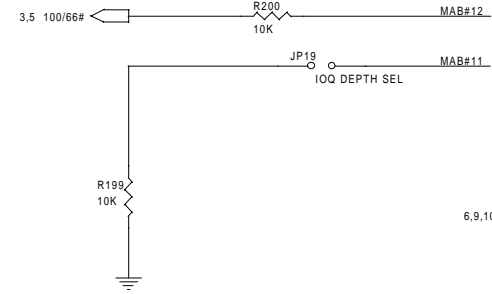
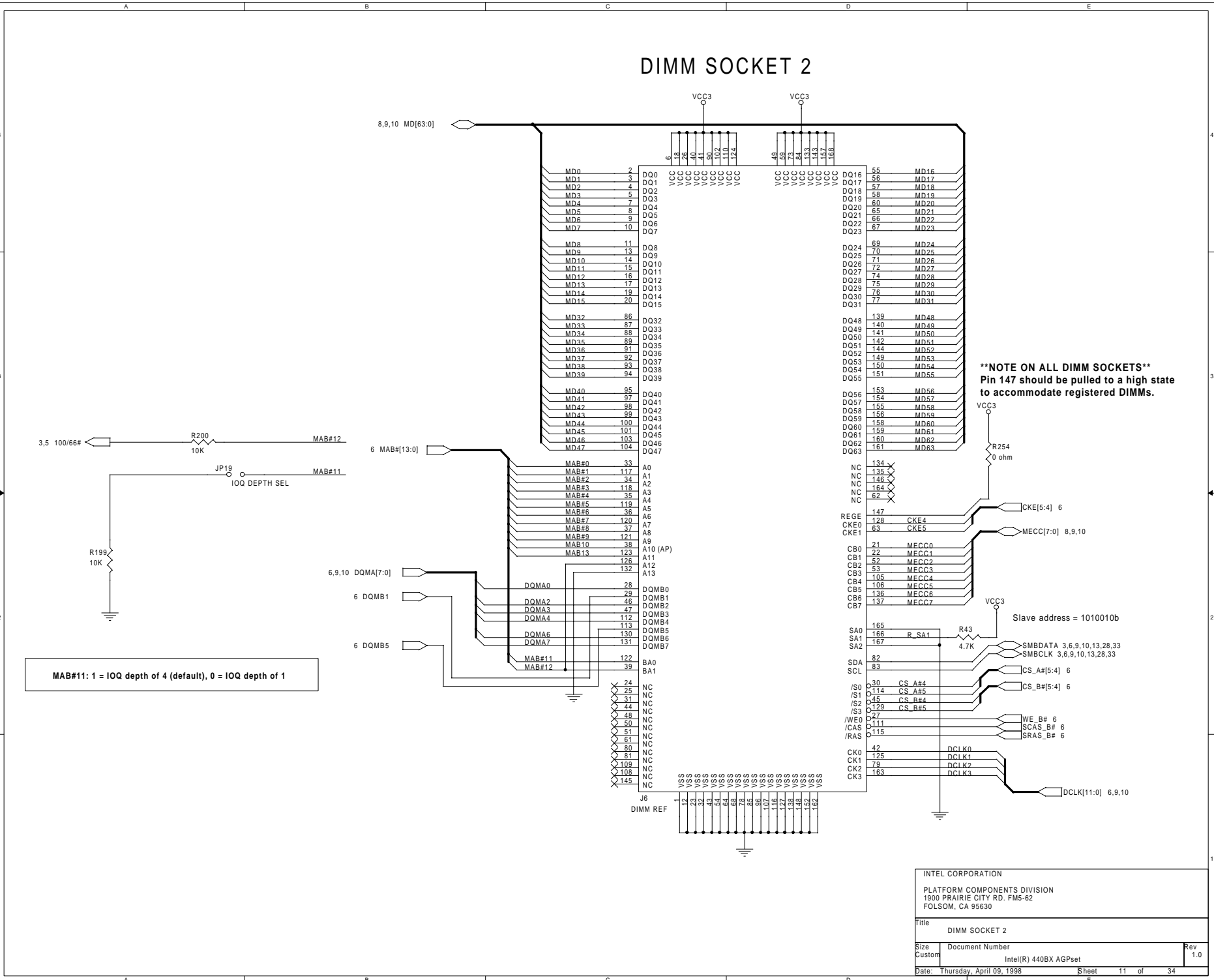


**\*\*NOTE ON ALL DIMM SOCKETS\*\***  
**Pin 147 should be pulled to a high state**  
**to accommodate registered DIMMs.**

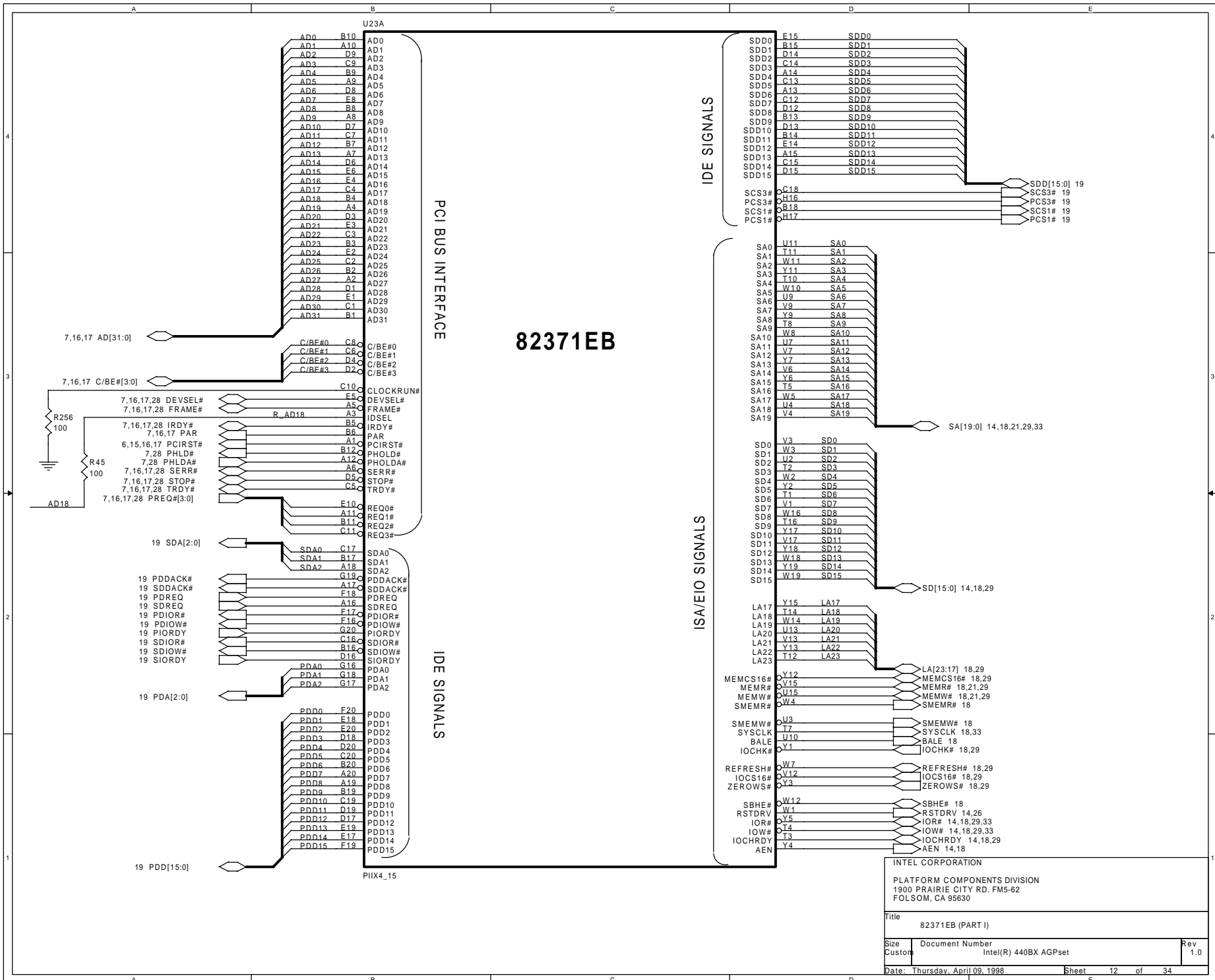
Slave address = 1010001b

|                              |                          |               |          |
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| Title                        |                          | DIMM SOCKET 1 |          |
| Size                         | Document Number          | Rev           | 1.0      |
| Custom                       | Intel(R) 440BX AGPset    |               |          |
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# DIMM SOCKET 2



MAB#11: 1 = IOQ depth of 4 (default), 0 = IOQ depth of 1



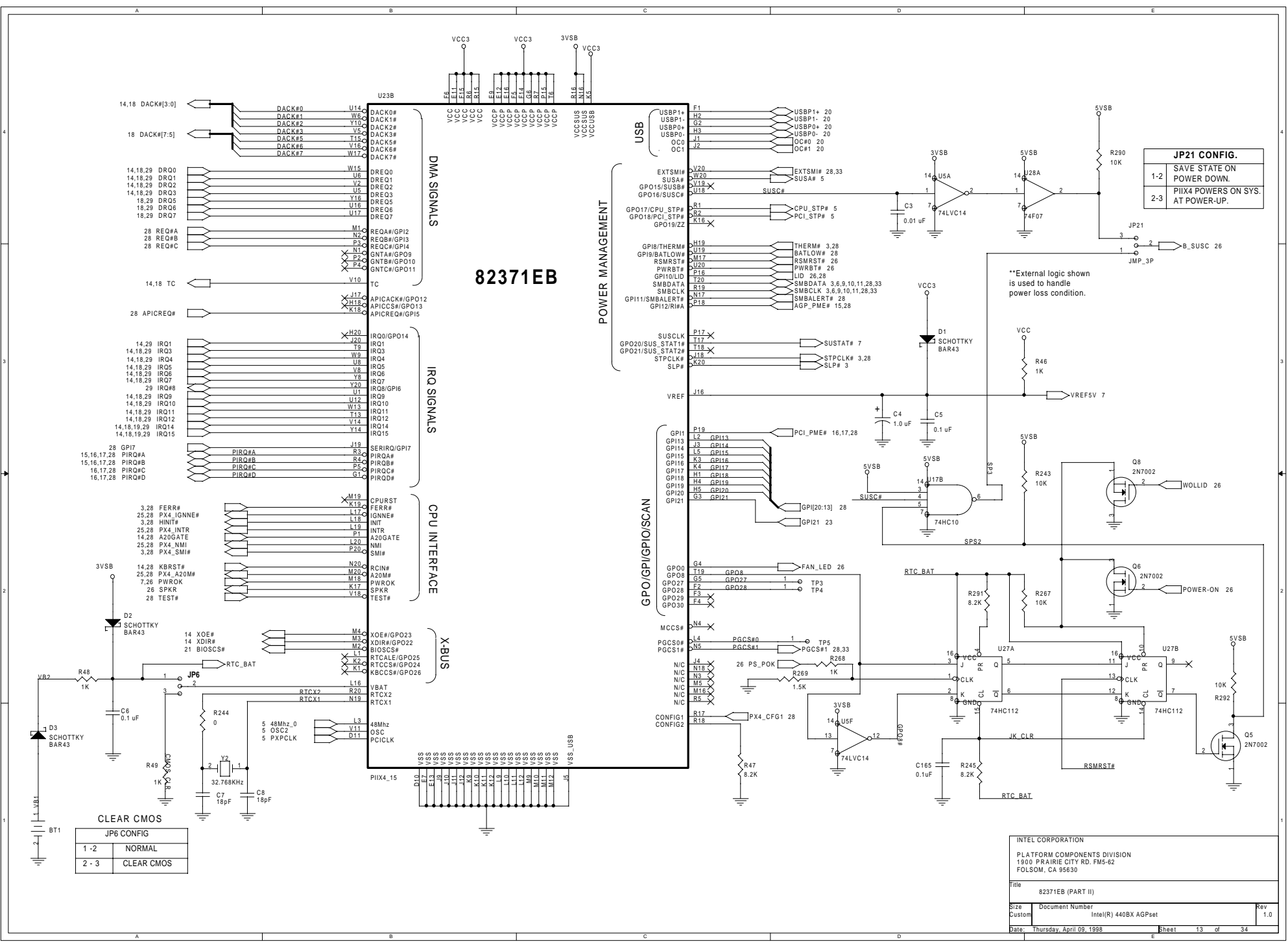
82371EB

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Title: 82371EB (PART I)

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**82371EB**

| JP21 CONFIG. |                                   |
|--------------|-----------------------------------|
| 1-2          | SAVE STATE ON POWER DOWN.         |
| 2-3          | PIIX4 POWERS ON SYS. AT POWER-UP. |

**CLEAR CMOS**

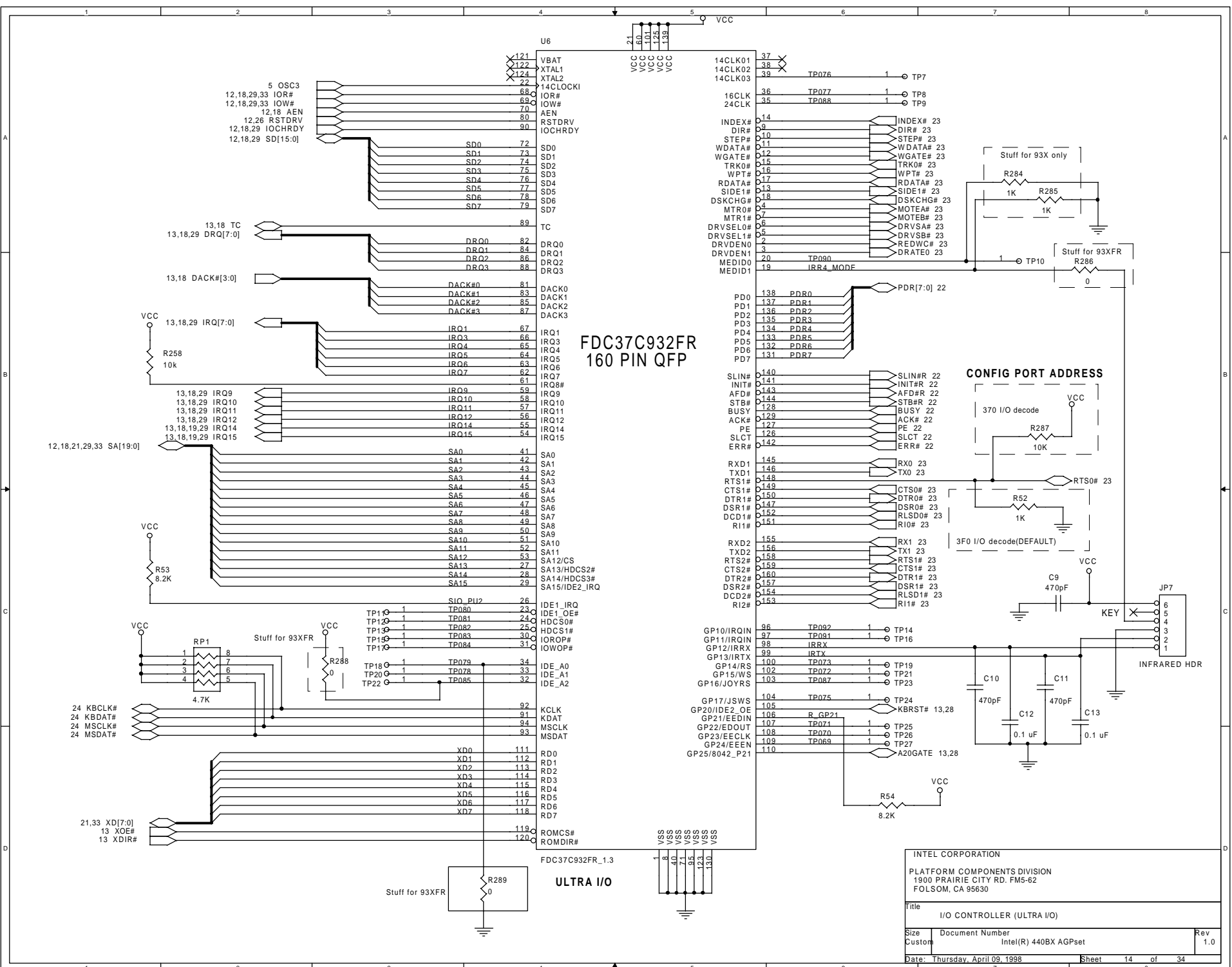
| JP6 CONFIG |            |
|------------|------------|
| 1 - 2      | NORMAL     |
| 2 - 3      | CLEAR CMOS |

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Title: 82371EB (PART II)

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**FDC37C932FR  
160 PIN QFP**

**CONFIG PORT ADDRESS**

**ULTRA I/O**

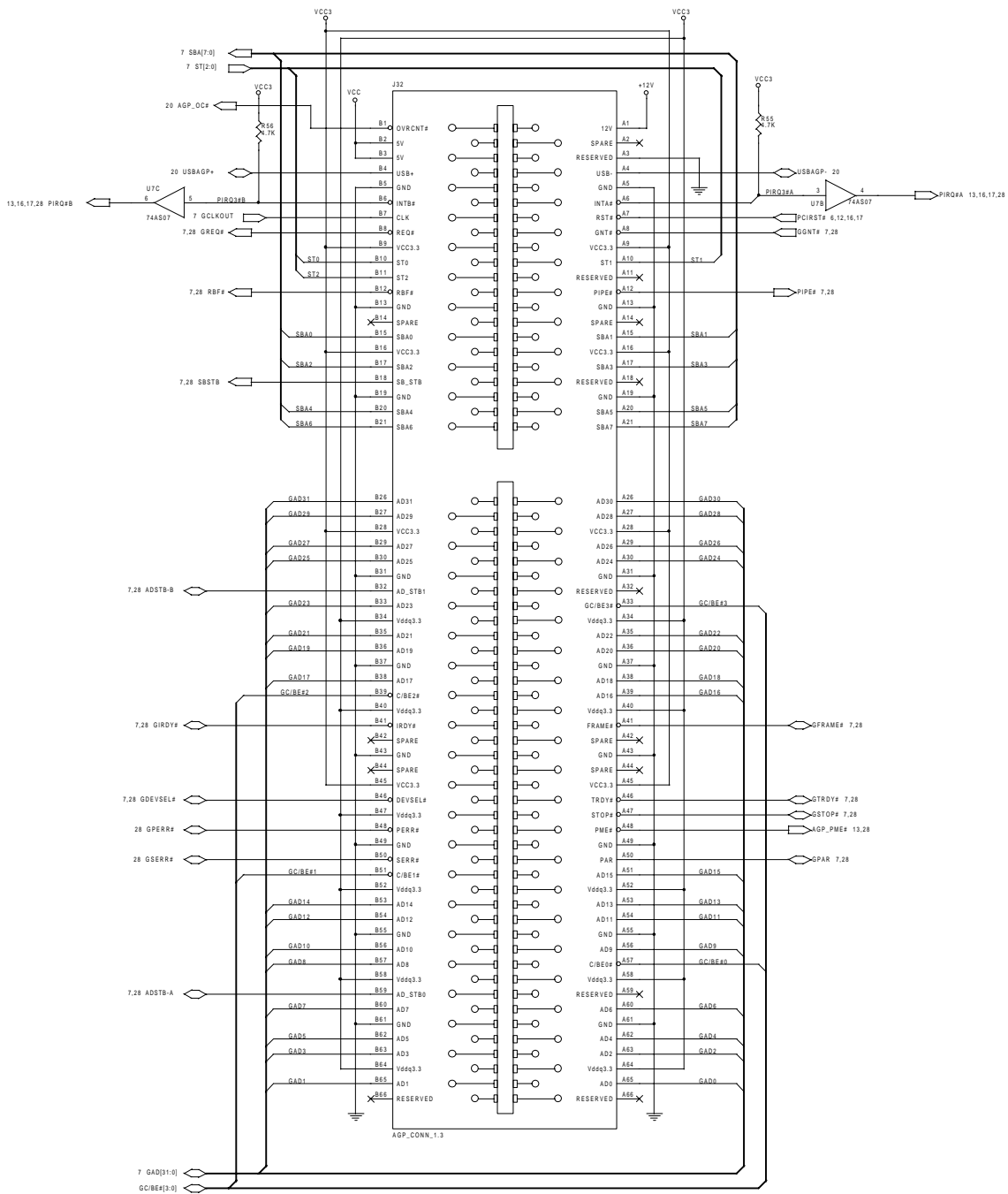
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Title: I/O CONTROLLER (ULTRA I/O)

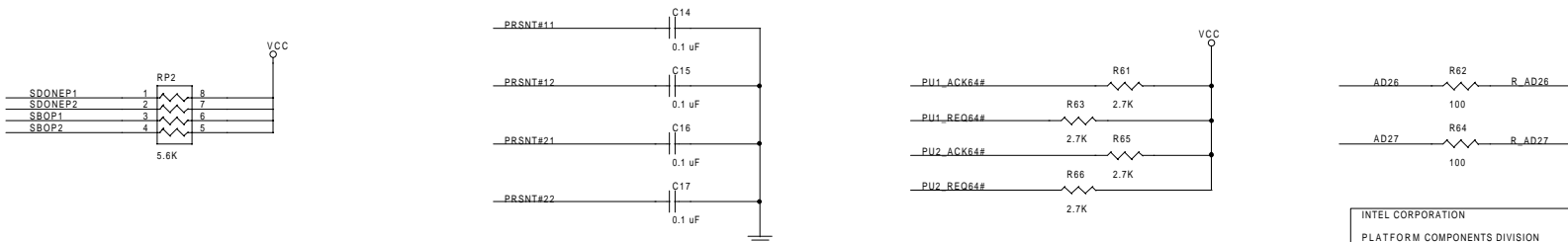
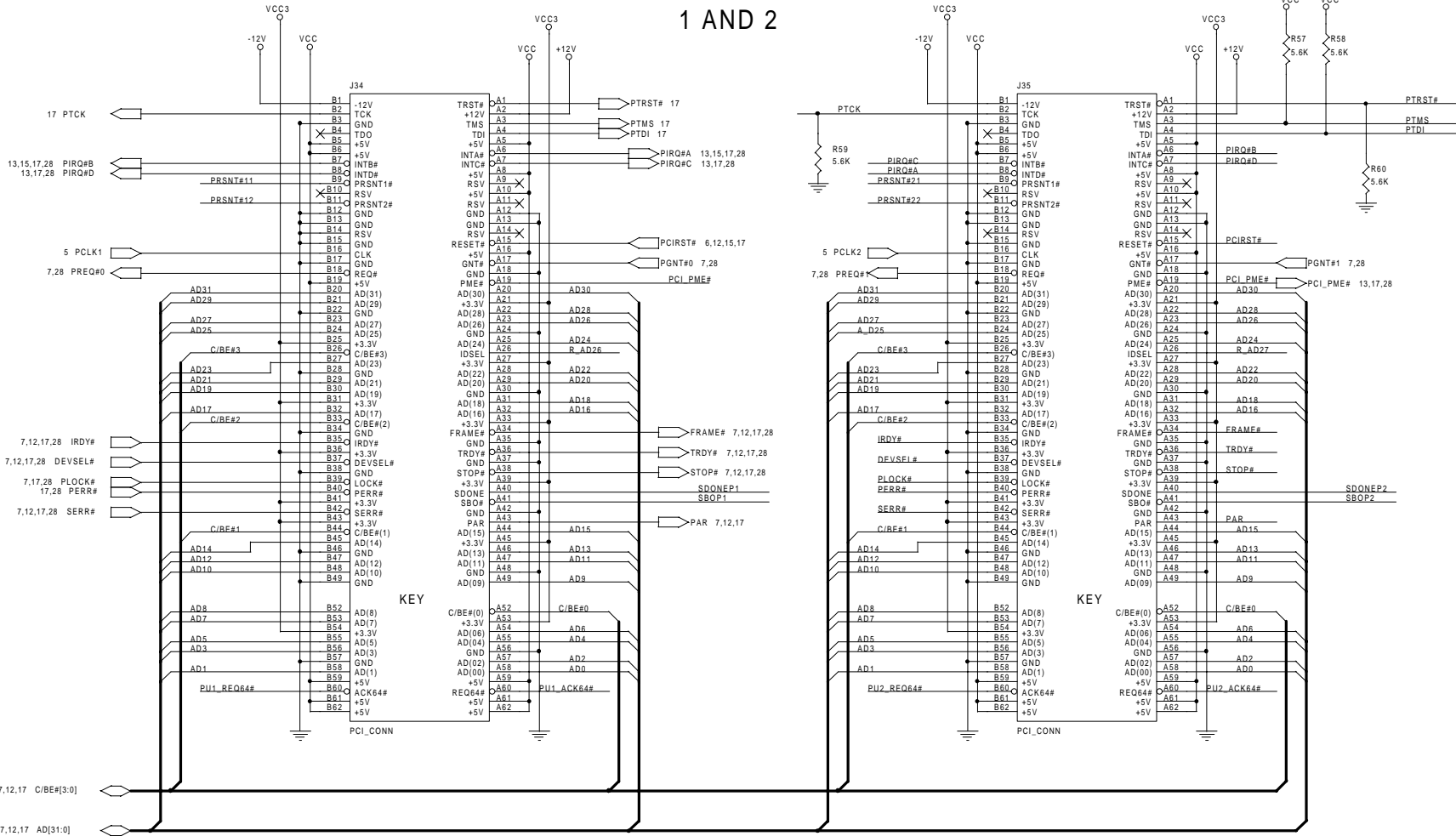
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|--------|-----------------------|-----|
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# AGP CONNECTOR



# PCI CONNECTORS 1 AND 2



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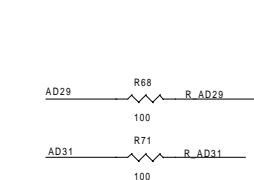
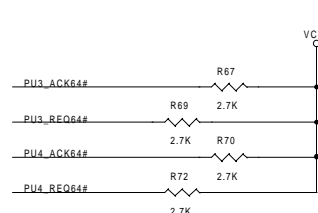
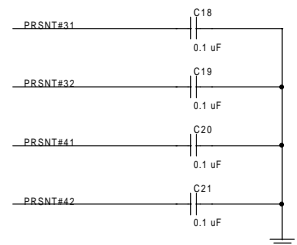
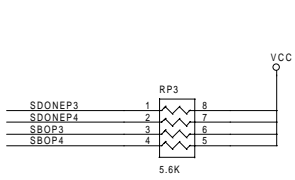
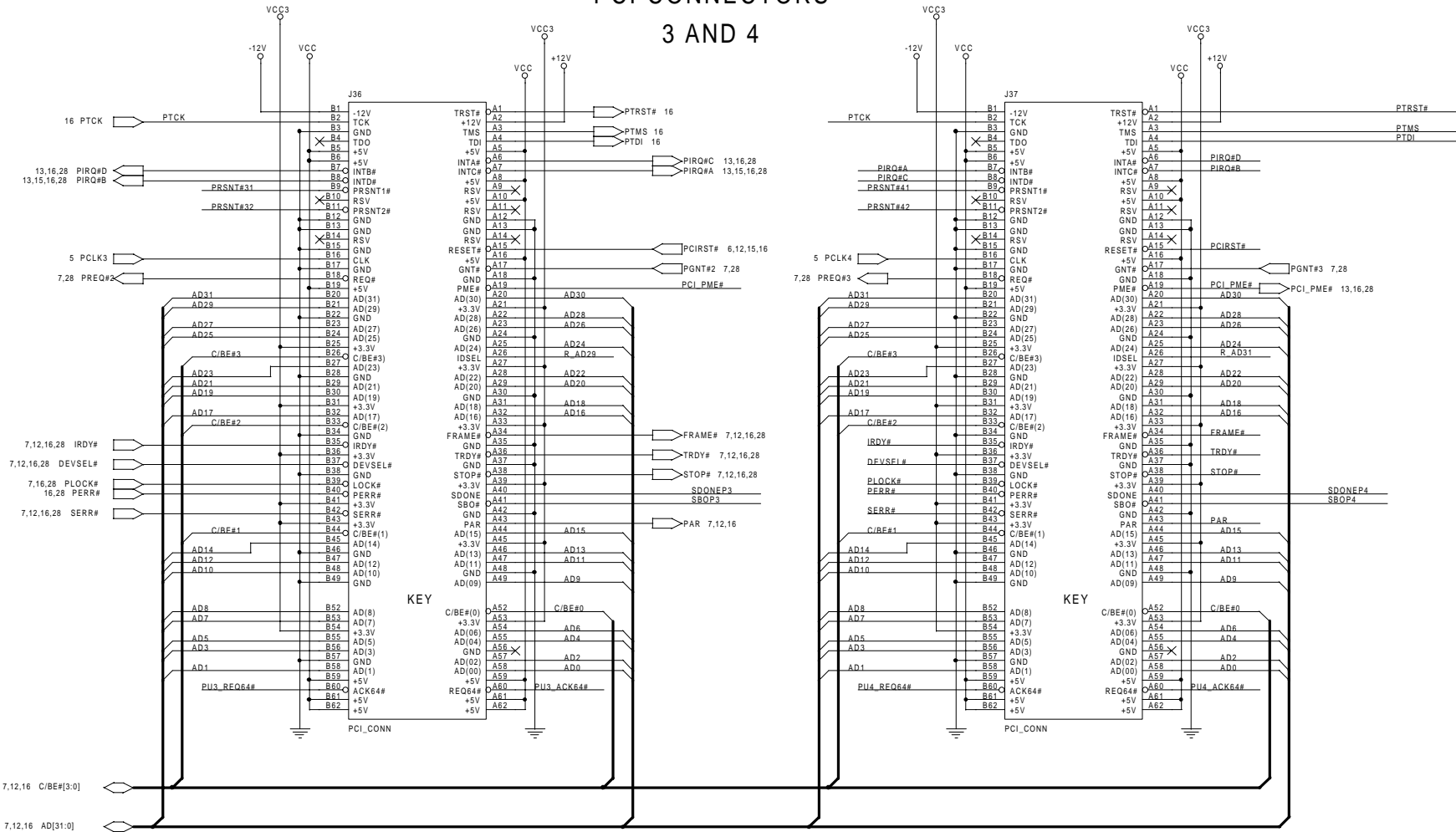
Title: PCI CONNECTORS 1 & 2

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# PCI CONNECTORS 3 AND 4



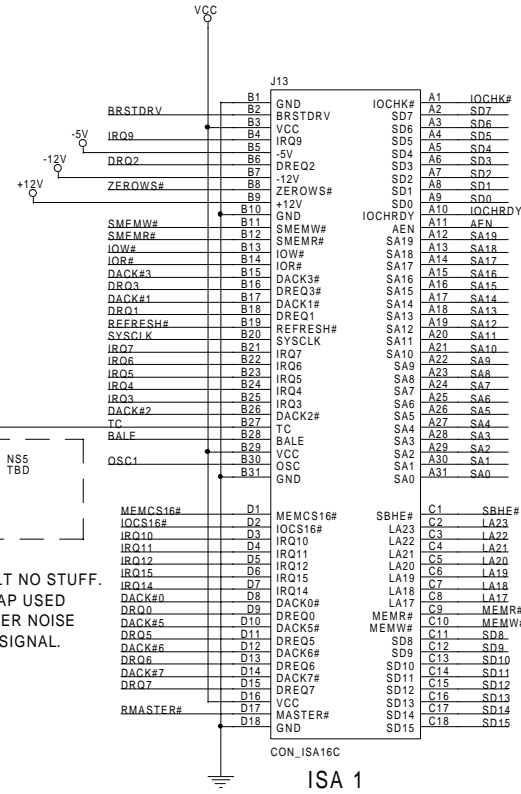
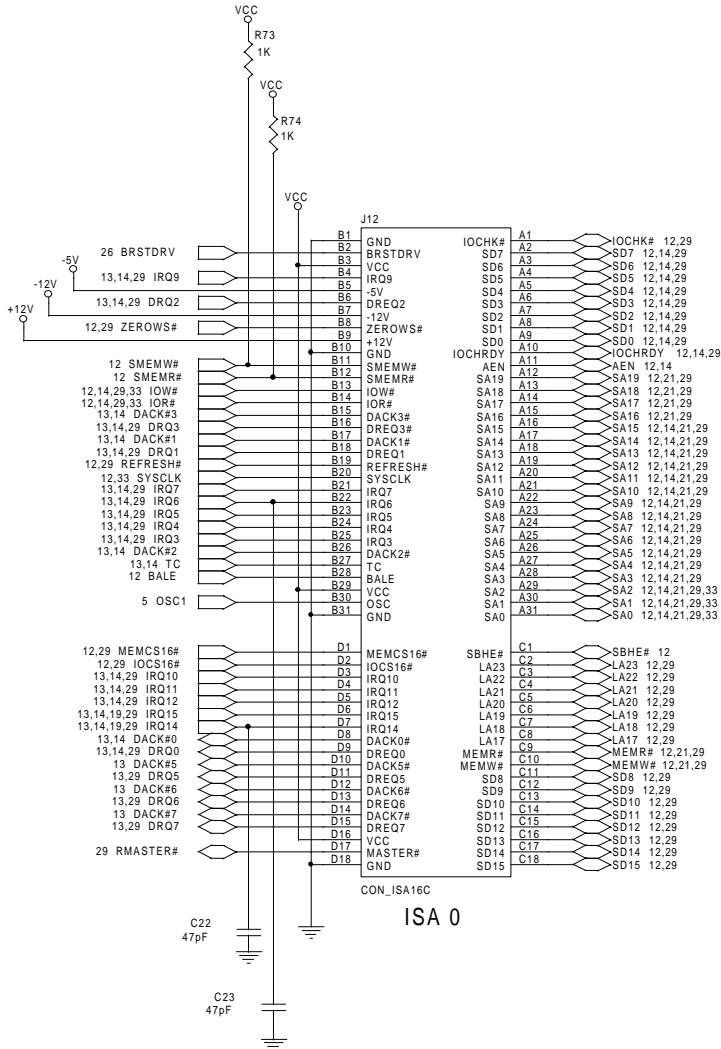
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Title: PCI CONNECTORS 3 & 4

Size: Custom Document Number: Intel(R) 440BX AGPset Rev: 1.0

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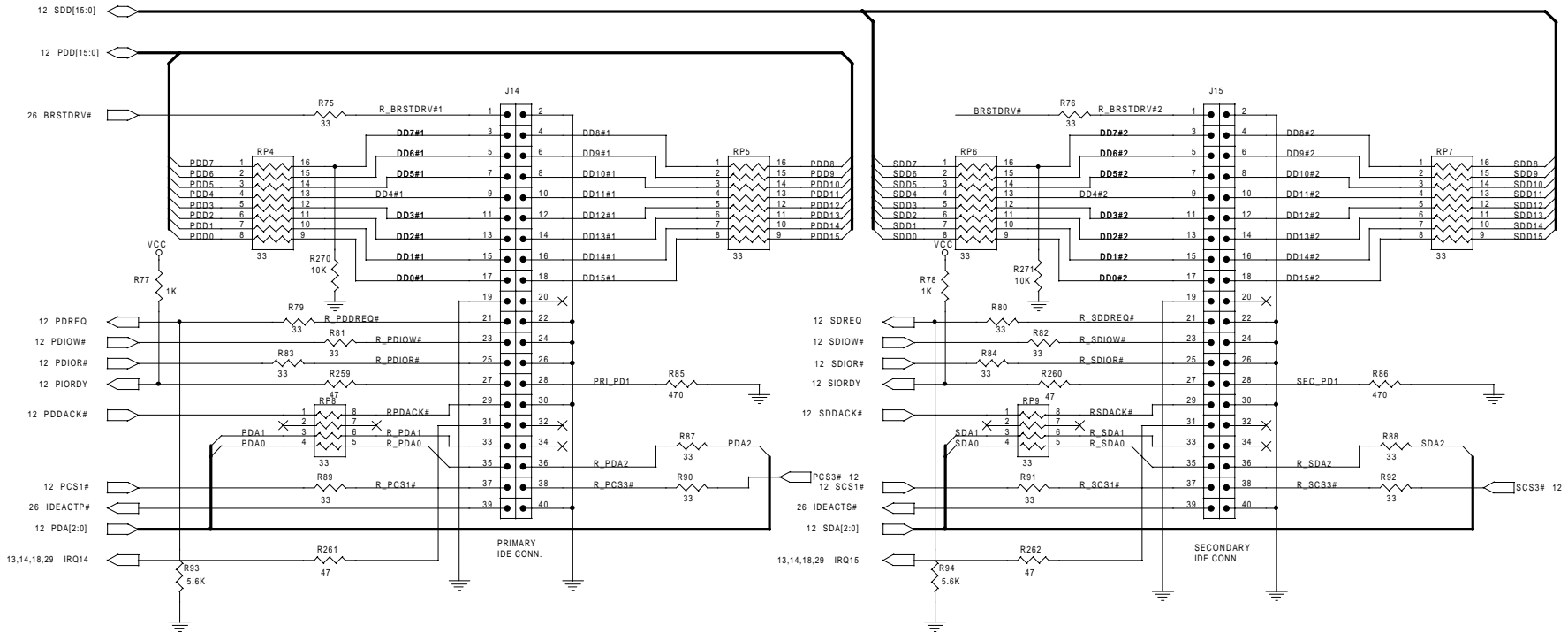
# ISA SLOTS



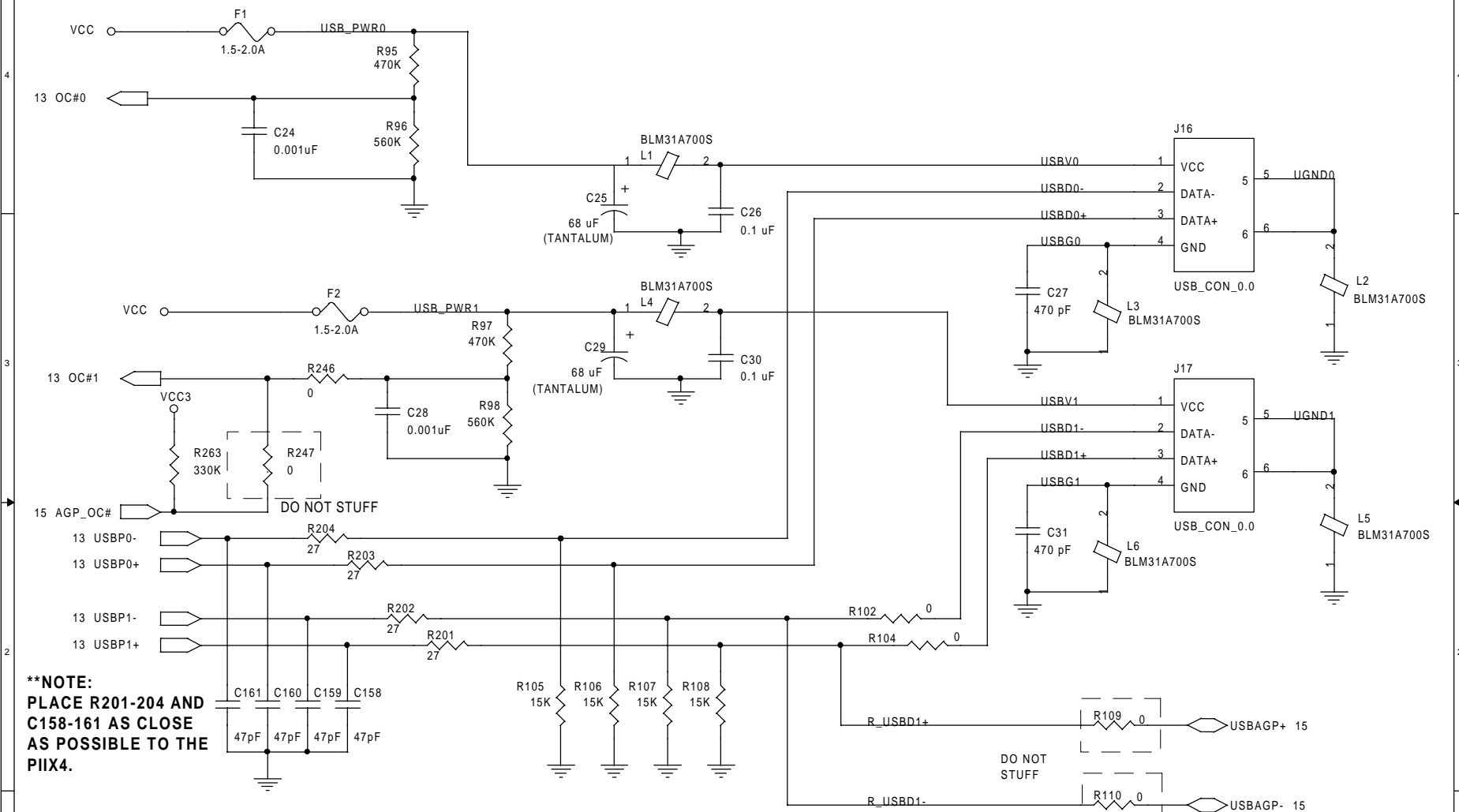
NOTE : DEFAULT NO STUFF.  
THIS CAP USED  
TO FILTER NOISE  
ON TC SIGNAL.

|                                |  |            |  |
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| Title<br>ISA SLOTS             |  |            |  |
| Size<br>Custom                 | Document Number<br>Intel(R) 440BX AGPset | Rev<br>1.0 |  |
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# IDE CONNECTORS



# USB CONNECTORS



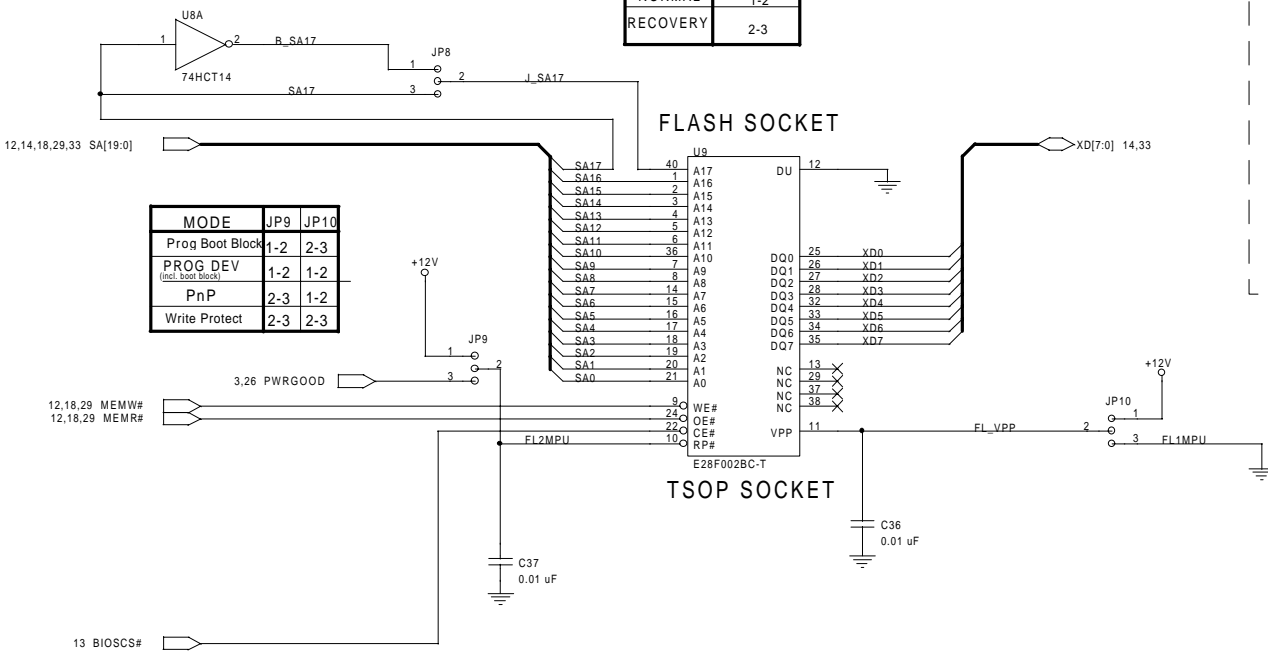
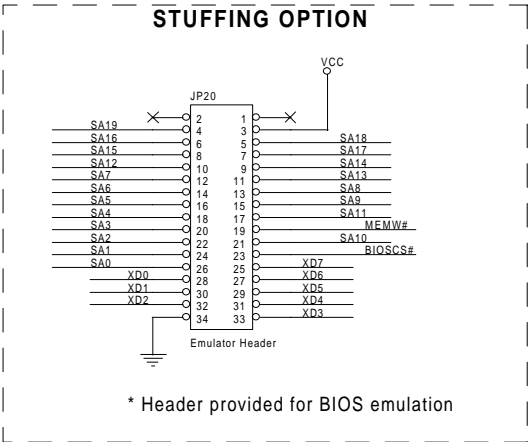
**\*\*NOTE:**  
**PLACE R201-204 AND**  
**C158-161 AS CLOSE**  
**AS POSSIBLE TO THE**  
**PIIX4.**

NOTE:  
 USE PIIX4  
 APPLICATION NOTE  
 FOR LAYOUT  
 GUIDELINES

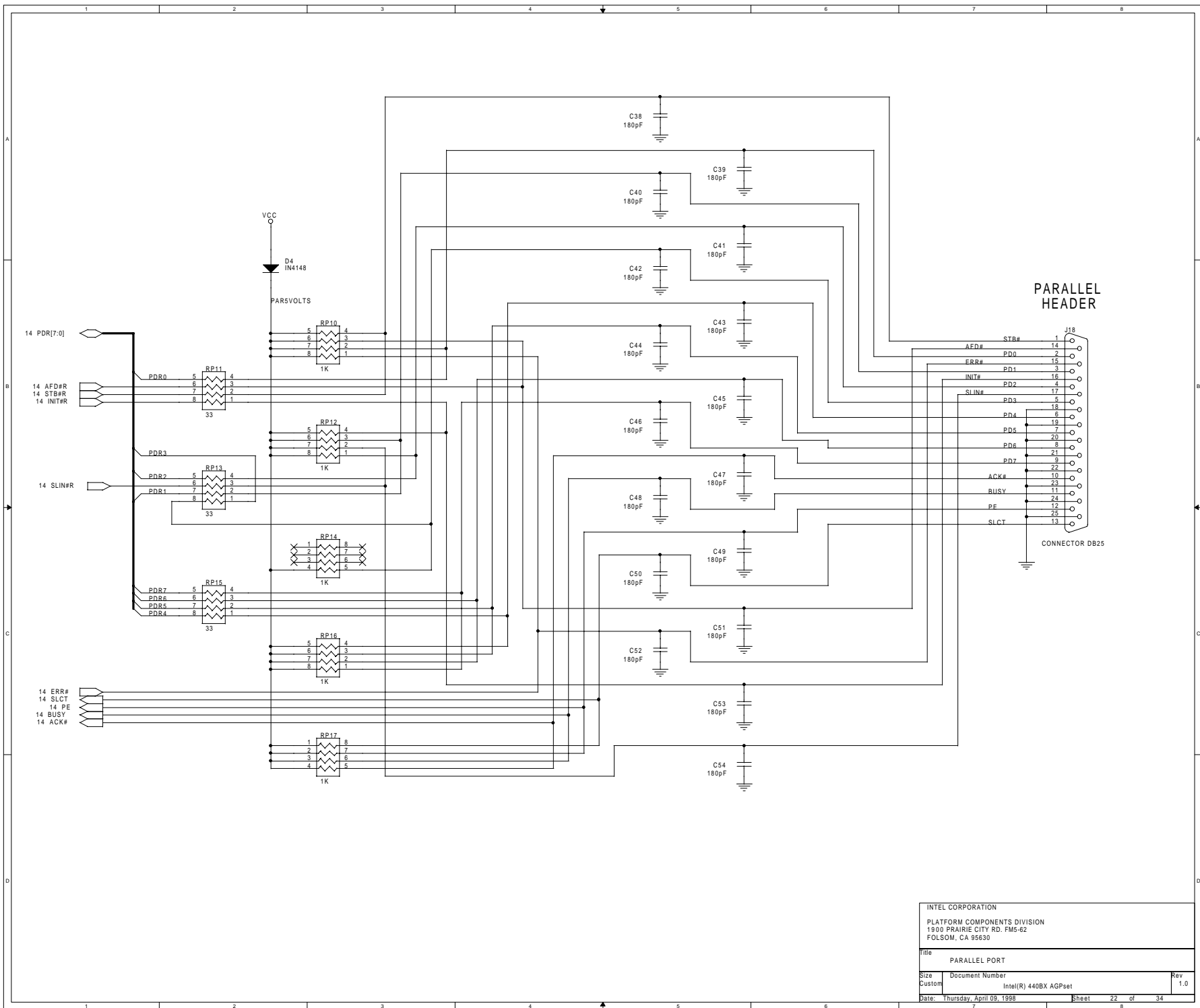
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| Title<br>USB HEADER  |  |            |
| Size<br>Custom   | Document Number<br>Intel(R) 440BX AGPset | Rev<br>1.0 |
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# SYSTEM ROM

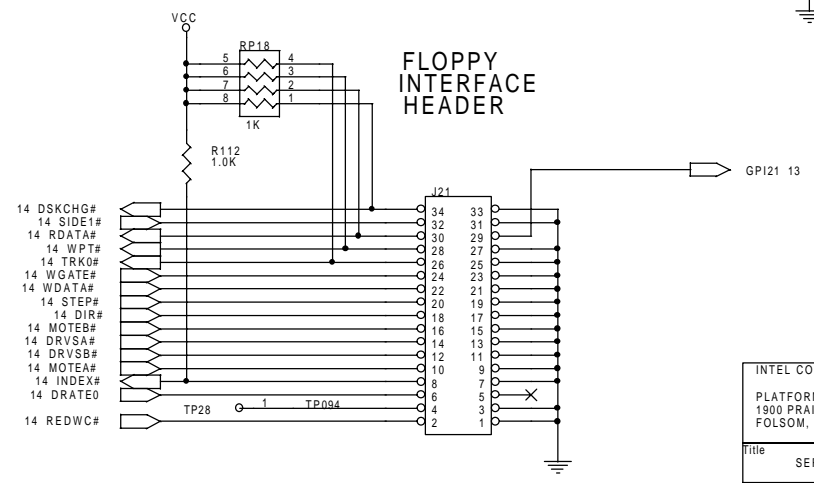
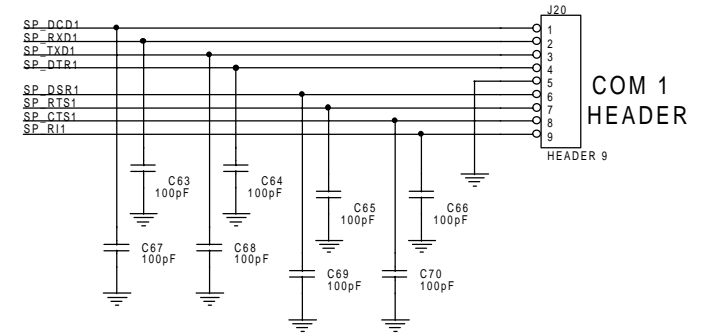
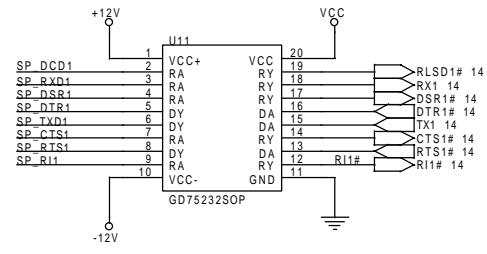
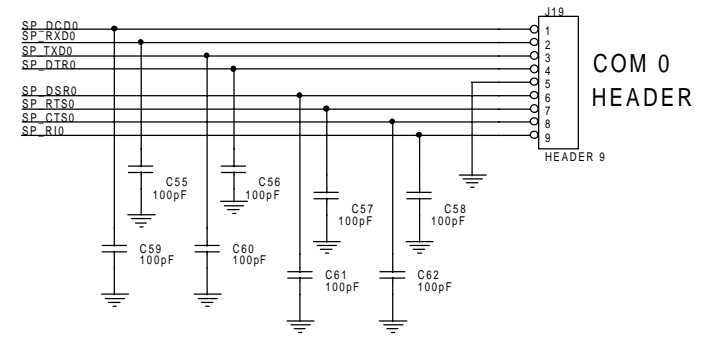
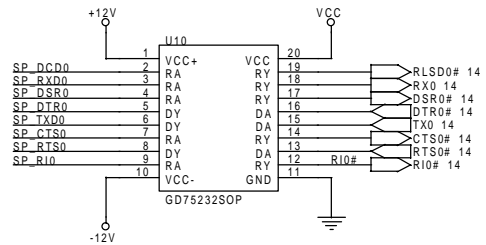
| MODE     | JP8 |
|----------|-----|
| NORMAL   | 1-2 |
| RECOVERY | 2-3 |



| MODE                        | JP9 | JP10 |
|-----------------------------|-----|------|
| Prog Boot Block             | 1-2 | 2-3  |
| PROG DEV (incl. boot block) | 1-2 | 1-2  |
| PnP                         | 2-3 | 1-2  |
| Write Protect               | 2-3 | 2-3  |

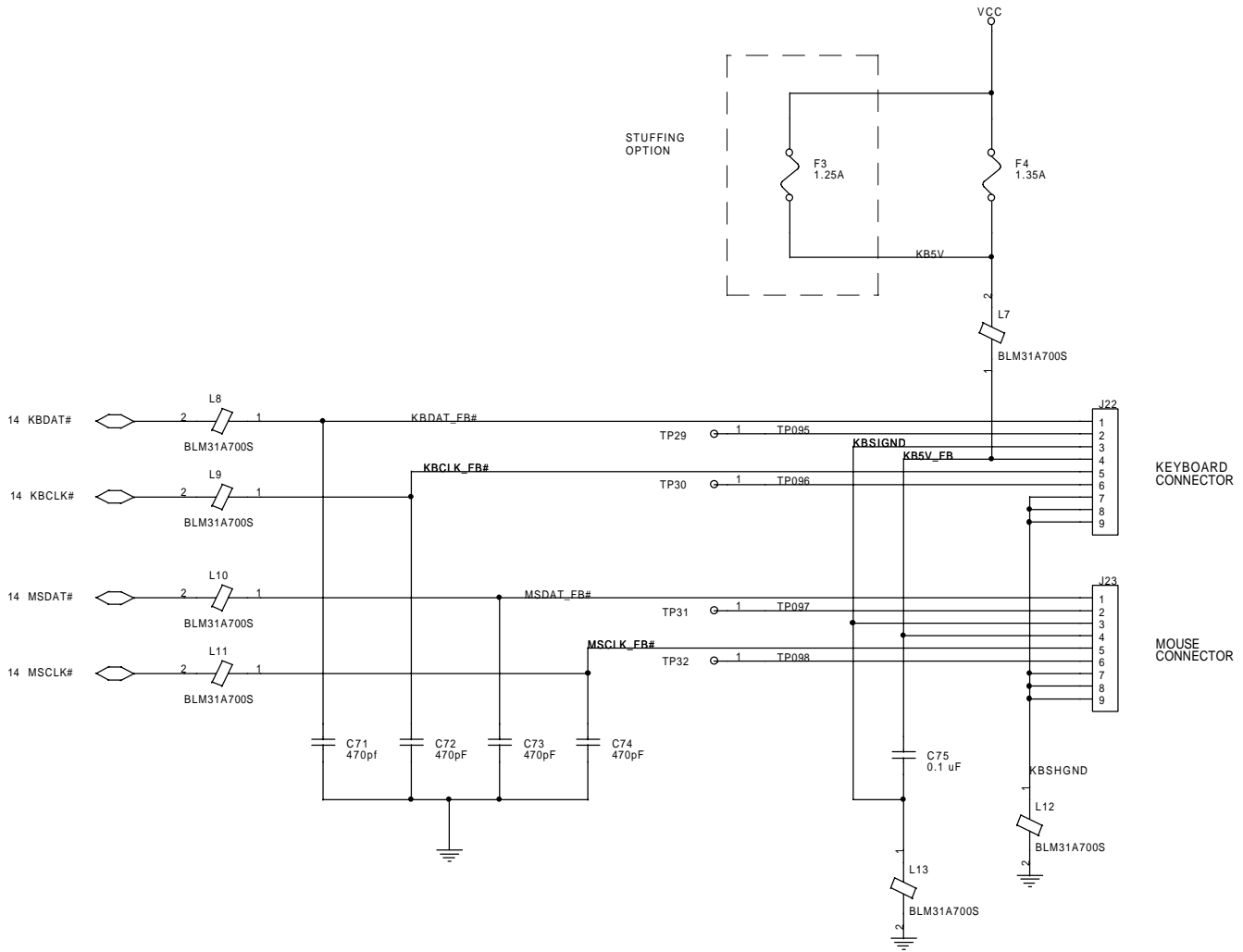


|                                |                                       |         |
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| FOLSOM, CA 95630               |                                       |         |
| Title PARALLEL PORT            |                                       |         |
| Size Custom                    | Document Number Intel(R) 440BX AGPset | Rev 1.0 |
| Date: Thursday, April 09, 1998 | Sheet 22 of 34                        |         |



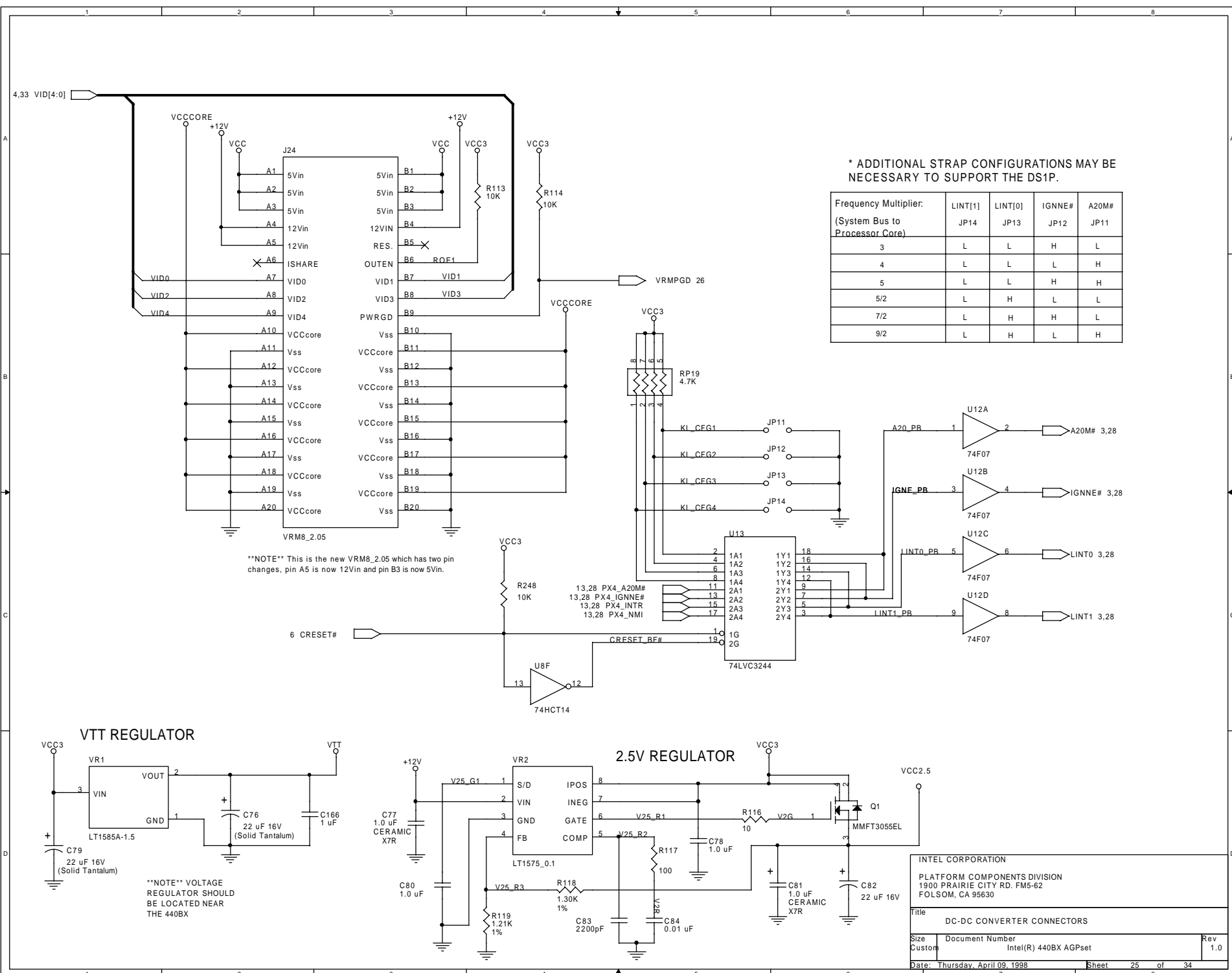
\*\* Connected to GPI21 of the PIIX4 for BIOS detection of a floppy drive.

|                                |                                       |         |
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| Title SERIAL AND FLOPPY        |                                       |         |
| Size Custom                    | Document Number Intel(R) 440BX AGPset | Rev 1.0 |
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|                              |                          |                |
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| FOLSOM, CA 95630             |                          |                |
| Title                        |                          |                |
| KEYBOARD/MOUSE INTERFACE     |                          |                |
| Size                         | Document Number          | Rev            |
| Custom                       | Intel(R) 440BX AGPset    | 1.0            |
| Date:                        | Thursday, April 09, 1998 | Sheet 24 of 34 |



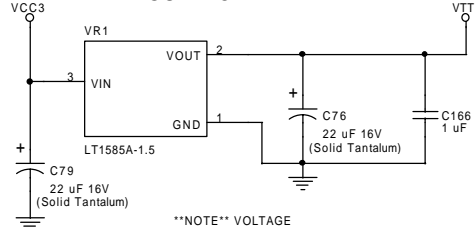


\* ADDITIONAL STRAP CONFIGURATIONS MAY BE NECESSARY TO SUPPORT THE DS1P.

| Frequency Multiplier:<br>(System Bus to<br>Processor Core) | LINT[1]<br>JP14 | LINT[0]<br>JP13 | IGNNE#<br>JP12 | A20M#<br>JP11 |
|--|-----------------|-----------------|----------------|---------------|
| 3  | L               | L               | H              | L             |
| 4  | L               | L               | L              | H             |
| 5  | L               | L               | H              | H             |
| 5/2  | L               | H               | L              | L             |
| 7/2  | L               | H               | H              | L             |
| 9/2  | L               | H               | L              | H             |

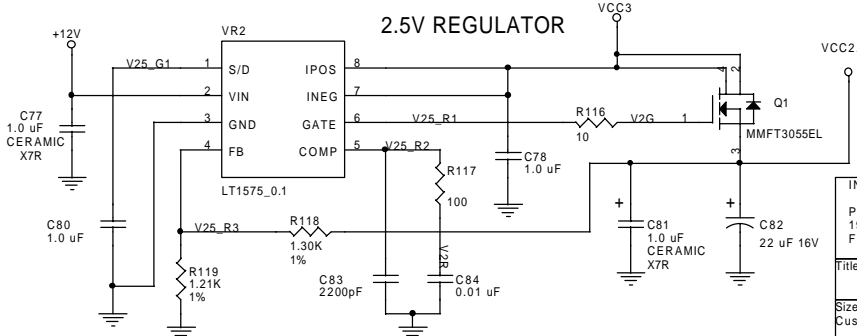
\*\*NOTE\*\* This is the new VRM8\_2.05 which has two pin changes, pin A5 is now 12Vin and pin B3 is now 5Vin.

VTT REGULATOR



\*\*NOTE\*\* VOLTAGE REGULATOR SHOULD BE LOCATED NEAR THE 440BX

2.5V REGULATOR



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Title: DC-DC CONVERTER CONNECTORS

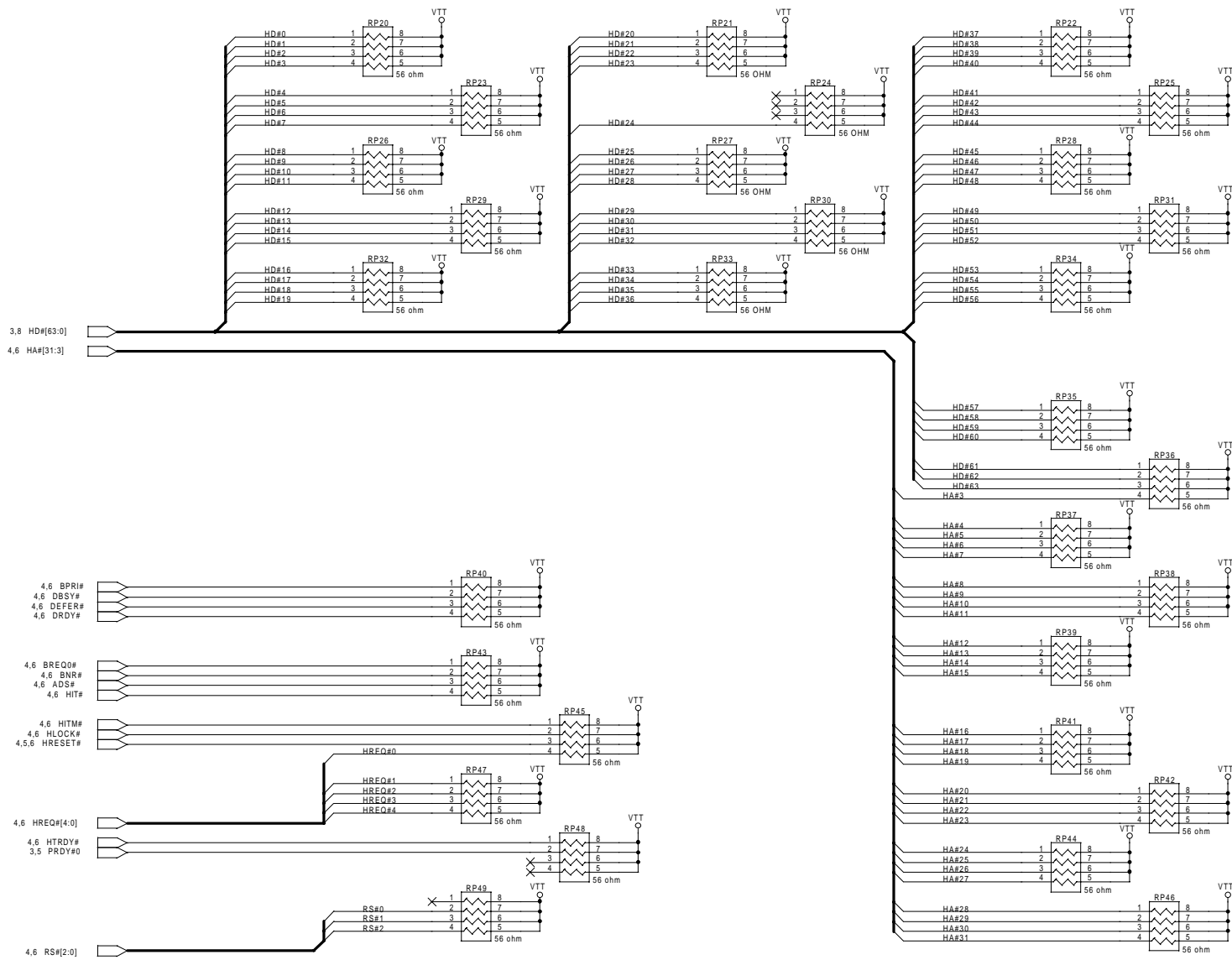
Size: Custom    Document Number: Intel(R) 440BX AGPset    Rev: 1.0

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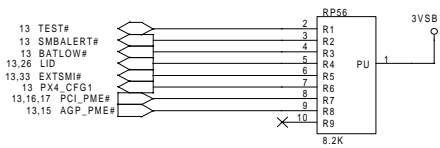
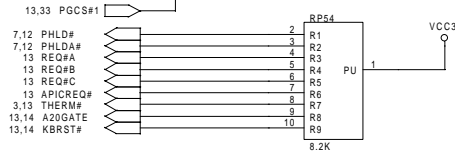
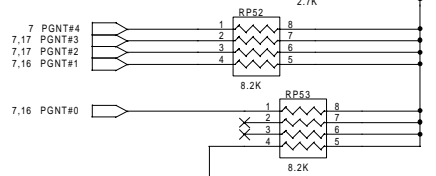
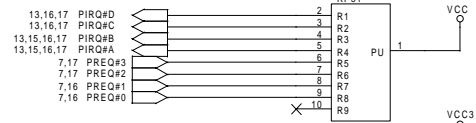
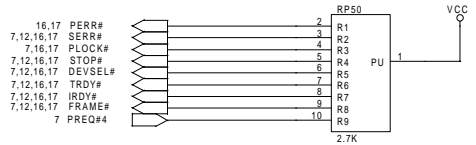


# GTL+ TERMINATION RESISTORS

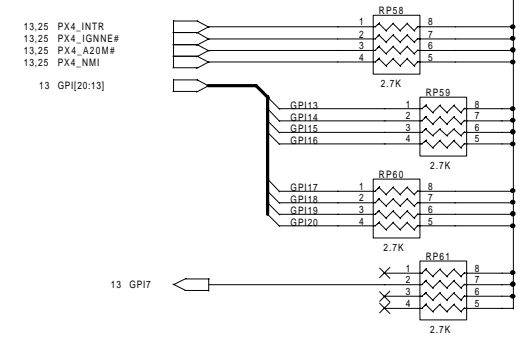
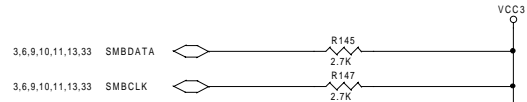
\*NOTE: May be removed if route lengths can be restricted to 1.5" MIN to 4.0" MAX.



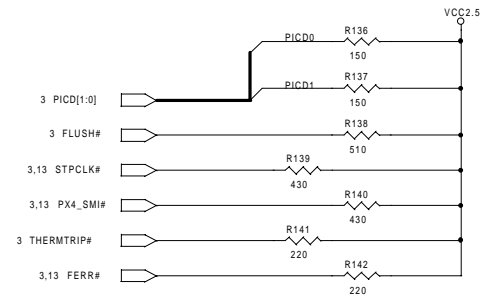
# PCI BUS



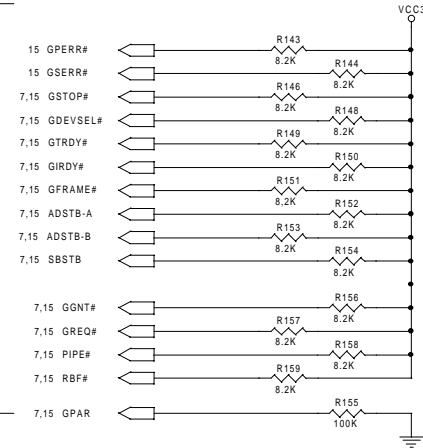
# PIIX4



# SLOT 1



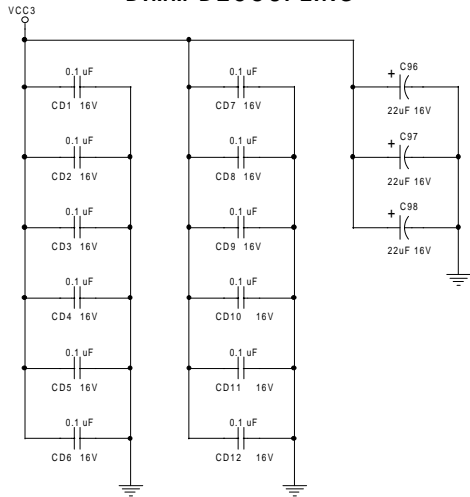
# AGP



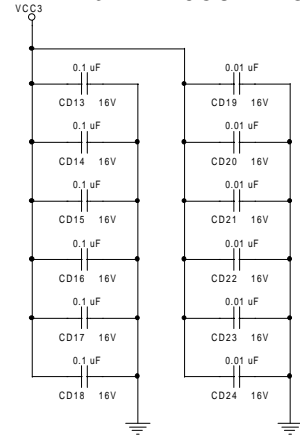
|                              |                          |                |
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| Title                        | Pullups: AGP/PCI/PIIX4   |                |
| Size                         | Document Number          | Rev            |
| Custom                       | Intel(R) 440BX AGPset    | 1.0            |
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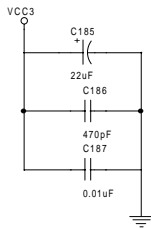
### DIMM DECOUPLING



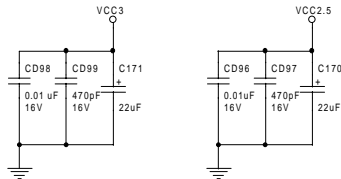
### 443BX DECOUPLING



### CKBF DECOUPLING

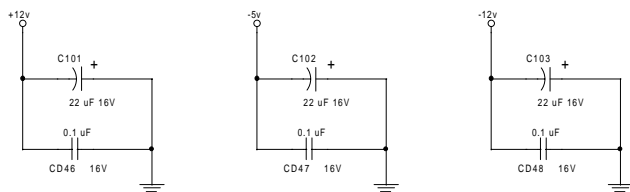
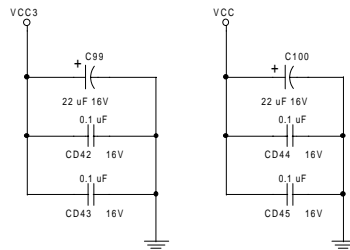


### CK100 DECOUPLING

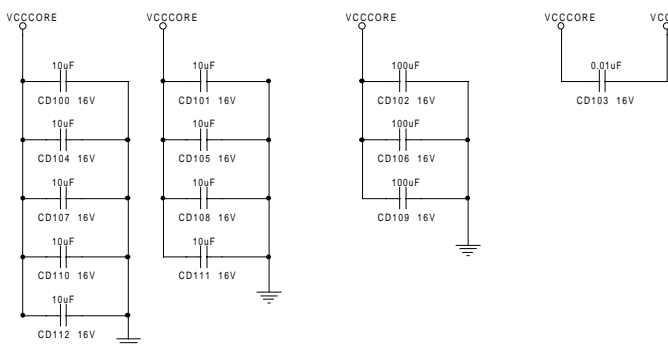


|                              |                          |   |          |
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| Title                        |                          | DRAM, CLOCK AND 440BX DECOUPLING CAPACITORS |          |
| Size                         | Document Number          |   | Rev      |
| Custom                       | Intel(R) 440BX AGPset    |   | 1.0      |
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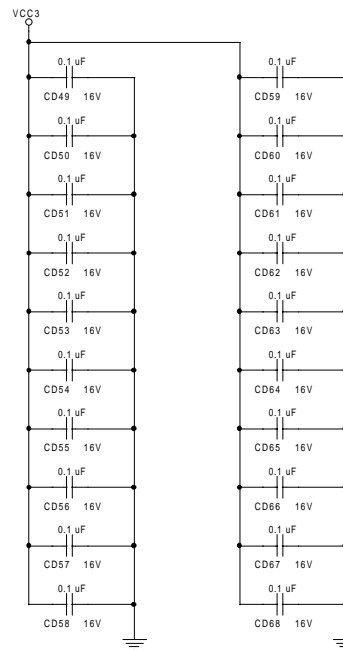
### BULK POWER DECOUPLING



### CORE VOLTAGE DECOUPLING

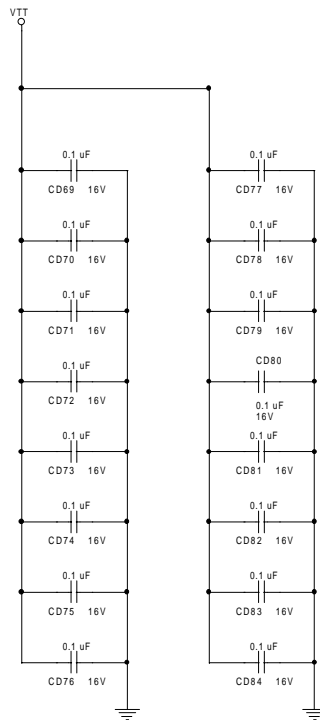


### 3 VOLT DECOUPLING



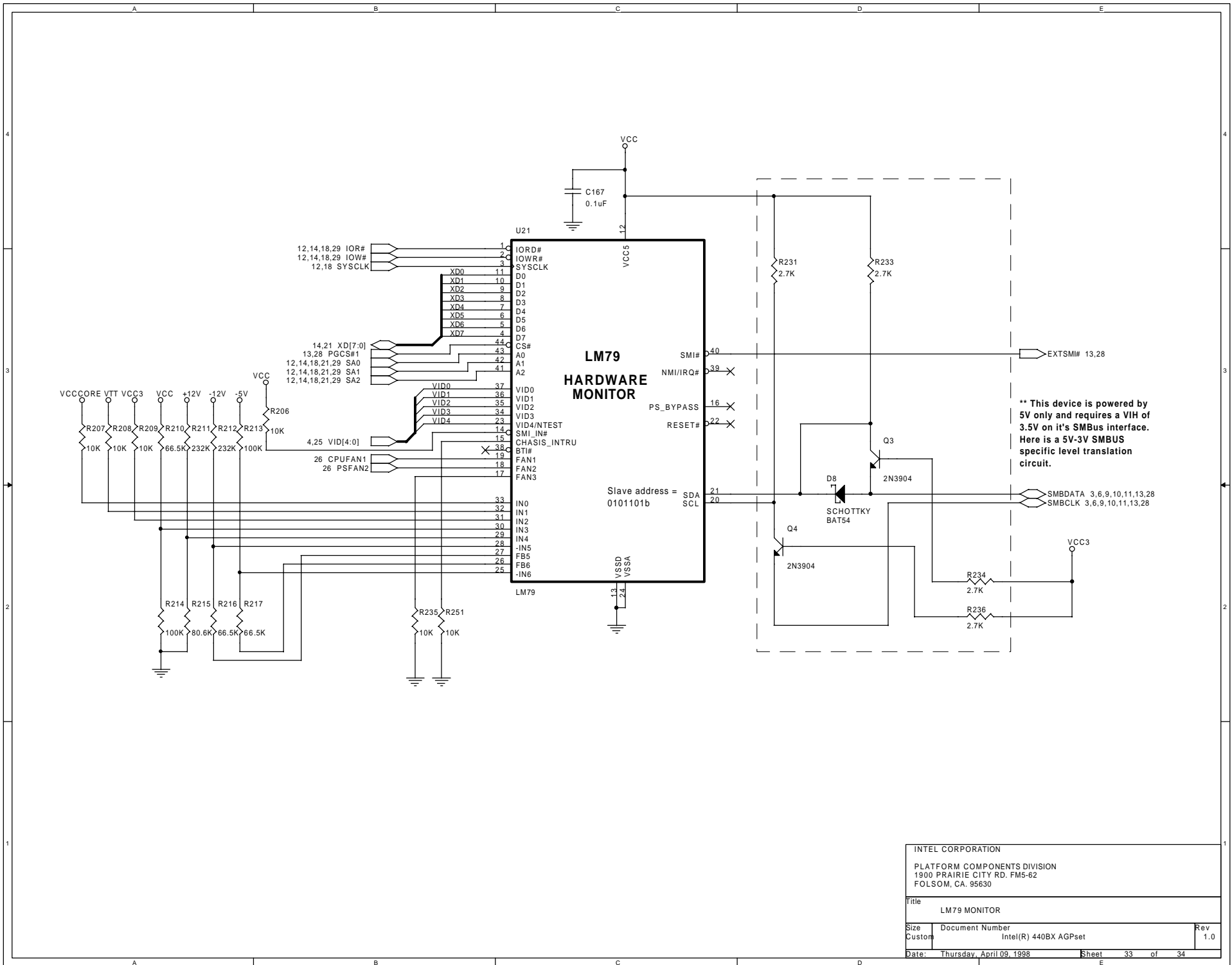
|  |                                    |          |
|--|------------------------------------|----------|
| INTEL CORPORATION  |                                    |          |
| PLATFORM COMPONENTS DIVISION<br>1900 PRAIRIE CITY RD. FM5-62<br>FOLSOM, CA 95630 |                                    |          |
| Title  | 3.3 VOLT AND BULK POWER DECOUPLING |          |
| Size   | Document Number                    | Rev      |
| Custom   | Intel(R) 440BX AGPset              | 1.0      |
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|  | 7                                  | 8        |

### TERMINATION VOLTAGE DECOUPLING



|                              |                          |                        |          |
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| Title                        |                          | TERMINATION DECOUPLING |          |
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| Title<br>LM79 MONITOR   |  |            |
| Size<br>Custom  | Document Number<br>Intel(R) 440BX AGPset | Rev<br>1.0 |
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REVISION 1.0 - Initial public release -- April, 1998

|                              |                          |       |          |
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| Title                        |                          |       |          |
| REVISION HISTORY             |                          |       |          |
| Size                         | Document Number          |       | Rev      |
| Custom                       | Intel(R) 440BX AGPset    |       | 1.0      |
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