Pentium® II Processor/ 440LX AGPset Design Guide

April, 1998

297651-001

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REVISION HISTORY

Revision Number	Date	Revision Status
Rev. 1.0	April 1998	Original Release

1

Introduction

CHAPTER 1
INTRODUCTION

1. Introduction

The intent of this document is to organize any special design recommendations and concerns that exist for creating a Pentium® II processor/440LX AGPset based system. Likely design errors have been identified and included here in a checklist format, in section 6 to alleviate problems during the debug phase. Some hints for early debug problems are also included in section 7.

Design Features: items that Intel feels will allow the capabilities of the Pentium II processor and the Intel® 440LX AGPset to be fully utilized in the market segments for which these products are designed.

Design Recommendations: items which Intel feels will provide flexibility to cover a broader range of products within a market segment.

Design Checklists: items which have been found to be incorrect on previous designs. These are provided as a tool to allow the quick debug of Pentium II processor based systems.

Design Considerations: items that should be considered, but may not be applicable to your design.

Debug Recommendations: items that may assist in the development of the Pentium II processor, 440LX AGPset, and products utilizing them.

1.1 Overview

Two different example designs are provided in this document: A single Slot 1 design (UP), and a two-way symmetric multiprocessor (referred to as 2-way SMP in this document) design. Both designs offer all of the following features:

- **Full Support for the Pentium II processor using Slot 1**
- **CPU bus frequencies of 66 MHz**
- **440LX AGPset**
  - **82443LX PCI/A.G.P. Controller (PAC)**
  - **82371AB PCI ISA IDE Xcelerator (PIIX4)**
- **Memory Interface: A wide range of DRAM support including**
  - **64-bit memory data interface plus 8 ECC bits**
  - **EDO DRAM and 66-MHz SDRAM (Synchronous) Support**
  - **4-Mbit, 16-Mbit and 64-Mbit DRAM Technologies**
- **4 PCI Add-in Slots**
  - **PCI Specification Rev 2.1 Compliant**
- **1 A.G.P. Slot**
  - **A.G.P. Interface Specification Rev 1.0 Compliant**
- **Integrated IDE Controller**
  - **PIO Mode [0–4]**
  - **PCI IDE Bus Master support Mode [SW1-MW2]**
  - **Ultra DMA Mode [0–2]**
- **Integrated Universal Serial Bus (USB) Controller and Hub with 2 USB ports**
- **Integrated System Power Management Support**
- **On-board Floppy, Serial, Parallel Ports**
- **2 ISA Add-in Slots**
- **ACPI Revision 1.0 support**
- **In addition, the 2-way (DP) SMP design has:**
  - **Support for two Pentium II processors (2 Slot 1's), each with a separate dedicated VRM**
  - **I/O APIC device support for MP interrupt support**

1.2 References

- Pentium® Pro Family Developer's Manual (Order Number: 242693)
- Pentium® Pro Processor BIOS Writer's Guide (Order Number: 649733)
- Intel Architecture MMX™ Technology Developer's Guide (Order Number: 243006)
- AP-523 Pentium® Pro Processor Power Distribution Guidelines (Order Number: 242764)
- AP-524 Pentium® Pro Processor GTL+ Layout Guidelines (Order Number: 242765)
- AP-525 Pentium® Pro Processor Thermal Design Guidelines (Order Number: 242766)
- Intel 440LX AGPset Data Sheet (Order Number: 290564)
- Intel 82371AB PIIX4 Data Sheet (Order Number 290562-001)
- Multi-Processor Specification 1.4 (242016-004)
- PCI Local Bus Specification, Revision 2.1
- Universal Serial Bus Specification, Revision 1.0
- Pentium® II Processor Enabling Technologies Supplier Guide, Revision 1.2 or later
- Pentium II Processor Data Sheet (http://www.intel.com/design/pentiumii/datashts/)
- Processor Heat Sink Design Guidelines (Application Note #586), Revision 1.0 or later
- Processor Fan/Heat Sink Target Specification, Revision 1.0 or later
- Slot 1 Test Kit User's Guide, Revision 1.0 or later
- AGP Interface Specification 1.0 Compliance (www.agpforum.org)
- PC100 SDRAM Specification Version 1.2
- 4 Clock 66-MHz 64/72-bit Unbuffered SDRAM DIMM
- 60 ns 64/72-bit 3.3V Unbuffered EDD DIMM
- VRM 8.1 DC-DC Converter Specification

Note: Pentium II Processor Data Sheet and Pentium II Processor/Slot 1 Data Sheet are the same document.

For reference questions regarding the above listed documents, contact your local Intel Sales Office.

2

Design Features

CHAPTER 2
DESIGN FEATURES

2. Design Features

2.1 Pentium® II Processor

The Pentium® II processor is a high-performance Intel Architecture processor which can be designed into products for the following market segments:

Desktop Home Market Segment

Desktop Corporate Market Segment

Workstation Market Segment

Server Market Segment

Please contact your local Intel Field Sales representative for assistance or guidance in your product definition process. They can provide you with Intel's Processor, AGPset and System roadmaps for the above market segments. Also available are system configuration recommendations for target segments for some of the above mentioned markets.

New applications and hardware add-ins from third party vendors are being developed that take advantage of the MMX(technology incorporated into the Pentium II processor. Please contact your local Intel Field Sales representative for information on IHV's and ISV's utilizing Intel's MMX technology.

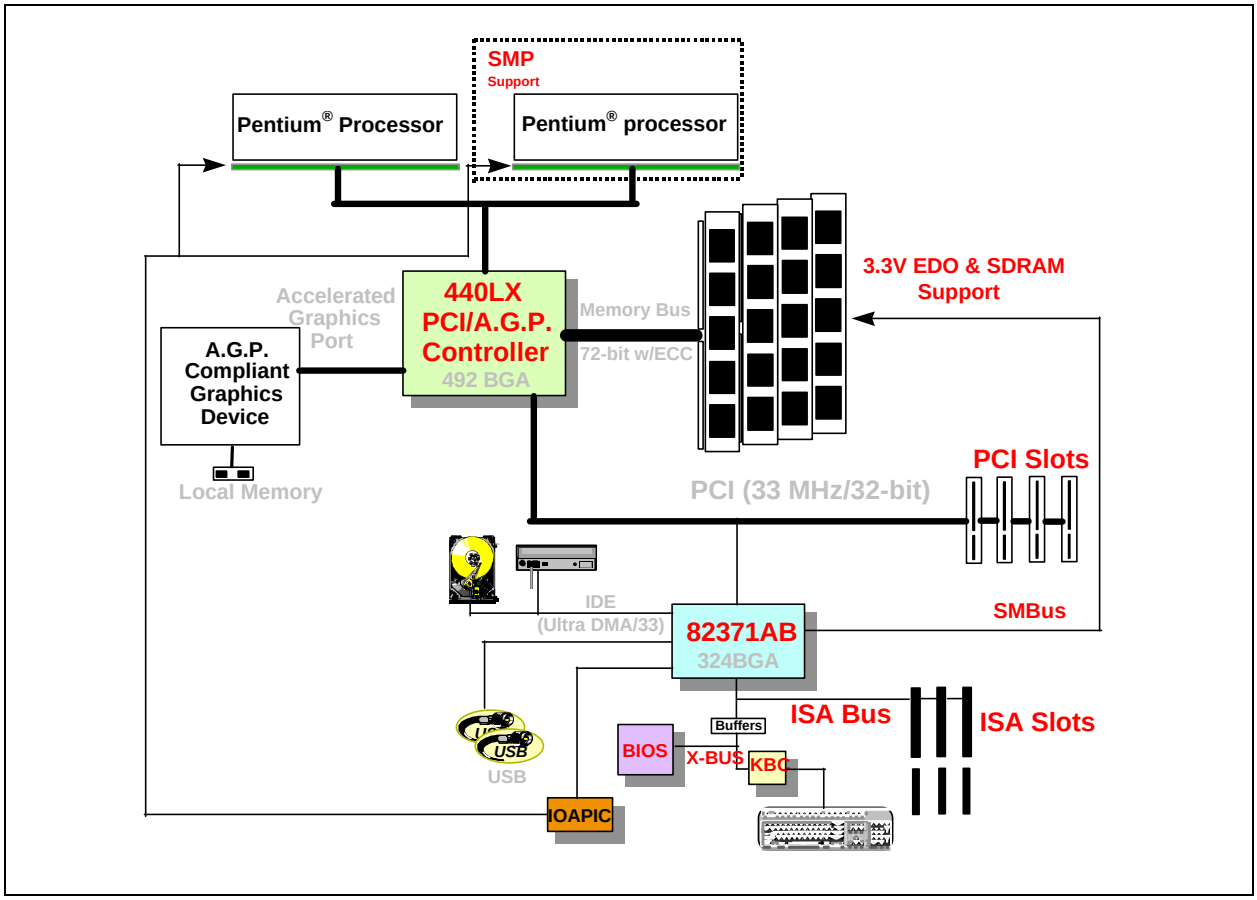


Figure 2-1. Intel Slot 1/440LX AGPset Reference Platform Block Diagram

2.2 Intel 440LX AGPset

The 440LX AGPset is the first generation of desktop AGPset products designed for the Pentium II processor. The 440LX PCI A.G.P. Controller (PAC) integrates a Host-to-PCI bridge, optimized DRAM controller and data path, and an Accelerated Graphics Port (A.G.P.) interface. A.G.P. is a high performance, component level interconnect, targeted at 3D graphics applications and based upon a set of performance enhancements to PCI. The I/O subsystem portion of the 440LX platform is based on the PIIX4, a highly integrated version of the Intel's PCI-to-ISA bridge family. The 440LX is developed as the ultimate Pentium II processor platform and is targeted for emerging 3D graphics and multimedia applications. The PAC component includes the following functions and capabilities:

Support for single and dual Pentium II processor configurations

64-bit GTL+ based Host Interface

32-bit Host address Support

64/72-bit Main Memory Interface with optimized support for SDRAM

32-bit PCI Bus Interface with integrated PCI arbiter

A.G.P. Interface with up to 133-MHz data transfer capability

Extensive Data Buffering between all interfaces for high throughput and concurrent operations

Figure 2-1 shows a block diagram of a typical platform based on the 440LX AGPset. The PAC host bus interface supports up to two Pentium II processors at 66 MHz. The physical interface design is based on the GTL+ specification. The PAC provides an optimized 72-bit DRAM interface (64-bit Data plus ECC). This interface supports 3.3V DRAM technologies. The PAC provides the interface to a PCI bus operating at 33 MHz. This interface implementation is compliant with *PCI Rev 2.1 Specification*. The PAC is the first Intel product that introduces the Accelerated Graphics Port interface. The PAC A.G.P. interface implementation is based on the *A.G.P. Specification Rev 1.0*. It can support up to 133-MHz data transfer rates.

The PAC is designed to support the PIIX4 I/O bridge. The PIIX4 is a highly integrated multifunctional component that supports the following functions and capabilities:

PCI Rev 2.1 compliant PCI-to-ISA Bridge with support for 33-MHz PCI operations

Deep Green Desktop Power Management Support

Enhanced DMA controller

8259 Compatible Programmable Interrupt Controller

System Timer functions

Integrated IDE controller with Ultra DMA/33 support

USB host interface with support for 2 USB ports

System Management Bus (SMB) with support for DIMM Serial Presence Detect

Support for an external I/O APIC component

System Interface

The Pentium II processor supports a second level cache size of 256K or 512K. All cache control logic is provided in the Pentium II processor. The PAC supports a maximum of 32-bit address or 4-GB memory address space from the processor perspective. The PAC provides bus control signals and address paths for transfers between the processors' host bus, PCI bus, Accelerated Graphics Port and main memory. The PAC supports a 4-deep in-order queue (i.e., it provides support for pipelining of up to four outstanding transaction requests on the host bus). Due to the system concurrency requirements, along with support for pipelining of address requests from the host bus, the PAC supports general request queuing for all three interfaces (Host, A.G.P. and PCI).

In Host-to-PCI transfers, depending on the PCI address space being accessed, the address will be either translated or directly forwarded on the PCI bus. If the access is to a PCI configuration space, the processor I/O cycle is mapped to a configuration cycle. If the access is to a PCI I/O or memory space, the processor address is passed without modification to the PCI bus, unless it hits a specific memory address range (later referenced as the A.G.P. Aperture or Graphics Aperture) dedicated for graphics memory address space. The address will be translated via the A.G.P. address remapping mechanism and forwarded to the DRAM subsystem. Host cycles forwarded to A.G.P. are defined by the A.G.P. address map.

The PAC also receives requests from PCI bus and A.G.P. bus initiators for access to main memory. If a target address is within the graphics aperture, then the request is translated into the appropriate memory address. A.G.P. accesses destined to the graphics aperture are not snooped on the host bus because coherency of aperture data is maintained by software. All accesses to the aperture, from the Host, PCI or A.G.P., are translated using the A.G.P. address remapping mechanism.

DRAM Interface

The PAC integrates a main memory controller that supports a 64/72-bit DRAM interface. The DRAM controller supports the following features:

- *DRAM type:* Extended Data Out (EDO) and Synchronous (SDRAM); DRAM controller optimized for dual-bank SDRAM organization

- *Memory Size:* SDRAM: 8 Mbytes to 512 Mbytes with eight memory rows
  EDO: 8 Mbytes to 1Gbyte with eight memory rows
- *Addressing Type:* Symmetrical and Asymmetrical addressing
- *Memory Modules supported:* Single and double density DIMMs
- *Configurable DRAM Interface:* Configuration #1: Large Memory Array (8 Row Support for x8 and x16 SS or DS DIMMs, x4 SS DIMMs)
  Configuration #2: Small Memory Array (6 Row Support for x8, x16 and x32 SS or DS DIMMs)
- *DRAM device technology:* 4 Mbit, 16 Mbit and 64 Mbit
- *DRAM Speeds:* 50 ns and 60 ns EDO DRAM and SDRAM 66-MHz parameters for synchronous memory.
- *Serial Presence Detect:* SDRAM: Required
  EDO: Supported

The PAC provides optional data integrity features including EC (Error Checking) or ECC (Error Checking and Correcting) in the memory array. Error Checking (EC) mode provides single and multiple bit error detection. In ECC mode, the PAC provides error checking and correction of the data during reads from the DRAM. The PAC supports multiple-bit error detection and single-bit error correction.

Accelerated Graphics Port Interface

The 440LX is the first chip set that supports the A.G.P. interface; hence the name change to AGPset. The PAC A.G.P. implementation complies with the *Accelerated Graphics Port Specification 1.0*. The PAC A.G.P. interface, must synchronously couple to the host bus. The A.G.P. interface can reach a theoretical 532-Mbytes/sec transfer rate.

PCI Interface

The PAC PCI interface is PCI Local Bus Specification Revision 2.1 compliant (32-bit and 33 MHz) and supports up to five external PCI bus masters in addition to the I/O bridge (PIIX4). The PAC only supports synchronous PCI coupling to the host bus.

The 440LX supports:

- 8 Mbytes to 512 Mbytes of SDRAM or EDO in Memory Configuration #1
- 8 Mbytes to 384 Mbytes of SDRAM or EDO is supported in Memory Configuration #2
- 1 Gbyte of memory is achieved with *Buffered* EDO DIMMs.

Read/Write Buffers

The PAC implements a sophisticated data buffering algorithm to support the required level of concurrent operations and provide adequate sustained bandwidth between DRAM subsystem and all other system interfaces (e.g. CPU, A.G.P. and PCI).

System Clocking

The PAC operates the host interface at 66 MHz, the PCI interface at 33 MHz and the A.G.P. interface at 66/133 MHz. Coupling between all interfaces and internal logic is done synchronously. The PAC is not designed to support host bus frequencies lower than 66 MHz. The PAC uses an external clock synthesizer which produces reference clocks for the host, A.G.P. and PCI interfaces.

I/O APIC

The I/O APIC supports interrupts for dual processor designs. Refer to I/O APIC datasheet for more information. Dual Processor Schematics are provided in this document.

2.3 PCI ISA IDE Xcelerator: PIIX4

The 82371AB PCI ISA IDE Xcelerator (PIIX4) is a multi-function PCI device implementing a PCI-to-ISA bridge function, a PCI IDE function, a Universal Serial Bus host/hub function, and an Enhanced Power Management function. As a PCI-to-ISA bridge, the PIIX4 integrates many common I/O functions found in ISA-based PC systems—a seven channel 82C371 DMA Controller, two 82C59 Interrupt Controllers, an 82C54 Timer/Counter, and a Real Time Clock. In addition to compatible transfers, each DMA channel supports Type F transfers.

The 440LX/PIIX4 also contains full support for PC/PCI protocol implementing PCI based DMA. The Interrupt Controller has Edge or Level sensitive programmable inputs and fully supports the use of an external I/O Advanced Programmable Interrupt Controller (APIC) and Serial Interrupts. Chip select decoding is provided for BIOS, the Real Time Clock, the Keyboard Controller, the external Microcontroller, as well as two Programmable Chip Selects. The PIIX4 provides full Plug and Play compatibility. The PIIX4 can be configured as a Subtractive Decode bridge or as a Positive Decode bridge.

The PIIX4 supports up to four IDE devices on two separate IDE controllers. It provides an interface for IDE hard disks and CD ROMs. The PIIX4 supports PIO, BMIDE, and Ultra DMA/33.

The PIIX4 contains a Universal Serial Bus (USB) Host Controller that is Universal Host Controller Interface (UHCI 1.0) compliant. The Host Controller’s root hub has two programmable USB ports.

The PIIX4 supports Advanced Power Management, including full clock control, device management for up to 14 devices, and suspend and resume logic. It fully supports operating system directed power management via the Advanced Configuration and Power Interface (ACPI) specification 1.0. The PIIX4 integrates both a System Management Bus (SMBus) host and slave interface for serial communication with other devices.

For more information on PIIX4, refer to the PIIX4 Datasheet, Order Number 290562.

3

440LX Platform Reference Design

CHAPTER 3
440LX PLATFORM REFERENCE DESIGN

3. 440LX Platform Reference Design

3.1 440LX UP Reference Design

This section describes the 440LX Reference Design Schematics shown in ***Appendix H*** of this document. Please read this section carefully to observe all design recommendations and requirements.

The description of each schematic page is named by the logic block shown on that page. The two numbers after the schematic page name list the page number of the single processor design (i.e. UP-x).

Cover Sheet **UP-1**

The Cover Sheet shows the Schematic page titles, page numbers and disclaimers.

Block Diagram **UP-2**

This page shows a block diagram of the 440LX system. Schematic page numbers of each of the major components are shown.

Slot 1 Connector (part 1) **UP-3**

This page shows the Slot 1 Connector (part 1). Shown on this page are the VTT supply, and pullups for IERR# and TESTHI. SLP# connection comes directly from the PIIX4. Intel recommends placing 0 ohm resistors on the EMI signals.

Primary Slot 1 Connector (part 2) **UP-4**

This page shows the Slot 1 Connector (part 2). This page shows the optional connections for overriding the VID from the processor. This page also shows an optional thermal sensor.

Clock Synthesizer and ITP Connector **UP-5**

This page shows the clock synthesizer components CK3D and CKI/O. The clock synthesizer components must meet all of the host, PCI and other system clock requirements. Several vendors offer components that can be used in this design.

This page also shows the In Target Probe (ITP) Connector. The ITP connector is recommended in order to use the In Target Probe tool available from Intel and other tool vendors for Pentium II processor based platform debug. **Note:** Some logic analyzer vendors also support the use of the ITP connector. This connector is optional. **It is recommended to design these headers into the system for initial system debug and development, and leave the connector footprints unpopulated for production.**

PAC Component (Host and DRAM Interfaces) **UP-6**

This page shows the PAC component, Host and DRAM Interfaces. The PAC connects to the lower 32-bits of the CPU address bus and the CPU control signals, and generates DRAM control signals for the memory interface.

In this design, the PAC is configured to interface to a “small” memory array. Two copies of the memory address signals are provided in this configuration. A buffered copy of CKE is provided to each DIMM socket.

Note:

No series resistors are required on the DRAM interface signals from the PAC to the array. The IOQ jumper is optional, but needed for initial debug.

PAC Component (PCI and A.G.P. Interfaces) UP-7

This page shows the PAC component, PCI and A.G.P. Interfaces. Follow the recommendations outlined in the *A.G.P. Platform Design Guide*, available on the A.G.P. Implementer's Forum WWW site (http://www.agpforum.org). Note: you must be a member of the A.G.P. Implementer's Forum to download this document.

PAC Component (Memory and Host Data Bus Interfaces) UP-8

This page shows the PAC component, Memory and Host Data Bus Interfaces. GTL_REF signals are also shown on this page. Ideally, the GTL_REF signals should be decoupled separately, and as close as possible to the PAC component, but this is not an absolute requirement. ECC is optional in a 440LX platform. We recommend that MECC[7:0] be routed to the memory array, to allow the option to use either ECC or non-ECC DIMMs.

DIMM Connectors 0, 1, And 2 UP- 9

UP-10

UP-11

These three pages show the DRAM interface connections from the PAC to the DRAM array. This reference design uses memory configuration #2 as described in 82443LX PAC Datasheet. It is very important to follow the memory subsystem layout and routing guidelines outlined in this document.

For this memory design, using Memory Configuration #2:

MAA[13:0], RCSA[1:0], SRAS0, SCAS0, CDQA[7:0], WE0# are connected to the ***furthest*** DIMM socket from the PAC (in this reference design, the furthest DIMM socket is DIMM #2).

MAA[13:0], RCSA[3:2], SRAS1, SCAS1, CDQA[7:0], WE1# are connected to the ***middle*** DIMM socket from the PAC (in this reference design, the middle DIMM socket is DIMM #1).

MAB[13:0], RCSA[5:4], SRAS2, SCAS2, CDQA[7,6,4:2,0], CDQB[5,1], WE2# are connected to the ***closest*** DIMM socket from the PAC (in this reference design, the closest DIMM socket is DIMM #0).

To ensure your 440LX memory array supports both EDO DRAM and SDRAM, 16 Mb and 64 Mb, 2-bank and 4-bank, follow the signal connection recommendations in the *Intel EDO and SDRAM DIMM Specifications*.

PIIX4 Component UP-12

This page shows the PIIX4 component. The PIIX4 component connects to the PCI bus, dual IDE connectors, and the ISA bus. This reference design supports a subset of the power management features of the PIIX4. Refer to the Power Management section of this document.

PIIX4 Component UP-13

This page shows the PIIX4 component Interrupts, USB, DMA, Power Management, XBus, and GPIO interfaces. The RTC is required if any power management features are used. JP3: If using an external RTC, VBAT can receive power from 3.3VSTBY (jumper 1-2), else, use the backup battery BT1 (jumper 2-3).

SUSC# is connected to the ATX power connector, pg 26, to pin #14. The VREF circuit is provided to ensure proper power sequencing.

Ultra I/O Component UP-14

This page shows the Ultra I/O component. The RTC may optionally be used. An Infra Red Header Port is also optional.

A.G.P. Connector **UP-15**

This page shows the A.G.P. Connector. In this design, A.G.P. INTA and INTB are connected directly to the PCI INTA and INTB. The interrupt signals are open-collector, and are pulled up to $V_{CC3.3}$.

Follow the recommendations outlined in the *A.G.P. Platform Design Guide*, available on the A.G.P. Implementer's Forum WWW site. Note: you must be a member of the A.G.P. Implementer's Forum to download this document.

PCI Connectors **UP-16**

UP-17

These pages show the PCI Connectors. In this design, 4 PCI Connectors are used. Be sure to follow the 440LX PCI Interface Checklist in this document.

ISA Connectors **UP-18**

This page shows the ISA Connectors.

PCI IDE Connectors **UP-19**

This page shows the IDE Connectors. No special external logic is required to support Ultra DMA/33 hard drives.

USB Headers **UP-20**

This page shows the USB Headers. Note, the voltage divider on the over current (OC) signals provide logic level transitions for the PIIX4.

Flash BIOS Component **UP-21**

This page shows the 28F002BC-T Flash BIOS component which provides 128 Kbytes of BIOS memory. A jumper is used to provide the option for allowing the BIOS to be programmed in the system for BIOS upgrades and/or for programming plug and play information into the Flash device.

Note that a 2 Meg Flash device may be required for certain applications (motherboard devices such as graphics, SCSI or LAN).

Parallel Port **UP-22**

This page shows the Parallel Port Interface.

Serial and Floppy **UP-23**

This page shows the Serial Ports and Floppy Drive interfaces.

Keyboard and Mouse Connectors **UP-24**

This page shows the Keyboard and Mouse interface.

VRM 8.1 **UP-25**

The top of this page shows the voltage regulator modules (VRM) connector(s). The VRM modules provide the 5V to $V_{CC_{CORE}}$ voltage conversion for the Pentium II processor.

The bottom of this page shows two voltage regulators, one for generating the 1.5V GTL+ terminating voltage (VTT), the other is a 2.5V regulator. The VTT generation circuit must be able to provide about 4.6 amps of current under worst case conditions.

Note that the 4.6 amps of current will normally be supplied from two linear regulator devices (about 2.5 amps each), one located at each end of the GTL+ bus traces. However, one linear regulator device (supplying the entire 4.6 amps) can be used if both ends of the GTL+ bus traces are near each other.

Power Connectors Front Panel Jumpers **UP-26**

This page shows the system power connectors, hardware reset logic, and standard chassis connectors for the hard disk, power LEDs, and speaker output. **Note:** a CPU Fan Header is required for the Intel Boxed Pentium II processor.

GTL+ Bus Termination Resistors **UP-27**

This page shows the GTL+ bus termination resistors. The components shown are flat chip resistor array devices. These components are available in both 4 and 8 devices per package options. These devices have been chosen for their small size to reduce board space required. Discrete, SIP or SOJ resistor packages can also be used but will require more board area. Each GTL+ signal that connects between the PAC and the slot 1 connector should be dual terminated to insure the most robust GTL+ signaling. Each GTL+ signal should be routed using a daisy chain methodology as described in the GTL+ layout guidelines section of this document. The termination resistors for each net must be located at the ends of the nets. Connect the VTT side of the resistor packs to as short of a trace as possible before routing to the VTT plane. If the VTT plane is on an inner layer, keep the trace distance to the via as short as possible by placing the via between pins 6 and 7 for each resistor package. Where this is not possible, use multiple vias to the VTT plane for each group of 4 signals. Please refer to the GTL+ Specification for more complete details on GTL+ signaling.

Note: See Appendix F for single end termination designs.

Pull-up and Pull-down Resistors **UP-28**

UP-29

These pages show pull-up and pull-down resistors for PCI signals, PIIX4, Slot 1(CMOS), ISA, and A.G.P. signals. Also shown are spare gates.

De-coupling Capacitors **UP-30**

UP-31

UP-32

These pages show de-coupling capacitance used in these schematics.

3.2 440LX DP Reference Design

This section describes the 440LX DP Reference Design Schematics shown in ***Appendix H*** of this document. Please read this section carefully to observe all design recommendations and requirements.

The description of each schematic page is named by the logic block shown on that page. The two numbers after the schematic page name list the page number of the dual processor design (DP-x).

Cover Sheet **DP-1**

The Cover Sheet shows the Schematic page titles, page numbers and disclaimers.

Block Diagram **DP-2**

This page shows a block diagram overview of the 440LX system design. Schematic page numbers of each of the major schematics components are shown.

First Slot 1 Connector (part 1) **DP-3**

This page shows the Slot 1 Connector (part 1). Shown on this page are the VTT supply. SLP# connection comes directly from the PIIX4. Intel recommends placing 0 ohm resistors on the EMI signals.

First Slot 1 Connector (part 2) DP-4

This page shows the Slot 1 Connector (part 2). This page shows the optional connections for overriding the VID from the processor. This page also shows an optional thermal sensor. A_SLOTOCC# is used to gate the POWERGOOD signal to the processor.

Second Slot 1 Connector (part 1) DP-5

This page shows the Slot 1 Connector (part 1). Shown on this page are the VTT supply. SLP# connection comes directly from the PIIX4. Intel recommends placing 0 ohm resistors on the EMI signals.

Second Slot 1 Connector (part 2) DP-6

This page shows the Slot 1 Connector (part 2). This page shows the optional connections for overriding the VID from the processor. This page also shows an optional thermal sensor. B_SLOTOCC# is used to gate the POWERGOOD signal to the processor.

Clock Synthesizer and ITP Connector DP-7

This page shows the clock synthesizer components CK4D and CKI/O. The clock synthesizer components must meet all of the host, PCI and other system clock requirements. Several vendors offer components that can be used in this design.

This page also shows the In Target Probe (ITP) Connector. The ITP connector is recommended in order to use the In Target Probe tool. This tool is available from Intel and other tool vendors for Pentium II processor based platform debug. **Note:** Some logic analyzer vendors also support the use of the ITP connector. This connector is optional. **It is recommended to design these headers into the system for initial system debug and development, and leave the connector footprints unpopulated for production.**

TDI and TDO jumpers are provided for three different configurations—when one processor is in first slot 1 (second has termination card), when one processor is in second slot 1 (first has termination card) or when both the processors are present.

PAC Component (Host and DRAM Interfaces) DP-8

This page shows the PAC component, Host and DRAM Interfaces. The PAC connects to the lower 32-bits of the CPU address bus and the CPU control signals, and generates DRAM control signals for the memory interface.

In this design, the PAC is configured to interface to a “large” memory array. Two copies of the RAS#/CS# signals are provided in this configuration. There is one copy of memory address bits 13 down to 2. So these must be buffered. There are two copies of memory address bits 1 and 0 and they must not be buffered. A buffered copy of CKE is provided to each DIMM socket.

Note: No series resistors are required on the DRAM interface signals from the PAC to the array. The IOQ jumper is optional, but needed for initial debug.

PAC Component (PCI and A.G.P. Interfaces) DP-9

This page shows the PAC component, PCI and A.G.P. Interfaces. Follow the recommendations outlined in the *A.G.P. Platform Design Guide*, available on the A.G.P. Implementer’s Forum WWW site (http://www.agpforum.org). Note: you must be a member of the A.G.P. Implementer’s Forum to download this document.

PAC Component (Memory and Host Data Bus Interfaces) DP-10

This page shows the PAC component, Memory and Host Data Bus Interfaces. GTL_REF signals are also shown on this page. Ideally, the GTL_REF signals should be decoupled separately and as close as possible to the PAC component, but this is not an absolute requirement. ECC is optional in a 440LX platform. We recommend that MECC[7:0] be routed to the memory array, to allow the option to use either ECC or non-ECC DIMMs.

DIMM Connectors 0, 1, 2, and 3 **DP-11**

DP-12

DP-13

DP-14

These four pages show the DRAM interface connections from the PAC to the DRAM array. This reference design uses memory configuration #1 as described in 82443LX PAC Datasheet. It is very important to follow the memory subsystem layout and routing guidelines outlined in this document.

For this memory design, using Memory Configuration #1:

Copies of **RCSA#[7:0], CDQA[5]&[1]**, and **WE#** are provided to the most heavily loaded control signals in this array. A buffered copy of **MAA[13:2]** must go to each DIMM socket. **MAA[1:0]** and **MAB[1:0]** are copies of the first two memory address signals.

To ensure your 440LX memory array supports both EDO DRAM and SDRAM, 16 Mb and 64 Mb, 2-bank and 4-bank, follow the signal connection recommendations in the *Intel EDO and SDRAM DIMM Specifications*.

PIIX4 Component **DP-15**

This page shows the PIIX4 component. The PIIX4 component connects to the PCI bus, dual IDE connectors, and the ISA bus. This reference design supports a subset of the power management features of the PIIX4. Refer to the Power Management section of this document.

PIIX4 Component **DP-16**

This page shows the PIIX4 component Interrupts, USB, DMA, Power Management, XBus, and GPIO interfaces. The RTC is required if any power management features are used. JP3: If using an external RTC, V_{BAT} can receive power from $3.3V_{STBY}$ (jumper 1-2), otherwise, use the backup battery BT1 (jumper 2-3).

SUSC is connected to the ATX power connector, pg 30, to pin #14. The V_{REF} circuit is provided to ensure proper power sequencing.

I/O APIC **DP-17**

This page shows the I/O APIC component.

Ultra I/O Component **DP-18**

This page shows the Ultra I/O component. The RTC may optionally be used. An Infra Red Header Port is also optional.

A.G.P. Connector **DP-19**

This page shows the A.G.P. Connector. In this design, A.G.P. INTA and INTB are connected directly to the PCI INTA and INTB. The interrupt signals are open-collector, and are pulled up to $V_{CC3.3}$.

Follow the recommendations outlined in the *A.G.P. Platform Design Guide*, available on the A.G.P. Implementer's Forum WWW site (http://www.agpforum.org). Note: you must be a member of the A.G.P. Implementer's Forum to download this document.

PCI Connectors **DP-20**

DP-21

These pages show the PCI Connectors. In this design, 4 PCI Connectors are used. Be sure to follow the 440LX PCI Interface Checklist in this document.

ISA Connectors **DP-22**

This page shows the ISA Connectors.

PCI IDE Connectors **DP-23**

This page shows the IDE Connectors. No special external logic is required to support Ultra DMA/33 hard drives.

USB Headers **DP-24**

This page shows the USB Headers. Note: the voltage divider on the over current (OC) signals provide logic level transitions for the PIIX4.

Flash BIOS Component **DP-25**

This page shows the 28F002BC-T Flash BIOS component which provides 128 Kbytes of BIOS memory. A jumper is used to provide the option for allowing the BIOS to be programmed in the system for BIOS upgrades and/or for programming plug and plug information into the Flash device.

Note that a 2 Meg Flash device may be required for certain applications (motherboard devices such as graphics, SCSI or LAN).

Parallel Port **DP-26**

This page shows the Parallel Port Interface.

Serial and Floppy **DP-27**

This page shows the Serial Ports and Floppy Drive interfaces.

Keyboard and Mouse Connectors **DP-28**

This page shows the Keyboard and Mouse interface.

VRM 8.1 **DP-29**

The top of this page shows two voltage regulator modules (VRM) connector(s). The VRM modules provide the 5V to VCC_{CORE} voltage conversion for the Pentium II processor.

The bottom of this page shows two voltage regulators. One generates the 1.5V GTL+ terminating voltage (VTT), while the other is a 2.5V regulator. The VTT generation circuit must be able to provide about 4.6 amps of current under worst case conditions.

Note that the 4.6 amps of current will normally be supplied from two linear regulator devices (about 2.5 amps each), one located at each end of the GTL+ bus traces. However, one linear regulator device (supplying the entire 4.6 amps) can be used if both ends of the GTL+ bus traces are near each other.

Power Connectors Front Panel Jumpers **DP-30**

This page shows the system power connectors, hardware reset logic, and standard chassis connectors for the hard disk, power LEDs, and speaker output. Note: a CPU Fan Header is required for the Intel Boxed Pentium II processor.

Pull-up and Pull-down Resistors **DP-31**

DP-32

These pages show pull-up and pull-down resistors for PCI signals, PIIX4, Slot 1(CMOS), ISA, and A.G.P. signals. Also shown are spare gates.

De-coupling Capacitors **DP-33**

DP-34

DP-35

These pages show decoupling capacitance used in these schematics.

4

Design Recommendations

CHAPTER 4
DESIGN RECOMMENDATIONS

4. Design Recommendations

Voltage Definitions

For the purposes of this document the following nominal voltage definitions are used:

V_{CC}	5.0V
V_{CC_3}	3.3V
$V_{CC_{CORE}}$	Voltage is dependent on the five bit VID setting
V_{CC_P}	Voltage is dependent on the five bit VID setting
$V_{CC_{2.5}}$	2.5V
V_{TT}	1.5V
V_{REF}	1.0V
AGPV_{REF}	3.3V

4.1 General Design Recommendations

1. Intel recommends using an industry standard programmable Voltage Regulator Module (VRM) installed in a VRM header or an on-board programmable voltage regulator designed for Pentium II processors. Please see the *VRM 8.1 DC-DC Converter Specification* for details on Pentium II processor regulator requirements.
2. Systems should be capable of varying the host bus to processor core frequency ratio per the System Bus to Core Frequency Multiplier Configuration table of the *Pentium II Processor/Slot 1 Data Sheet*. The Pentium II processor uses the following signals to configure the internal clock multiplier ratio: LINT[0]/INTR, IGNNE#, A20M#, LINT[1]/NMI. Follow the recommendations in this document to ensure adequate hold times are met on the strapping signals. Ensure the output of the strapping logic is a $V_{CC_{2.5}}$ logic level for connection to the Slot 1 connector. This can be accomplished using an open-drain output driver with pull-up resistors to $V_{CC_{2.5}}$.
3. Design to the Flexible Motherboard table of the *Pentium II Processor/Slot 1 Data Sheet*. Also prepare additional thermal margin for increases of 1-5W for higher performance or otherwise enhanced processors.
4. Motherboard designs targeted for system integrators should design to the Boxed Pentium II electrical, mechanical and thermal specifications provided in the Boxed Pentium II section of the *Pentium II Processor/Slot 1 Data Sheet*, most notably the required fan power header and fan/heatsink physical clearance on the motherboard.
5. Motherboard designs should incorporate the retention mechanism, retention mechanism attach mount and heat sink support mounting holes and keep out areas for the Pentium II processor and Boxed Pentium II processor.

4.2 Pentium Pro Processor/440FX to a Pentium II Processor/440LX Design Transition

The following list of items should be considered when Transitioning an existing Pentium Pro Processor Socket 8/440FX PCIset based system to one based on a Slot 1 connector/440LX AGPset. 82450KX/GX PCIset designs are not supported by the Pentium II processor.

1. The Pentium II processor in the Slot 1 connector has a different physical form factor than the existing Pentium Pro processor. Please see the *Pentium II Processor/Slot 1 Data Sheet* for mechanical details to ensure that the mechanical keep out areas are observed and no mechanical interference occurs between the Pentium II processor and your chassis. For motherboard designs targeted for use with the Boxed Pentium II processor, ensure that the fan/heatsink mechanical keep out areas are observed as described in the *Pentium II Processor/Slot 1 Data Sheet.*
2. Pentium II processors will be provided in the new Single Edge Contact Cartridge (S.E.C. Cartridge) packaging technology. The Slot 1 connector requires mechanical support of the S.E.C. Cartridge and heat sink. Intel has enabled a retention mechanism and heat sink support to retain the S.E.C. Cartridge during shock and vibration conditions. Proper mechanical support must be provided for the S.E.C. Cartridge. The Intel enabled solution requires mechanical keep out areas (on the top and bottom of the motherboard) for the retention mechanism, retention mechanism attach mount and heat sink support. Refer to the *Pentium II Processor/Slot 1 Data Sheet.*
3. The Pentium II processor physical form factor difference will cause different air flow dynamics in your chassis. Your thermal management solution should be examined to ensure that proper airflow and Pentium II processor cooling is provided to meet the T_{PLATE} specification provided in the *Pentium II Processor/Slot 1 Data Sheet.*
4. The Pentium II processor utilizes a $V_{CC_{CORE}}$ of 2.8V while the existing Pentium Pro processor has a V_{CC_P} of 3.3V for the 166 to 200-MHz versions and 3.1V for the 150-MHz version. Please ensure that your VRM or on-board regulator solution supports the *VRM 8.1 DC-DC Converter Specification* voltage range and the Pentium II processor current requirements. Designs utilizing a VRM 8.0 solution should consult their VRM or regulator vendor to determine if these devices support the higher current requirement of a Pentium II processor and the requirements for a flexible motherboard as documented in the *Pentium II Processor/Slot 1 Data Sheet.* Please note that a VRM 8.0 solution will not support future processors. Intel highly recommends a five bit V_{ID} regulator.
5. The Slot 1 has defined an additional V_{ID}[4] pin. The regulator must provide between 1.8 and 2.8V to be able to support the Pentium II processor and future higher performance processors.
6. Please see the *Pentium II Processor/Slot 1 Data Sheet* for the flexible motherboard $V_{CC_{CORE}}$ current requirements.
7. The VRM 8.1 header has three pins that are redefined from the VRM 8.0 header:

Pin	VRM8.1	VRM8.0
A9	V_{ID}4	UP#
B3	Reserved	5V IN
A6	IShare	Reserved

8. The UP# signal is defined as RESERVED on the Slot 1 connector and must be a no-connect.
9. No UP# signal is defined on the VRM 8.1 header.
10. The following list of input signals are required to be converted to $V_{CC_{2.5}}$ logic levels going to the Slot 1 connector: A20M#, IGNNE#, TDI, PWRGOOD, LINT[0]/INTR, LINT[1]/NMI, PREQ#, FLUSH#, SMI#, INIT#, STPCLK#, SLP#, TMS and TRST#. Intel recommends that an open collector/drain driver be used with a pull-up to $V_{CC_{2.5}}$ for the logic level conversion. The pull-up resistor values should take into consideration the LAI recommendation in section 7.3.1.
11. The following list of open drain output signals must be pulled up to $V_{CC_{2.5}}$ from the Slot 1 connector: FERR#, IERR#, THERMTRIP#, TDO. Unused outputs may be left as a no-connect. The pull-up resistor values should take into consideration the LAI recommendation in section 7.3.1.

12. The following open drain bi-directional signals must be pulled up to $V_{CC2.5}$ to/from the Slot 1 connector: PICD[1:0]#. Consider the LAI recommendation in section 7.3.1. when choosing pull-up resistors.
13. The following clocks must be $V_{CC2.5}$ going to the Slot 1 connector: PICCLK, BCLK and TCK.
14. The Pentium II processor ITP port has redefined pin (29) as BCLK, it was previously defined as GND. This clock should be driven from a separate host clock driver.
15. The existing Pentium Pro processor provides support for up to four processors. Slot 1 and the 440LX AGPset only support a maximum of two processors. The Pentium II processor only provides BREQ[1:0] for connection to the host bus.
16. TESTHI (pin A13) must be pulled-up to $V_{CC2.5}$ (1 kohm to 10 kohm). TESTHI for the Pentium Pro processor was previously required to be pulled-up directly to V_{CCP} or through a 10 kohm resistor.
17. The Pentium Pro processor requires high frequency decoupling on the motherboard, 40 1 µF capacitors are recommended. The Pentium II processor has high frequency decoupling on the processor so no additional high frequency decoupling should be required for a properly designed power delivery system. Please see the reference and *Pentium II Processor/Slot 1 Data Sheet* for recommendations and requirements for the Slot 1 connector.
18. The Pentium II processor has a new signal called SLP#. If a more advanced level of power management is desired, this signal can be connected from the PIIX4 to the Slot 1. If this signal is not used, it should be pulled up to $V_{CC2.5}$ with a 150 ohm to 330 ohm resistor.
19. The Slot 1 connector has a new signal called 100/66#. This signal must be a grounded on an Intel 440LX AGPset based motherboard.
20. The Slot 1 connector has reserved the pin placement (Pin B14 and B15) for a thermal sensor on future Pentium II processors. These signals should be left as a no connect.
21. The Slot 1 connector has a new signal called SLOTOCC#, this is similar to the function of the CPUPRES# pin on the existing Pentium Pro processor, in that it is a ground on the Pentium II processor. The signal is used to inform motherboard logic that a processor or termination card is present with GTL+ termination. The presence of a CPU core can be determined from the V_{ID} signals, all ones designates “No Core.”
22. The Pentium II processor has the GTL+ termination resistors on the processor. For dual end termination UP designs a second set of termination resistors should be placed on the motherboard. For single end termination designs reference appendix F. Dual-processor (DP) systems must not have GTL+ termination’s on the motherboard. A terminator card is required if only a single processor is installed in a dual processor system. “GTL+” is the technology used for the bus signaling between the Pentium II processor and the 440LX AGPset. The GTL+ bus and the Pentium II processor bus are synonymous. For more information see Pentium Pro family developers manual (see figure below).

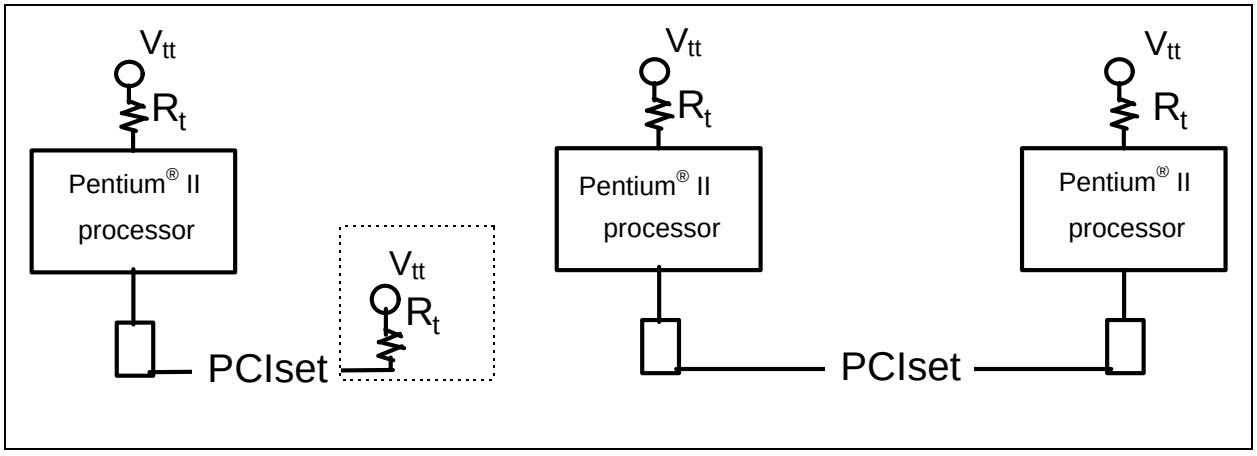


Figure 4-1. GTL+ Termination Locations

23. Unlike the requirements for the Boxed Pentium Pro processor, motherboards designed for use with the Boxed Pentium II Processor should provide a matched power header for the Boxed Pentium II processor fan/heatsink power cable connector. Please consult the *Pentium II Processor/Slot 1 Data Sheet* for specifications of the fan power cable connector. The power header must be positioned within close proximity to the Slot 1 connector.
24. The Pentium II processor and the Boxed Pentium II processor require mounting holes for the retention mechanism and heat sink support. Please see the *Pentium II Processor/Slot 1 Data Sheet*.
25. The PIIX4 provides an SMBus interface.
26. The PAC provides a configurable memory interface and supports SDRAM. Please see the reference schematics and the *Intel 440LX AGPset Data Sheet* for further details.
27. The PIIX4 provides additional power management signals. Please see the reference schematics for details.

5

Motherboard Layout and Routing Guidelines

CHAPTER 5
MOTHERBOARD LAYOUT AND ROUTING GUIDELINES

5. Motherboard Layout and Routing Guidelines

This section describes layout and routing recommendations that should be followed to insure a robust design. These guidelines should be followed as closely as possible. Any deviations from the guidelines listed here should be simulated to insure adequate margin is still maintained in the design.

5.1 Placement

The pins on the 440LX AGPset components have been assigned in order to simplify routing and keep board reduce fabrication cost by enabling a 4-layer "UP" motherboard design. Figure 5-1 shows the signal quadrants of the 82443LX. The component placement on the motherboard with this in mind. This will simplify routing and minimize the number of signals that cross. The individual signals within the respective groups have also been placed in order to simply route with only 2 PCB layers.

A complete list of signals and ball assignment can be found in the *82443LX PAC Data Sheet.*

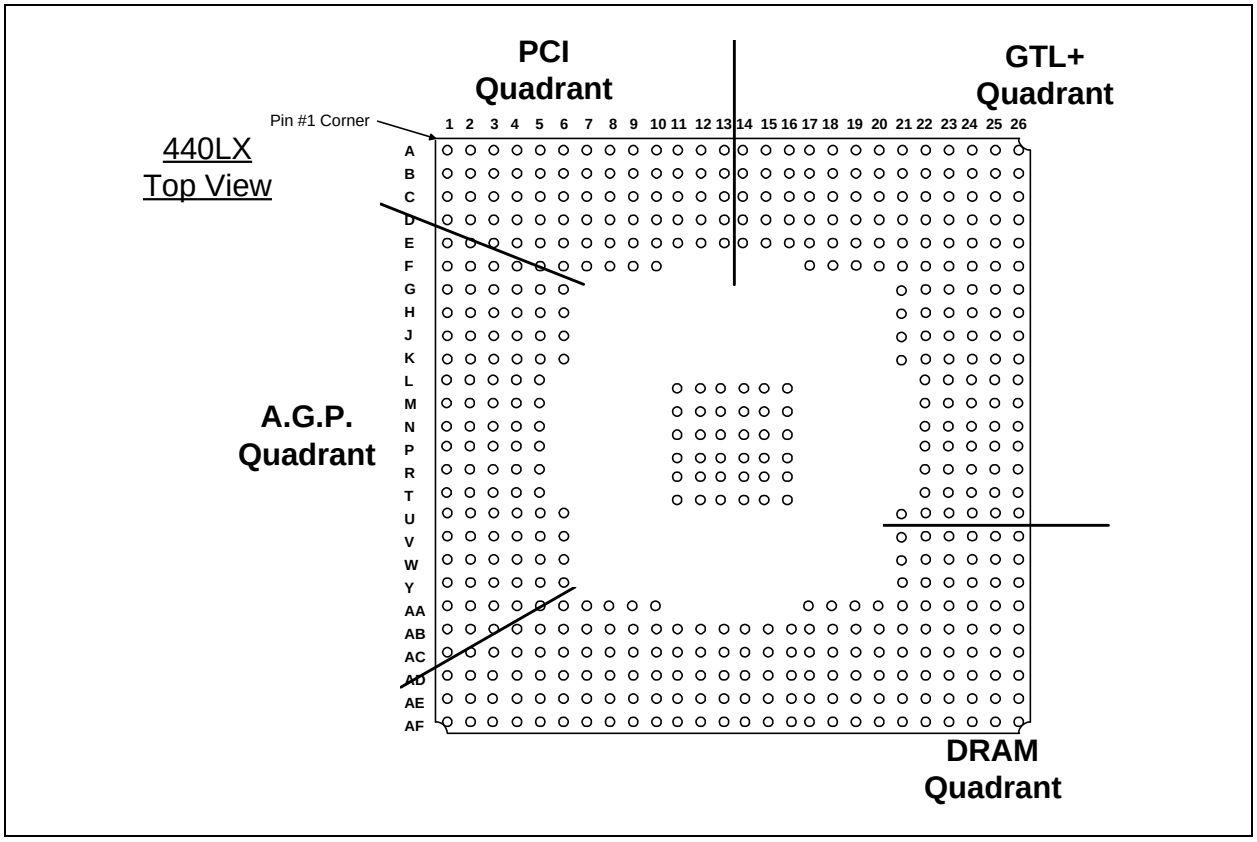


Figure 5-1. Signal Quadrants

Examples of the proposed component placement for single Pentium II processor designs are shown in Figure 5-2 and 5-3 for both an ATX and NLX form factor design.

ATX Form Factor:

1. The ATX placement and layout Figure 5-2 is recommended for single (UP) Pentium II processor 440LX system design.
2. The example placement Figure 5-2 shows 4 PCI slots, 2 ISA slots, 3 DIMM sockets, and one A.G.P. connector.
3. For an ATX form factor design, the A.G.P. compliant graphics device can be on the motherboard (device down option) or on an A.G.P. connector (device up option).
4. The trace length limitation between critical connections will be addressed later in this document.
5. The Figure 5-2 is for reference only and the trade-off between the number of PCI and ISA slots, number of DIMM sockets, and other motherboard peripherals needs to be evaluated for each design.

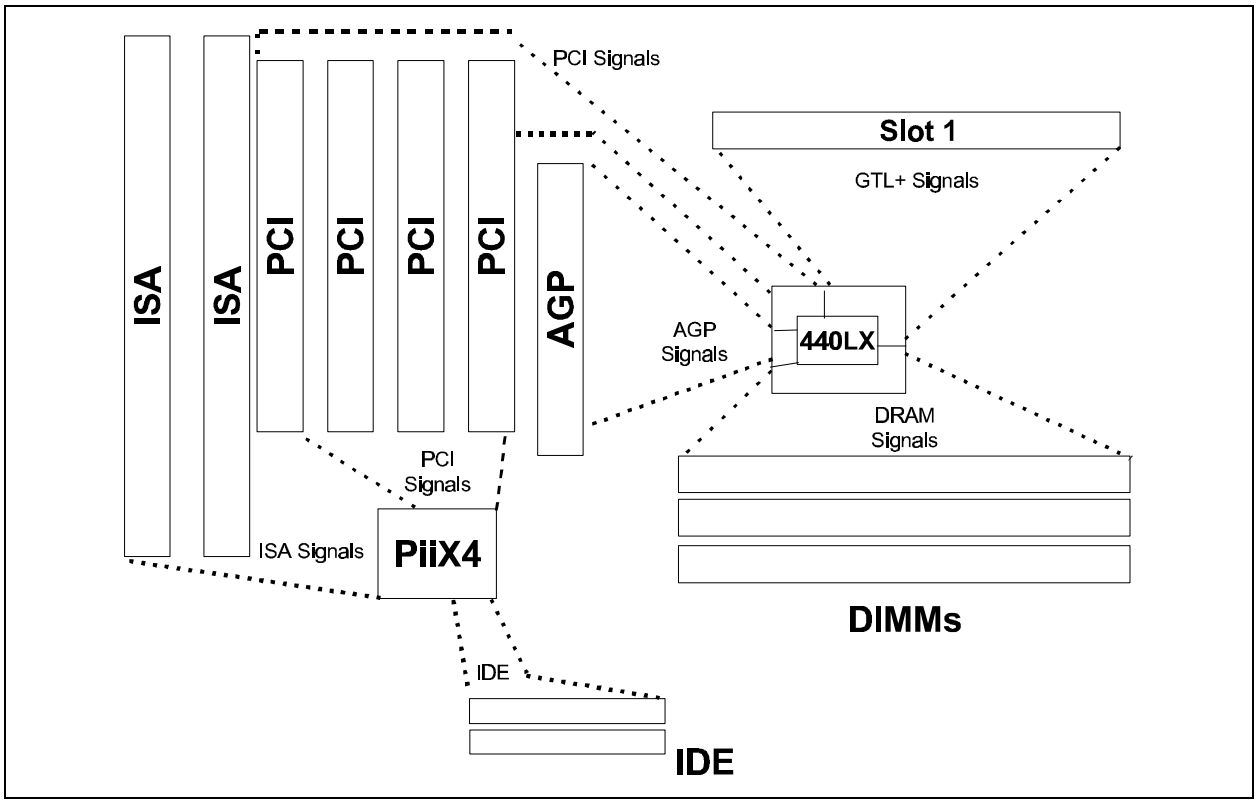


Figure 5-2. Example ATX Layout for a UP Pentium® II/440LX Design

NLX Form Factor:

1. The NLX placement and layout below is recommended for a single (UP) Pentium II/440LX system design.
2. The example placement below shows one Slot 1 connector, 3 DIMM sockets, and A.G.P. compliant device down.
3. For an NLX form factor design, the A.G.P. compliant graphics device may readily be integrated on the motherboard (device down option).
4. The trace length limitation between critical connections will be addressed later in this document.
5. The figure below is for ***reference only*** and the trade-off between the number of DIMM socket, and other motherboard peripherals need to be evaluated for each design.

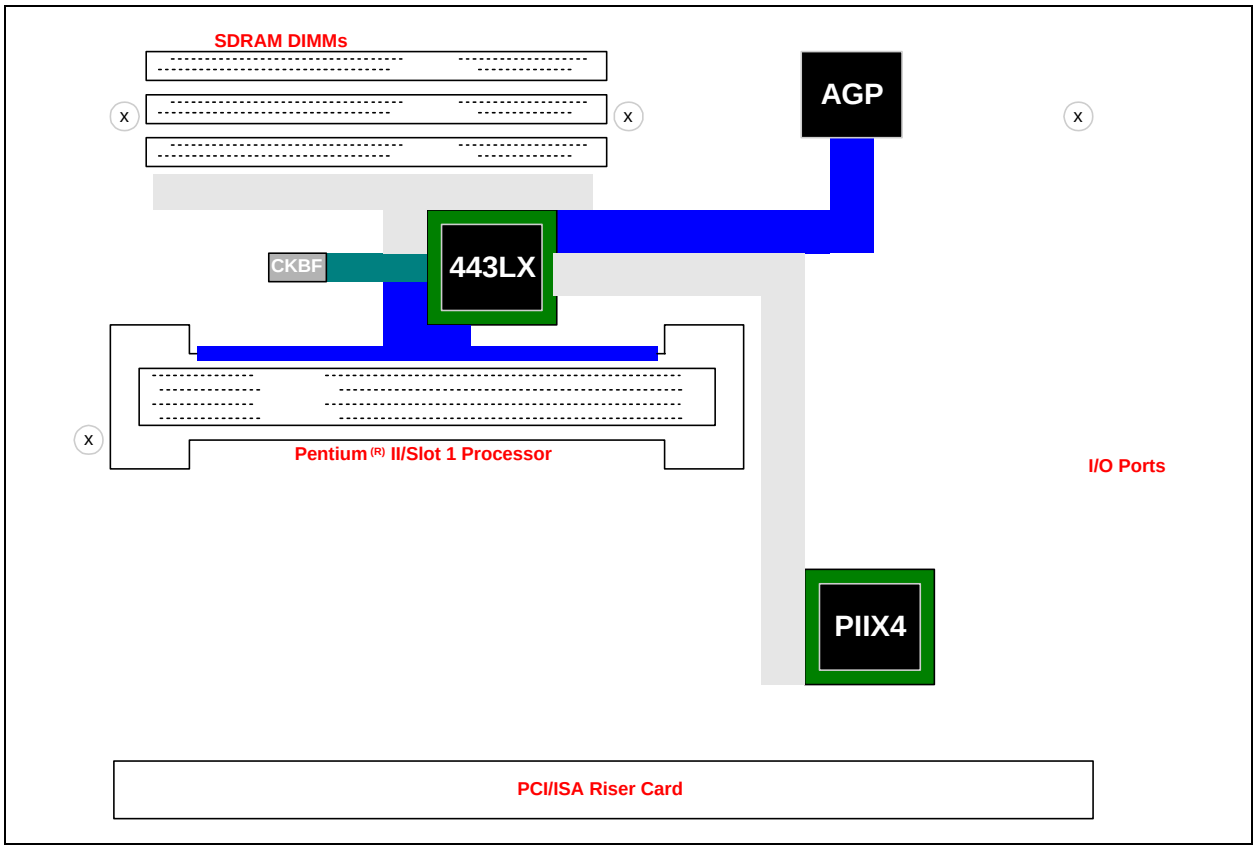


Figure 5-3. Example NLX Placement for a UP Pentium® II processor/440LX Design

Note:

AGP can also be on the riser card.

5.2 Board Description

For a single Pentium II processor/440LX AGPset motherboard design, a 4 layer stack-up arrangement is recommended. The stack up of the board is shown in Figure 5-4. The impedance of all the signal layers must be between 50 and 80 ohms. Lower trace impedance will reduce signal edge rates, reduce over & undershoot, and will create less crosstalk. Higher trace impedance will increase edge rates and may slightly decrease signal flight times.

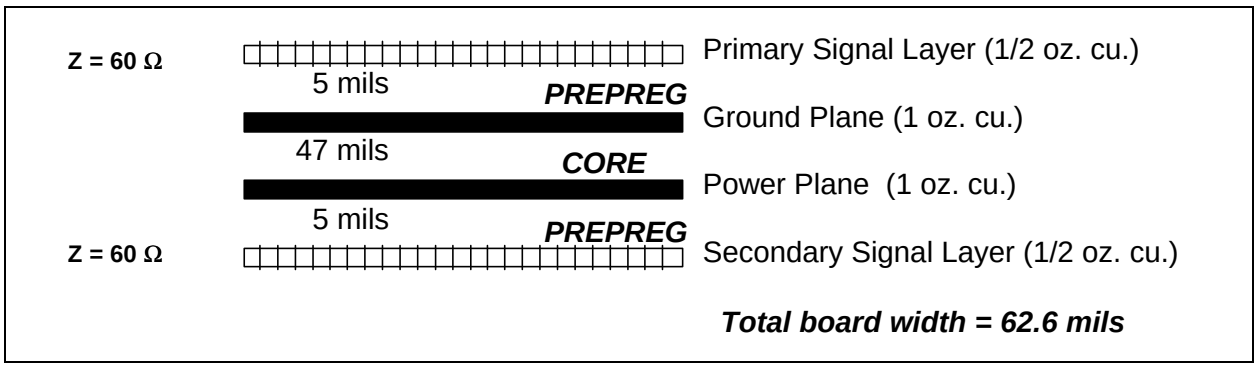


Figure 5-4. Four Layer Board Stack-up

Note that the top and bottom routing layers specify 1/2 oz. cu. However, after plating, the traces will be 1 oz. cu. Please check with your fab vendor on the exact value and insure that any signal simulation is performed.

Note:

A thicker core helps reduce board warpage.

The Intel 440LX Uni-Processor reference design has been successfully routed on a 4 layer board. If more signal layers are necessary one of the six layer stack-up should be used. For DP designs a six layer stack-up is recommended. Two examples are shown below. The first example has 4 signal layers, 1 power plane and 1 ground plane. The second example shows 3 signal plane layers, 2 power planes and 1 ground plane. The second option makes it easier to accommodate all of the power planes required in a 440LX design.

If a 6 layer stack-up is used, route the GTL+ bus signals on the inner layers. The primary and secondary signal layer can be used for GTL+ signals where needed. On the two inner layers (Figure 5-5) route orthogonally to reduce crosstalk.

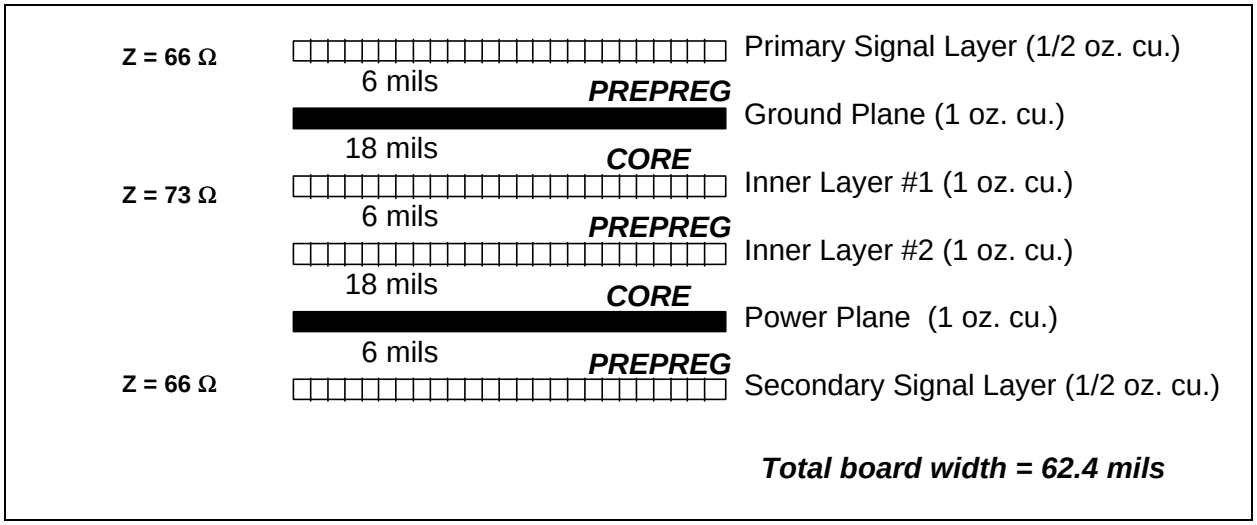


Figure 5-5. Six Layer Board Stack-up with 4 signal planes, 2 power planes

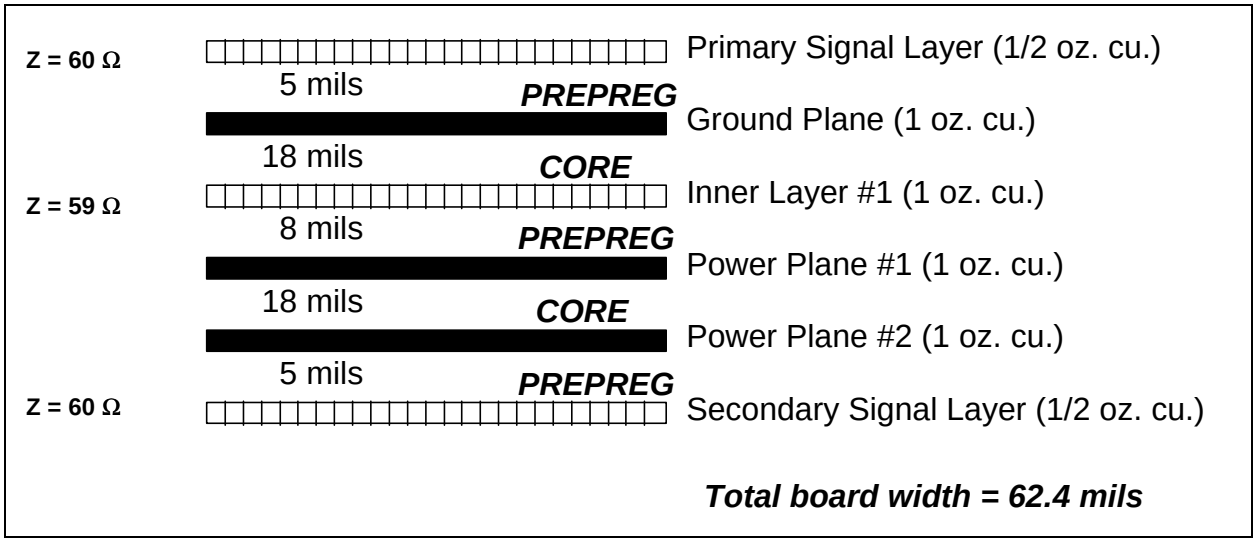


Figure 5-6. Six Layer Board Stack-up with 3 signal planes, 3 power planes

Additional guidelines on board buildup, placement and layout include:

- Dual ended termination is recommended for GTL+ signals. One set of termination resistor is present on the Pentium II processor, and the other set of termination resistors are on the motherboard. For single end termination please see appendix F.
- For a 6-layer dual processors design, no termination is required on the motherboard, as each end of the GTL+ bus is terminated on each Pentium II processors. If a single Slot 1 is populated in a DP design, the second Slot 1 must be populated with a termination card.
- The termination resistors on the GTL+ bus should be 56 ohms.
- The board impedance (Z) should be 65 ohms ± 20%.
- FR-4 material should be used for the board fabrication.
- The ground plane should not be split. If necessary, it is acceptable to route a signal on the power plane, but only for very short distance.
- Place vias for decoupling capacitors as close to the capacitor pads as possible.

5.3 Ball Grid Array (BGA) Component

This section addresses the breakout of the 492 BGA PAC.

5.3.1 BGA Pad Size

The PAC contains 6 rows of balls. To break out from the package route two traces between pads to achieve a 4 layer motherboard design. Figure 5-7 shows routing examples for 24 mil and 20 mil ball pads. To route two traces between 24 mil pads, 5 mil traces and 5 mil spaces are required for a 24 mil pad size. To route two traces between 20 mil pads, 6 mil traces and 6 mil spacing can be used. Either pad size is acceptable, so the pad size tradeoff should be determined by the manufacture. If larger trace widths are desired, another alternative is to route 5/5 or 6/6 within the BGA pads, and then “neck up” to the larger trace widths once you have cleared the BGA component area.

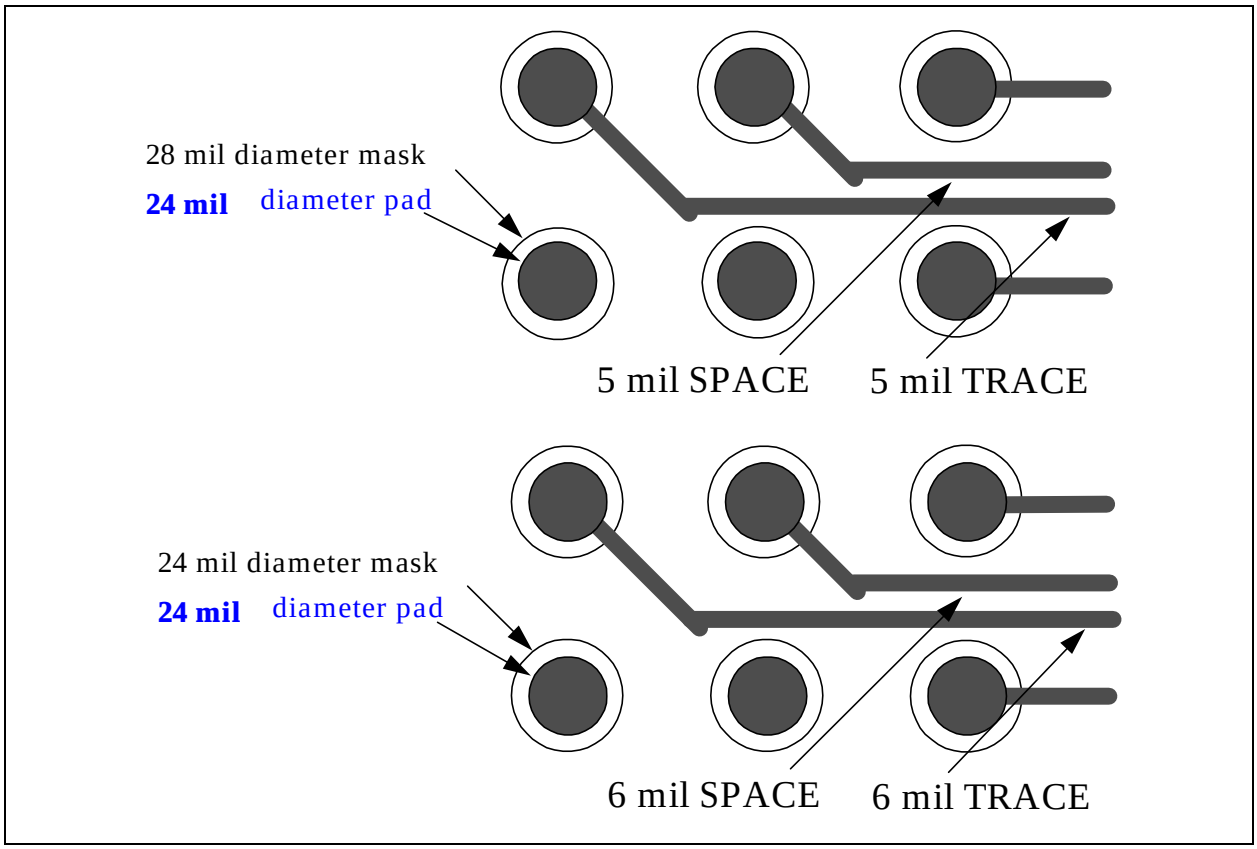


Figure 5-7. Routing Example for 24 mil and 20 mil Ball Pads

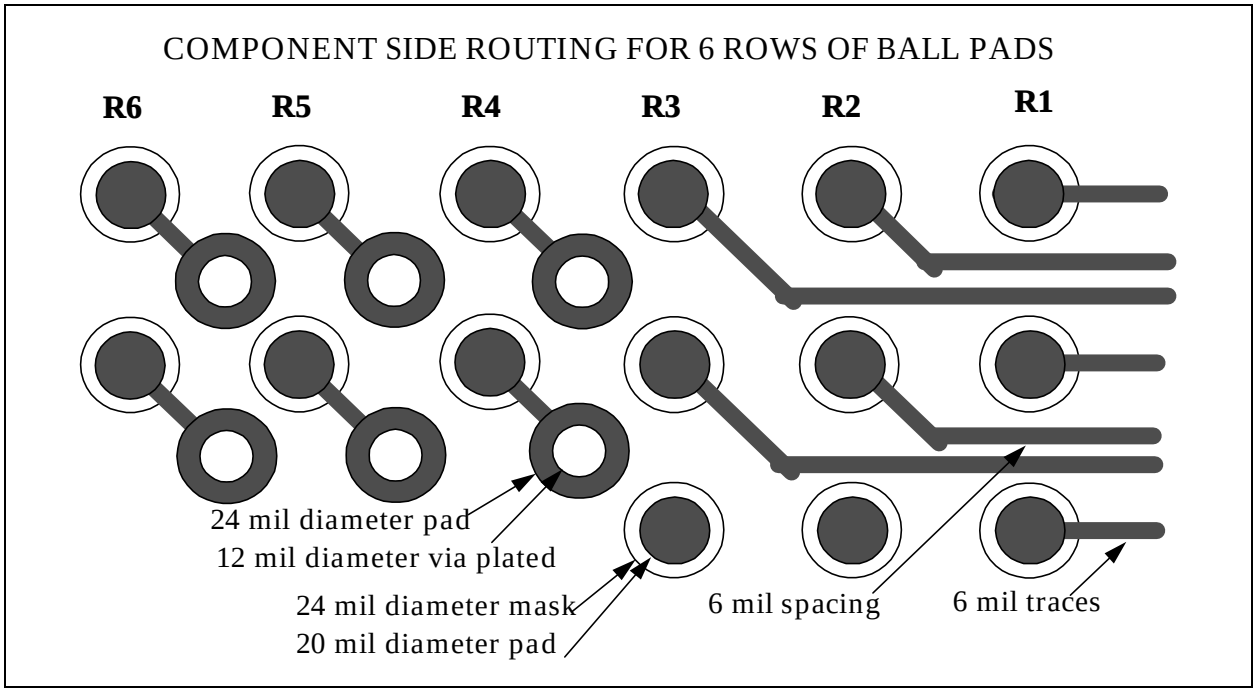


Figure 5-8. BGA Routing Example

Using the routing examples shown in Figure 5-7 and Figure 5-8, the first 3 rows of balls can be routed on the top signal layer. The inner two rows (R4 & R5) must be routed on the bottom side or the inner layers of a 6-layer board. As a result, vias are required in between the BGA pads. The vias will be discussed in the next section. **NOTE**: The inner most row of balls on the PAC (R6 in the figure above) are power balls or ground balls. These balls will require vias to connect them to their proper plane layer.

5.3.2 BGA Vias

Figure 5-9 shows the connection between the BGA pad and a via. **All vias located between the BGA pads must be covered with solder mask!** This prevents solder from wicking to the vias pad. A 24 mil via pad size is recommended.

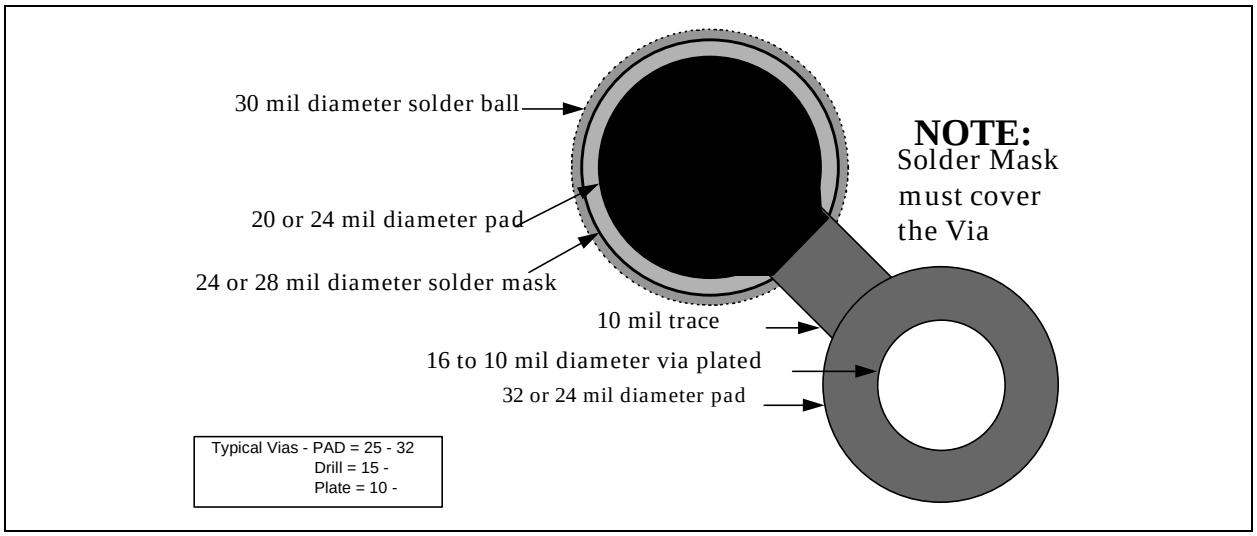


Figure 5-9. BGA Pads and Vias

5.3.3 BGA Routing

Figure 5-10 and Figure 5-11 show routing example for the component and solder sides of a 4 layer board. The first three rows are routed on the component side, while the inner three rows are routed on the solder side. The examples shows 6 mil trace widths.

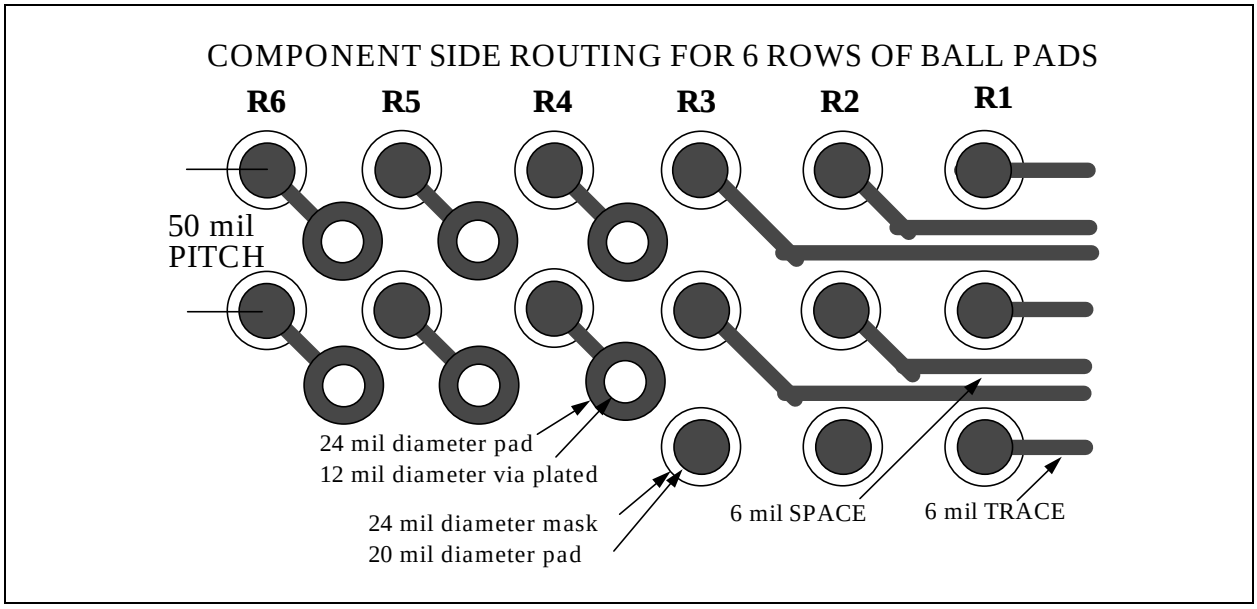


Figure 5-10. BGA Component Side Routing Example

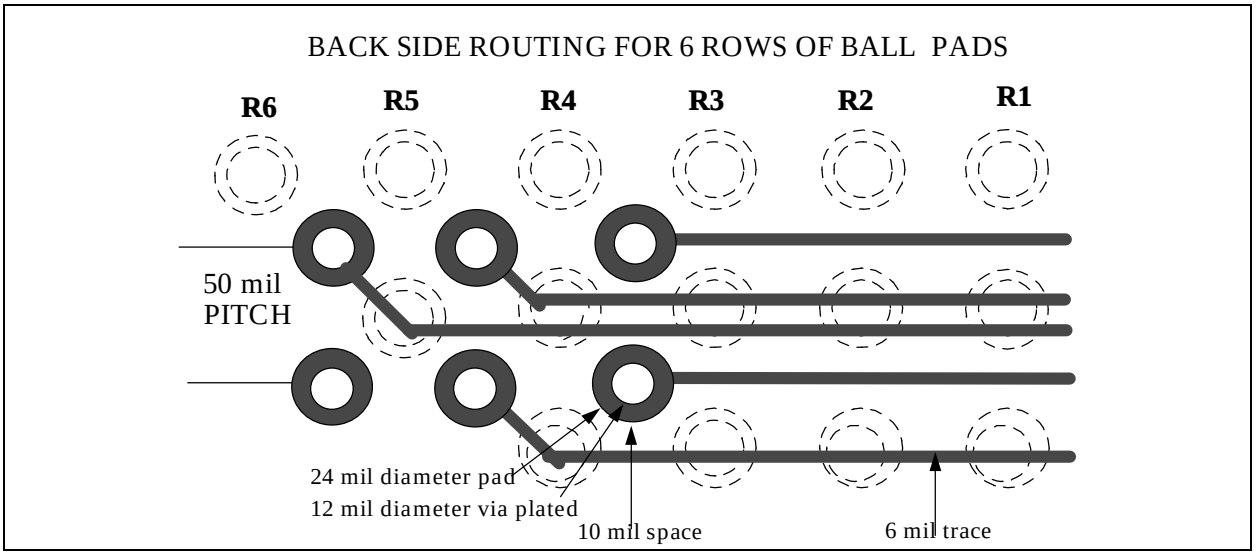


Figure 5-11. BGA Solder Side/Inner Layer Routing Example

5.4 Routing Guidelines

If the guidelines are not followed then it is imperative that you simulate your design. If the guidelines are followed, simulation is still recommended. Contact your Intel Field Representative for IBIS Models.

5.4.1 Host Bus Layout and Routing Guidelines

The GTL+ routing guidelines were developed through simulation of the Pentium II processor/440LX interconnect.

Single Processor (UP) Layout Guidelines:

- Slot 1 connector to the beginning of the GTL+ termination stub: 1.5” min and 10” max.
- The GTL+ termination stub is not a critical trace and can be as much as 6”.
- PAC to the beginning of the GTL+ termination stub: 1.5” max.
- For single end termination designs see appendix F.

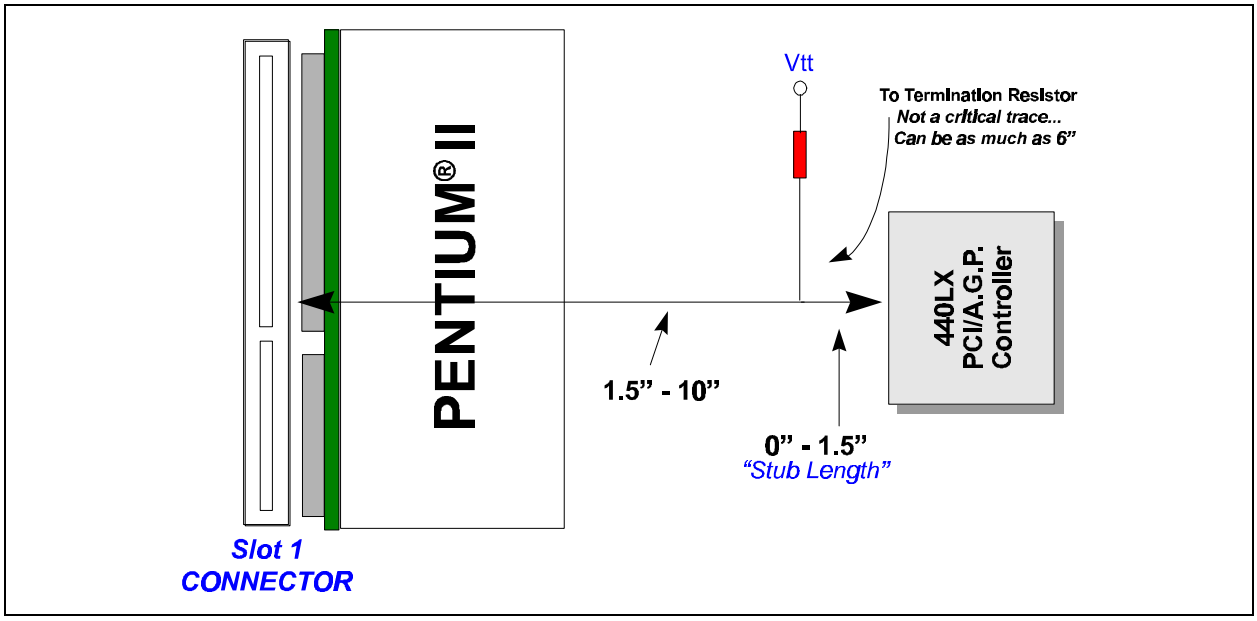


Figure 5-12. "UP" Layout

Dual Processor Layout Guidelines:

- Slot 1 to Slot 1: 3" min to 14" max.
- PAC Stub Length: 1.5" max.

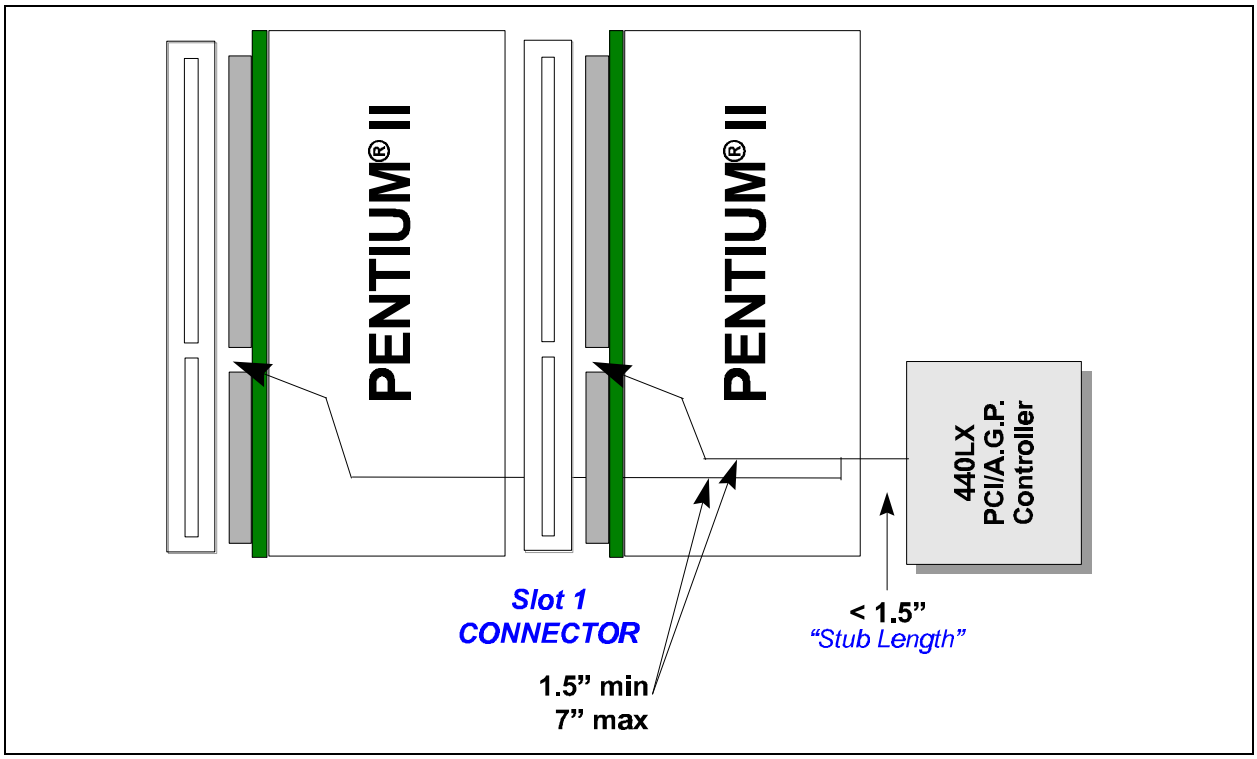


Figure 5-13. "DP" Layout

5.4.2 A.G.P. Layout and Routing Guidelines

For the definition of the A.G.P. Interface functionality (protocols, rules and signaling mechanisms, as well as the platform level aspects of A.G.P. functionality), refer to the latest *A.G.P. Interface Specification*. This section describes 440LX platform recommendations for the A.G.P. interface. Refer to AGP Interface Specification revision 1.0 for more information.

The PAC A.G.P. implementation is compliant with the Accelerated Graphics Port Interface Specification Rev. 1.0. The PAC supports only synchronous A.G.P. interface, coupling to the host bus frequency. The A.G.P. interface can reach a theoretical 532-Mbytes/sec transfer rate. The actual bandwidth will be limited by the capability of the PAC memory subsystem.

Throughout this section the term “data” refers to AD[31:0], C/BE[3:0]# and SBA [7:0]. The term “strobe” refers to AD_STB[1:0] and SB_STB.

Table 5-1A. Associated Data and Strobe

Associate Data	Strobe
AD[15:0] and C/BE[1:0]#	AD_STB0
AD[31:16] and C/BE[3:2]#	AD_STB1
SBA[7:0]	SB_STB

A.G.P. Connector (“Up Option”) Layout Guidelines:

The maximum line length is dependent on the routing rules used on the motherboard. These routing rules were created to give design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. These routing rules are divided by trace spacing. In 1:1 spacing, the distance between the traces (air gap) is the same as the width of traces. In 1:2 spacing, the distance between the traces is twice the width of the traces.

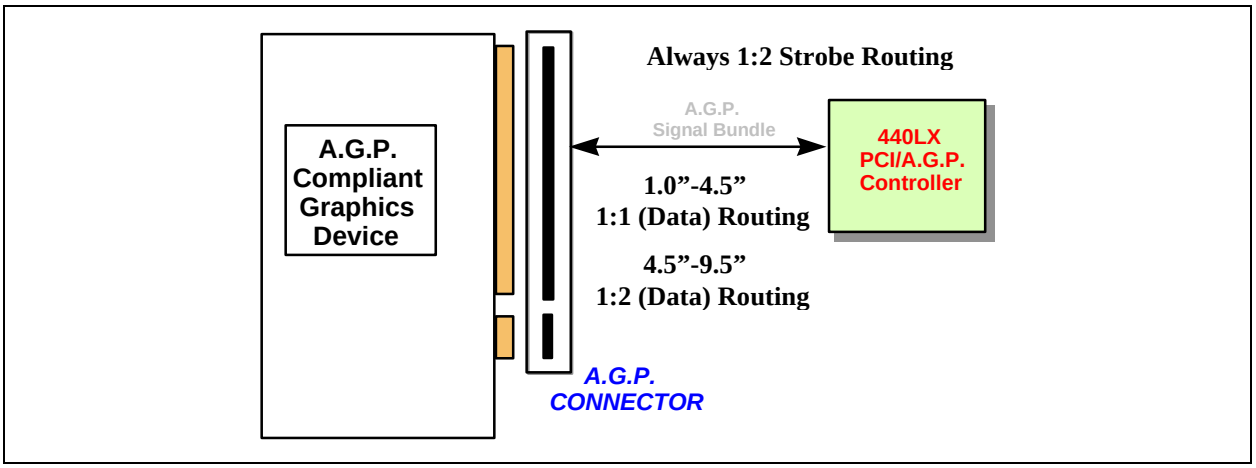


Figure 5-14. A.G.P. Connector Layout Guidelines

For trace lengths that are between 1.0” and 4.5”, a 1:1 trace spacing is recommended for data lines. The strobe requires a 1:2 trace spacing. This is for designs that require less than 4.5 inches between the A.G.P. connector and the A.G.P. target.

Longer lines have more crosstalk. Therefore in order to maintain skew, longer line lengths require a greater amount of spacing between traces. For line lengths greater than 4.5” and less than 9.5”, 1:2 routing is recommended for all data lines and strobes. For all designs, the line length mismatch must be less than 0.5”, and the strobe must be the longest signal of the group.

Reduce line length mismatch to insure added margin. In order to reduce trace to trace coupling (crosstalk), separate the traces by as much as possible.

Table 5-1B. Source Synchronous Routing Recommendations

Width:Space	Trace	Line Length	Line Length Matching
1:1(Data) / 1:2 (Strobe)	Data / Strobe	1.0” < line length < 4.5”	-0.5”, strobe longest trace
1:2	Data / Strobe	1.0” < line length < 9.5”	-0.5”, strobe longest trace

The clock lines on the motherboard can couple with other traces. It is recommended that the clock spacing (air gap) be at least twice the trace width to any other traces. It is also strongly recommended that the clock spacing be at least four times its trace width to any strobes.

The clock lines on the motherboard need to be simulated to determine the proper line length. The motherboard needs to be designed to the characteristics of clock driver that is being used and motherboard trace topology. These clocks need to meet the loading of the receiving device as well as the add-in trace length.

Additionally, control signals less than 8.5 inches can be routed 1:1. Control signals (non-data signals) greater than 8.5 inches should be routed 1:2.

Table 5-1C. Control Signal Routing Recommendations

Width:Space	Board	Trace	Line Length	Pull-up Stub Length
1:1	Motherboard	Control signals	1.0” < line length < 8.5”	< 0.5” (Strobes < 0.1”)
1:2	Motherboard	Control signals	1.0” < line length < 10.0”	< 0.5” (Strobes < 0.1”)
1:2 (1:4 to Strobe)	Motherboard	Clock		

Some of the control signals require pull-up resistors to be placed on the motherboard. A.G.P. signals must be pulled up to $V_{CC3.3}$ using 8.2 kohm to 10 kohm pull-up resistors (refer to section 7.2.6 A.G.P. Signals Checklist). Pull-up resistors should be discrete resistors, as resistor packs will need longer stub lengths and may break timings. The maximum stub length on a strobe trace is 0.1 inch. The maximum stub trace length on all other traces is 0.5.”

On-board A.G.P. Compliant Device (“Down Option”) Layout Guidelines:

Routing guidelines for the device ‘down’ option are very similar to those when using a connector.

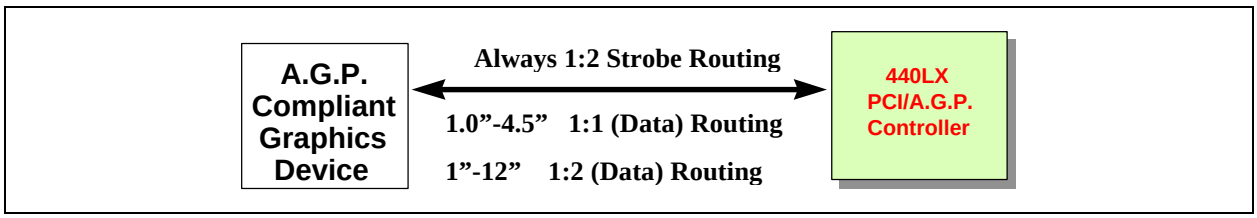


Figure 5-15. On-board A.G.P. Compliant Device Layout Guidelines

For trace lengths that are between 1.0” and 4.5”, a 1:1 trace spacing is recommended for data lines. The strobe requires a 1:2 trace spacing. This is for designs that require less than 4.5 inches between the A.G.P. connector and the A.G.P. target.

Longer lines have more crosstalk. Therefore in order to maintain skew, longer line lengths require a greater amount of spacing between traces. For line lengths greater than 4.5” and less than 9.5”, 1:2 routing is recommended for all data lines and strobes. For all designs, the line length mismatch must be less than 0.5”, and the strobe must be the longest signal of the group.

Table 5-1D. Source Synchronous Routing Recommendations

Width:Space	Trace	Line Length	Line Length Matching
1:1(Data) / 1:2 (Strobe)	Data / Strobe	1.0” < line length < 4.5”	-0.5”, strobe longest trace
1:2	Data / Strobe	1.0” < line length < 12.0”	-0.5”, strobe longest trace

The clock lines on the motherboard can couple with other traces. It is recommended that the clock spacing (air gap) be at least twice the trace width to any other traces. It is also strongly recommended that the clock spacing be at least four times its trace width to any strobes.

The clock lines on the motherboard need to be simulated to determine the proper line length. The motherboard needs to be designed to the characteristics of clock driver that is being used and motherboard trace topology. These clocks need to meet the loading of the receiving device as well as the add-in trace length.

Additionally, control signals less than 8.5 inches can be routed 1:1. Control signals greater than 8.5 inches should be routed 1:2.

Table 5-1E. Control Signal Line Length Recommendations

Width:Space	Board	Trace	Line Length	Pull-up Stub Length
1:1	Motherboard	Control signals	1.0” < line length < 8.5”	< 0.5” (Strobes < 0.1”)
1:2	Motherboard	Control signals	1.0” < line length < 12.5”	< 0.5” (Strobes < 0.1”)
1:2 (1:4 to Strobe)	Motherboard	Clock		

Some of the control signals require pull-up resistors to be installed on the motherboard. A.G.P. signals must be pulled up to $V_{CC3.3}$ using 8.2 kohm to 10 kohm pull-up resistors (refer to section 4.2.6 A.G.P. Signals Checklist). Pull-up resistors should be discrete resistors, as resistor packs will need longer stub lengths and may break timings. The maximum stub length on a strobe trace is 0.1”. The maximum stub trace length on all other traces is 0.5.”

5.4.3 440LX Memory Subsystem Layout and Routing Guidelines

The 440LX integrates a fully configurable main memory DRAM controller that supports a 72-bit memory data interface (64-bit memory data plus 8 ECC bits). The PAC supports Extended Data Out (EDO) DRAM, and Synchronous DRAM (SDRAM). The PAC generates the Row Address Strobe/Chip Selects (RCSA# and RCSB#), Column Address Strobe/Data Mask (CDQA# and CDQB#), SCAS#, SRAS#, CKE, WE#, and Memory Addresses (MA) for the DRAM array. For CPU/PCI/A.G.P.-to-DRAM cycles the address and data flows through the PAC. The PAC generates data on the MD and MECC buses for writes and accepts data on these buses during reads. The PAC asserts ECCERR#, if enabled, in the event of a single-bit correctable or multi-bit uncorrectable error. The 440LX DRAM interface operates synchronously to the CPU clock.

Fourteen memory address signals allow the PAC to support a wide variety of DIMMs. Both symmetrical and asymmetrical addressing are supported. Eight RCS# lines permit a maximum of eight 64-bit wide rows of DRAM. For write operations of less than a quad word, the PAC will either perform a byte-wise write (non ECC protected configuration) or a read-modify-write cycle by merging the write data on a byte basis with the previously read data (ECC configurations). The PAC supports 50 ns and 60 ns EDO DRAM and 66-MHz SDRAM with CL2 and CL3. Both single and double-sided DIMMs are supported.

Possible DRAM and system options supported by the 440LX AGPset include:

Table 5-2. Memory Types Supported by the 440LX

DRAM Type:	EDO, SDRAM
DRAM Module Type:	168-pin DIMM: 64-bit, 72-bit ECC, unbuffered
DRAM Voltage:	3.3V
Number of rows of memory:	8 rows (Configuration #1), 6 rows (Configuration #2).
DRAM Speed:	50 ns & 60 ns EDO DRAM, 66-MHz SDRAM
DRAM Component Width:	x4, x8, x16

In the following discussion the term *row* refers to a set of memory devices that are simultaneously selected by a RCSA&B#/CS# signal. The PAC supports a maximum of 8 rows of memory in configuration #1, or 6 rows in memory configuration #2.

The PAC supports "4-Clock 66-MHz 64/72-bit unbuffered SDRAM DIMM" Specification and the "60 ns 64-bit 3.3V unbuffered EDO DIMM" specification. Ask your local Intel Field Sales Engineer for these documents.

Populating a 440LX Memory Array:

- DIMM sockets can be populated in any order. However, to take advantage of potentially faster MA timing, it is recommended to populate sockets in order.
- SDRAM and EDO DIMMs can be mixed within the memory array.
- The DRAM Timing register, which provides the DRAM speed grade control for the entire memory array, must be programmed to use the timings of the slowest DRAMs installed.

440LX Memory Array Configurations:

- Large Memory Array (Configuration #1)
  - 512 Megabytes SDRAM/EDO
  - 1 Gigabyte Buffered EDO
  - 8 Rows
- Small Memory Array (Configuration #2)
  - 384 Megabytes SDRAM/EDO
  - 6 Rows

Each memory configuration offers a different set of signals. This memory configuration is selectable upon Boot/RESET by a strapping option on the CKE signal (please refer to the CKE signal description in the *Intel 82443LX PAC Data Sheet*.

Configuration #1: Enables large memory arrays (up to 8 rows) with two copies of Row Address Strobe/Chip Selects (RCSAx# & RCSBx#) and an extra copy of the Column Address Strobe/Data Mask 5 & 1, (CDQB[5 & 1]# are the most loaded CAS#/DQM signals when using ECC DIMMs). Four SRAS#, SCAS# and WE# signals are also provided. This configuration supports Single-Sided and Double-Sided x8, x16 and x32 DIMMs, and Single-Sided x4 DIMMs.

Configuration #1 interface signals:

In memory configuration #1, a buffered copy of MA[13:2] will go to all 4 DIMM sockets. MAA[1:0] will go to DIMM socket 0 and DIMM socket 1, and MAB[1:0] will go to DIMM socket 2 and DIMM socket 3. CDQA[7:0]# will go to DIMM socket 2 and DIMM socket 3. CDQA[7, 6, 4-2, 0]# will go to DIMM socket 0 and DIMM socket 1. CDQB[5&1]# will go to DIMM 0 and DIMM 1.

One CKE signal, provided by the PAC, is buffered and connected to each DIMM socket. Use a CMOS buffer to provide copies of the CKE signal. Four copies of the WE# signal are provided by the PAC, and one is connected to each DIMM socket.

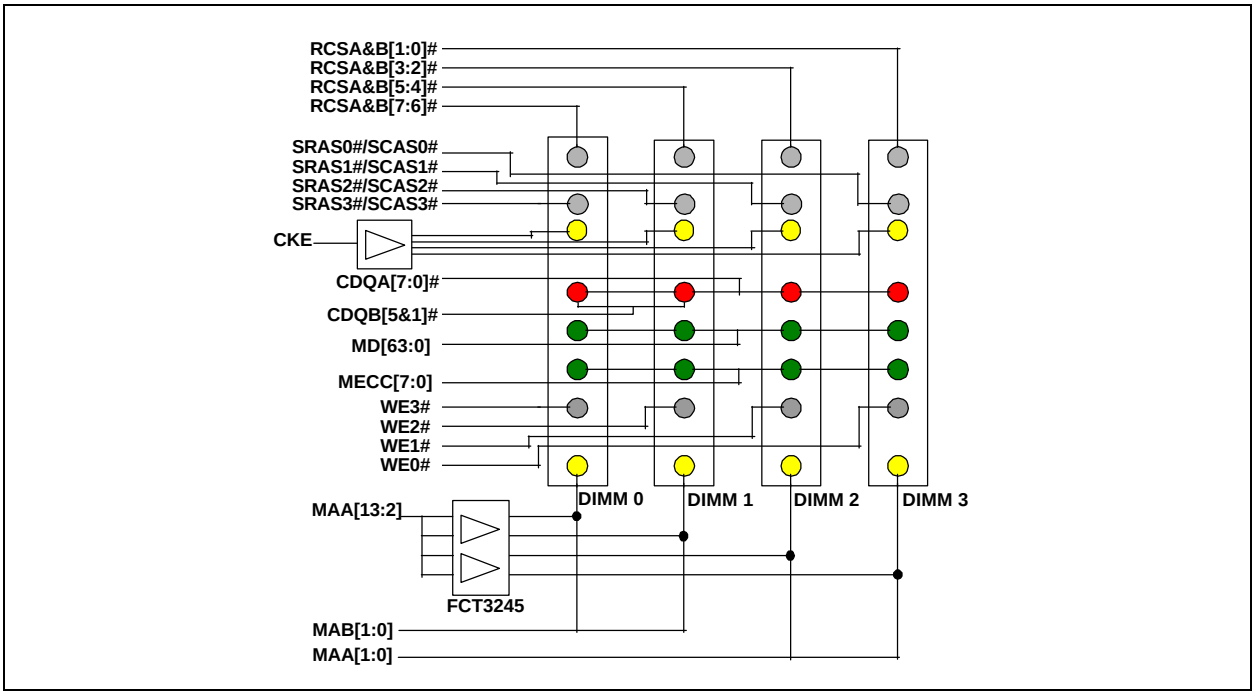


Figure 5-16. DIMM Sockets (Single or Double Sided, Unbuffered)

Figure 5-16 shows a typical 440LX memory array using Configuration #1. The maximum size of this memory array is 512 MB, using x4 single sided EDO DIMMs or 512 MB using x4 SDRAM. (1G is supported by using 4 double sided buffered EDO DIMMs.)

Copies of RCSA#[7:0], CDQA[5]&[1], and WE# are provided to the most heavily loaded control signals in this array. A buffered copy of MAA[13:2] must go to each DIMM socket. MAA[1:0] and MAB[1:0] are copies of the first two memory address signals. Copies of these signals are needed to ensure a fast memory read burst rate.

Layout Guidelines: Minimum trace length (from the PAC to the closest DIMM) is 1.0". Maximum trace length (from the PAC to the furthest DIMM) is 5.0".

Critical Signals: CDQA[7:0]#: "T" in the middle of the array.
CDQB[5],[1]#: "T" to the last 2 DIMMs.
MD[63:0]: "T" in the middle of the array. MECC[7:0]: "T" in the middle of the array.

Configuration #2: Enables small memory arrays (up to 6 rows) with two copies of Memory Address signals. Three SRAS#, SCAS# and WE# signals are provided to support 3 DS DIMM sockets. This configuration supports Single-Sided and Double-Sided x8 and x16 DIMMs.

Configuration #2 interface signals:

In memory configuration #2, connect MAB[13:0] to the DIMM socket closest to the PAC. Connect MAA[13:0] to DIMM sockets 1 and 2. No external buffering is needed on the memory control and address signals.

One CKE signal, provided by the PAC, is buffered and connected to each DIMM socket. Use a CMOS buffer to provide copies of the CKE signal. Three copies of the WE# signal are provided by the PAC, and one is connected to each DIMM socket.

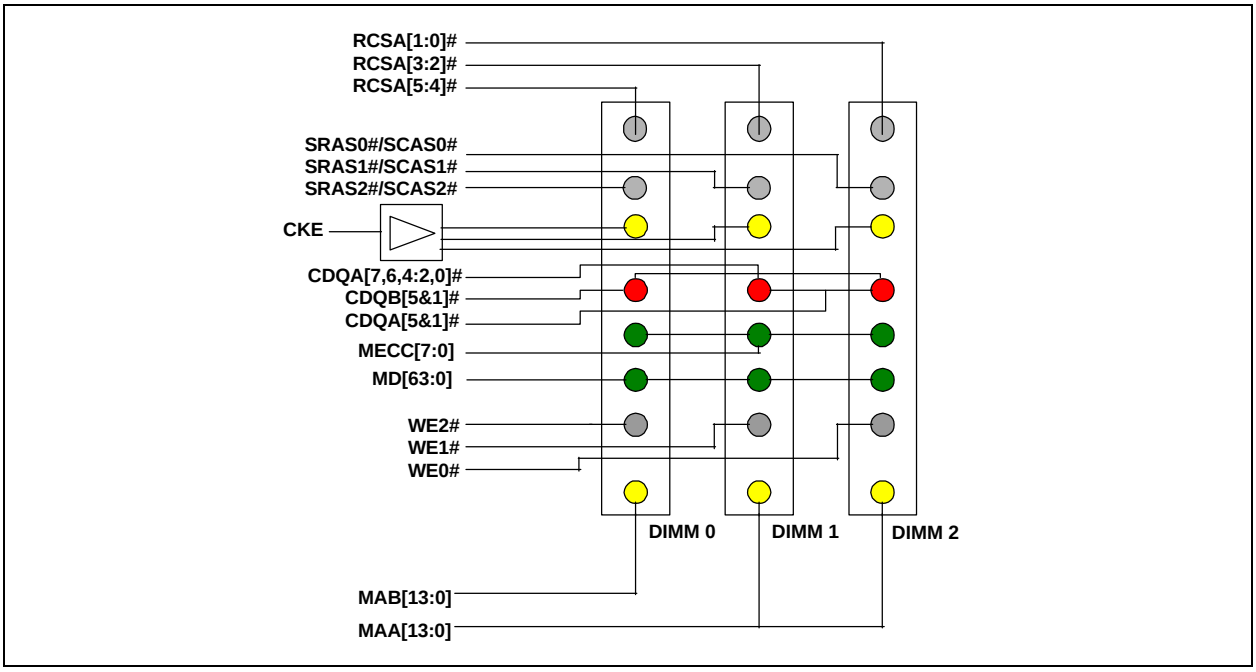


Figure 5-17. DIMM Sockets (Single or Double Sided, Unbuffered)

Figure 5-17 shows a typical 440LX memory array using Configuration #2. Connect MAB[13:0] to the closest DIMM socket to the PAC. Connect MAA[13:0] to DIMM sockets 1 and 2. No external buffering is needed on the memory control and address signals.

Layout Guidelines: Minimum trace length (from the PAC to the closest DIMM) is 1.0." Maximum trace length (from the PAC to the furthest DIMM) is 5.0".

Critical Signals: CDQB[5],[1]#: Must be routed to the closest DIMM, with MAB[13:0].
CDQA[7:0]#: Must be "T" between DIMMs #3 and #2.
MD[63:0]: Must be "T" from the middle of the array.

Termination: Series termination is not required for DRAM interface signals in a 440LX memory array. Adding series termination may cause difficulty in routing to the memory array.

5.4.4 PCI Bus Routing Guidelines

The 440LX provides a PCI Bus interface compliant with the PCI Local Bus Specification 2.1. The implementation is optimized for high-performance data streaming when the PAC is acting as either the target or the initiator of a transaction. For more information on the PAC PCI Bus interface, please refer to the **82443LX PAC Data Sheet**.

A 440LX platform PCI Bus design is basically the same as the 440FX PCIset. The 440LX supports 5 PCI Bus masters (excluding the PAC and PIIX4), by the support of 5 REQ# and 5 GNT# lines (4 PCI Connectors and one on-board PCI Device). Thus a system should only have 4 PCI "add-in" connectors.

Because of the specifics of an ATX layout, see Figure 5-2, it is recommended that the PIIX4 is at the "END" of the PCI bus, as shown in Figure 5-18. This insures proper "termination" of the PCI Bus signals. This is recommended but not required.

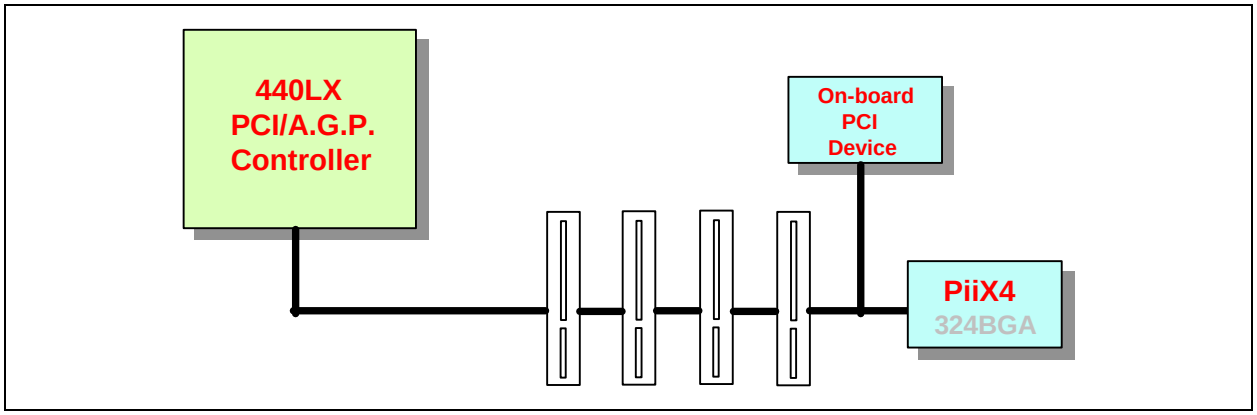


Figure 5-18. PCI Bus layout guidelines

5.4.5 Decoupling Guidelines for a 440LX Platform

Decoupling capacitors should be placed at the corners of the PAC. 0.1 µF and 0.01 µF are recommended at each corner. The host, A.G.P., PCI and DRAM interface can "break-out" from the BGA package on all four sides.

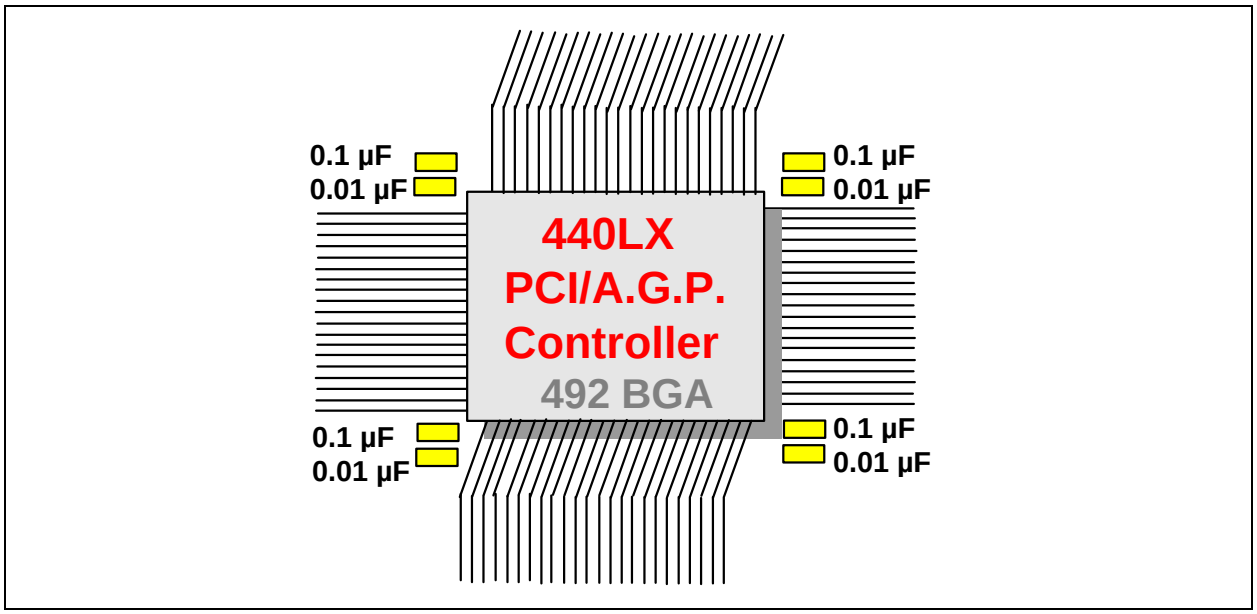


Figure 5-19. PAC Decoupling

Clock Routing Guidelines

A Pentium II/440LX platform will require a different clock synthesizer for different memory configurations. For a dual processor design with 4 DIMM sockets, the system will require 5 CPU clocks (2 CPU clocks, A.G.P., PAC, & ITP), 16 SDRAM clocks, and 6 PCI clocks. For a single processor design with 3 DIMM sockets, the system will require 4 CPU clocks (1 clock for the CPU, the AGP subsystem, the PAC, and the ITP), 12 SDRAM clocks, and 6 PCI clocks. The following figure and table indicates the relative skew requirement for each clock. Each skew requirement may require pin to pin (from the clock synthesizer chip), relative trace length on the motherboard, and the measurement point difference.

Symbol	Description	pin to pin	boards	2.5V - 3.3V	Total
A	Pentium® II(HCLK) to PAC(HCLK) skew	250 ps (max) -250 ps (min)	250 ps (max) 0 ps (min)		500 ps (max) -250 ps (min)
B	PAC(HCLK) to A.G.P. skew	250 ps (max) -250 ps (min)	250 ps (max) 0 ps (min)		500 ps (max) -250 ps (min)
C	PAC(HCLK) to PCI(PCLK) skew	4.0 ns (max) 1.0 ns (min)	1.5 ns (max) 0 ns (min)	500 ps (max) -500 ps (min)	6.0 ns (max) 0.5 ns (min)
D	SDRAM(HCLK) to PAC(HCLK) skew		500 ps (max) 0 ps (min)	500 ps (max) -500 ps (min)	1.2 ns (max) -0.7 ns (min)
E	PAC(HCLK) to APIC(PCLK) skew	4.0 ns (max) 1.0 ns (min)	1.5 ns (max) 0 ns (min)	500 ps (max) -500 ps (min)	6.0 ns (max) 0.5 ns (min)
F	PCI(PCLK) to PCI(PCLK) skew	500 ps (max) -500 ps (min)	1.5 ns (max) -1.5 ns (min)		2.0 ns (max) -2.0 ns (min)

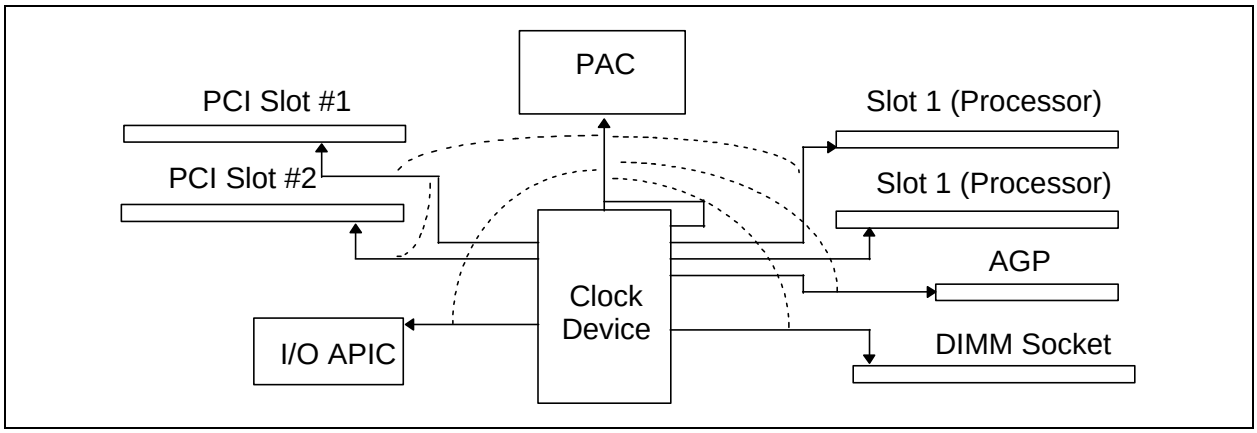


Figure 5-20. Clock skew guidelines.

6

Design Checklists

CHAPTER 6
DESIGN CHECKLISTS

6. Design Checklists

The design checklist provides recommendations and considerations for Pentium II processor/440LX system design. These are provided as a tool to allow the quick debug of 440LX systems.

Design Considerations

Pull-up and pull-down values are system dependent. The appropriate value for your system can be determined from an AC/DC analysis of the pull-up voltage used, the current drive capability of the output driver, input leakage current for all devices on the signal net, the pull-up voltage tolerance, the pull-up/pull-down resistor tolerance, the input high/low voltage specifications and the input timing specifications (RC rise time. An analysis should be done to determine the minimum and maximum values that may be used on an individual signal.)

A simplified DC calculation for a pull-up value is:

R_{MAX} = (VCC_{PU} MIN - V_{IH} MIN) / $I_{Leakage}$ MAX

R_{MIN} = (VCC_{PU} MAX - V_{IL} MAX) / I_{OL} MAX

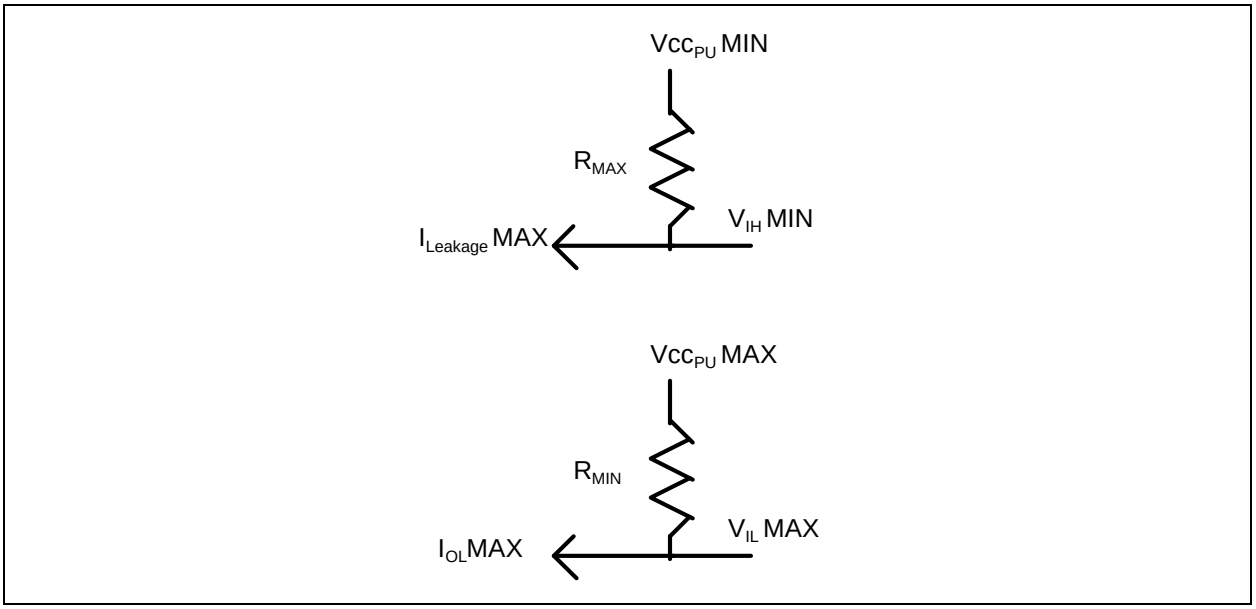


Figure 6-1. Pull-up Resistor Calculation Variables

6.1 Slot 1 Checklist

6.1.1 Pentium II Processor Errata

1. Refer to the *Pentium II Processor Specification Update* for workarounds for any errata.

6.1.2 Slot 1 Clocks

1. Include a circuit that provides the ability to set the host clock to processor core speed ratio.
2. Ensure the clock driver into the Slot 1 connector is 2.5V logic.
3. In a uni-processor system (UP) with an I/O APIC, the PICCLK must be driven to the Slot 1 connector, but it can be driven as fast as 33 MHz. A dual-processor (DP) system utilizing Intel's I/O APIC (82093AA) has a maximum PICCLK frequency of 16 MHz.

6.1.3 Slot 1 Signals

1. Dual termination (56 ohm) to V_{TT} of the GTL+ bus is recommended.
2. IERR# output must be pulled-up to $V_{CC_{2.5}}$ (150 ohm to 10 kohm) if used by system logic. These signals may be wire-ORed and do not require an external gate. They may be left as no-connects if they are not used. Please see section 7.3.1. for further information that may affect these resistor values.
3. The FERR# output must be pulled-up to $V_{CC_{2.5}}$ (150 ohm to 10 kohm) and connected to the PIIX4. Please see section 7.3.1 for further information that may affect these resistor values.
4. PICD[1:0]# must have 150 ohm pull-ups to $V_{CC_{2.5}}$ (even if an I/O APIC is not being used). Please see section 7.3.1 for further information that may affect these resistor values.
5. The SLP# input should be pulled up to $V_{CC_{2.5}}$ (150 ohm to 10 kohm). Please see section 7.3.1 for further information that may affect this resistor value.
6. The Slot 1 connector signal 100/66# must be a grounded on an Intel 440LX AGPset based motherboard.
7. TESTIN# must be pulled up to $V_{CC_{2.5}}$ (1 kohm - 10 kohm).
8. The Slot 1 connector has reserved the pins Pin B14 and B15 for a thermal sensor on future Pentium II processors. These signals should be no connects.
9. Be sure the Slot 1 inputs are not being driven by 3.3V or 5V logic. Logic translation of the 3.3V or 5V signals may be accomplished by using open-drain buffers pulled-up to $V_{CC_{2.5}}$.
10. The PWRGOOD input should be driven from the "AND" of the Power-Good signals from the 5V, 3.3V and $V_{CC_{CORE}}$ supplies. The output of any logic used to drive PWRGOOD should be 2.5V.
11. V_{REF} should not be generated for the Pentium II processor. V_{REF} is locally generated on the processor.
12. V_{TT} must have adequate bulk decoupling based on the reaction time of the regulator used to create V_{TT}. It must provide for a current ramp of up to 8A/µS. Maintain the voltage tolerance defined in the *Pentium II Processor/Slot 1 Data Sheet.*
13. If a VRM 8.1 Header is used then refer to the *VRM 8.1 DC-DC Converter Specification* to ensure that the connections are made properly.
14. If an on-board voltage regulator is used, $V_{CC_{CORE}}$ must have adequate bulk decoupling based on the reaction time of the regulator used to create $V_{CC_{CORE}}$. It must provide for a current ramp of up to 30A/µS while maintaining the *VRM 8.1 DC-DC Converter Specification.*
15. The V_{ID} lines should have pull-up resistors on them ONLY if they are required by the Voltage Regulator Module or on-board regulator. The V_{ID} signals may be used to detect the presence of a processor, a pull-up is not required unless the V_{ID} signals are used by other logic. The V_{ID} lines are the only signals on the Slot 1 connector that are 5V tolerant.
16. Pin B12 is reserved and should be a no connect.

17. V_{CC} (±5%) must be provided to the Slot 1, pin B109. This power connection is not used by the Pentium II processor. It is required for the Slot 1 EMT tool and may be required by future Intel Boxed processors.
18. The JTAG port must be properly terminated, even if it is not used. See the Debug Recommendation in chapter 7 of this document.
19. Pull down TRST# with a 680 ohm resistor.
20. The EMI pins of the Slot 1 connector (pins B1, B41, B61, B81 and B100) should be connected to system or chassis ground through zero ohm resistors. The decision to populate these resistors is design dependent and can be determined through empirical EMI testing. The current Pentium II processor connects the EMI pins to ground on the processor card, future processors may utilize these pins for EMI suppression.
21. Slot 1 connectivity:
    All Slot 1 $V_{CC_{CORE}}$, V_{TT}, $V_{CC_{3.3}}$, V_{CC}, and GND pins, are connected to $V_{CC_{CORE}}$, 1.5V, 3.3V, 5V, and GND respectively.

GND		
A2	A42	A82
A6	A46	A86
A10	A50	A90
A14	A54	A94
A18	A58	A98
A22	A62	A102
A26	A66	A106
A30	A70	A110
A34	A74	A114
A38	A78	A118

$V_{CC_{CORE}}$	
B13	B65
B17	B69
B25	B73
B29	B77
B33	B85
B37	B89
B45	B93
B49	B97
B53	B105
B57	

V_{TT}
A1
A3
B5
B9

$Vcc_{3.3}$
B113
B117
B121

Vcc_{5}
B109

TESTHI Pin A13 must be pulled-up to $VCC_{2.5}$ with a 1K to 10 kohm resistor.

TESTHI
A13

All Reserved Pins must be no-connects.

Reserved		
A16	A113	B20
A47	A116	B112
A88	B12	

Design Considerations:

- If two V_{TT} regulators are used, one at each end of the bus, Intel recommends connecting the two regulator outputs together with a wide trace that runs along the same basic path as the GTL+ signals. Be aware of potential cross talk signals. V_{REF} should be generated at each AGPset component from this combined V_{TT}. This is simply a recommendation to minimize the effects of noise. See *AP-523 Pentium Pro Processor Power Distribution Guidelines* for more information.
- A single V_{TT} regulator may be used. For a UP system, maximum V_{TT} current is 4.6A. This considers that some signals are not used by the 440LX AGPset and only a “single” termination resistor is used (the one on the processor card).
- A power header for the Boxed Pentium II processor fan/heatsink power cable should be matched. Please consult the *Pentium II Processor/Slot 1 Data Sheet* for specifications of the fan power cable connector. The power header must be positioned within close proximity to the Slot 1 connector.
- The Slot 1 connector signal SLOTOCC# (Pin B101) is grounded on the Pentium II processor. Using a pull-up on the motherboard, this signal is used to inform motherboard logic that a card is present with GTL+ termination. The presence of a CPU core can be determined from the V_{ID} signals, all ones designates “No Core”. SLOTOCC# is 5V tolerant.

6.1.4 Uni-Processor (UP) Slot 1 Checklist

1. A uni-processor system must connect BREQ[0] of the Slot 1 connector to the PAC’s BREQ0# signal. This will assign an agent ID of 0 to the processor. Leave BR[1] unconnected. .
2. For a uni-processor design one set of GTL+ termination resistors (56 ohm) are recommended on the motherboard. For single end termination designs refer to appendix F.

3. GTL+ termination decoupling is required. Please see *AP-523 Pentium Pro Processor Power Distribution Guidelines* for VTT decoupling recommendations.
4. FRCERR# may be left as a no connect for a UP design: FRCERR#. A board's termination resistor for FRCERR# is not required since it is provided on the Pentium II processor.
5. Uni-Processor (UP) systems must connect PICCLK and provide PICD[1:0]# pull-ups.

6.1.5 Dual-Processor (DP) Slot 1 Checklist

1. A dual-processor system must cross connect BREQ[1:0] of the Slot 1 connector to the PAC's BREQ0# signal, i.e. the signal BREQ0# should be tied to BREQ1# on the other processor. This will assign an agent ID of 1 and 0 respectively to the processors. The Boot Strap Processor (BSP) will be the processor with the highest agent ID, so the "second" processor will be the BSP. See appendix H, dual processor schematics, for more details.
2. Ensure all specifications are met for both Slot 1 connector sites.
3. No on-board termination is required. Termination resistors are provided on each of the Pentium II processors.
4. Dual Processor (DP) systems must incorporate an I/O APIC (82093AA for PIIX4 based designs), connect PICCLK and provide PICD[1:0]# pull-ups.

Design Considerations:

- Each processor site has an isolated VCC_{CORE} power plane. Contact your VRM vendor for the availability of VRMs with current sharing capabilities. Please see the *VRM 8.1 DC-DC Converter Specification* for details.
- The SLOTOCC# signal can be used to block the system from booting if two processors with GTL+ termination resistors are not present. The Slot 1 VID lines can be used to determine if a non-functional processor core or termination card is present. Please see the *Pentium II Processor/Slot 1 Data Sheet* for further information on this signal.

6.1.6 Slot 1 Decoupling Capacitance

1. No additional VCC_{CORE} de-coupling high frequency or bulk capacitance is required for a properly designed Slot 1 power delivery plane and VRM. Please see the *Pentium II Processor/Slot 1 Data Sheet* for details on the power plane length and resistance requirements. For designs utilizing a local regulator on the motherboard, bulk decoupling is required. This amount of bulk decoupling depends on the regulator reaction time. Please contact your regulator vendor for decoupling recommendations that will meet the *VRM 8.1DC-DC Converter Specification*.

Design Considerations:

- Add as many extra high frequency and bulk decoupling capacitance sites as will fit near the processor slot to ensure proper decoupling of the Slot 1 connector.
- Decoupling capacitor traces should be as short and wide as possible.

6.2 440LX AGPset Checklist

6.2.1 440LX AGPset Errata

1. Refer to the Intel 82443LX PAC and 82371AB PIIX4 specification updates for work arounds on errata.

6.2.2 440LX AGPset Voltage

1. The PAC is a $VCC_{3.3}$ component. Connect all VCC3 pins to $VCC_{3.3}$.
2. Pull up PAC REF5V to 5V through a 1 kohm resistor.
3. The PAC A.G.P._REFV pin must be 0.4 of $VCC_{3.3}$, this can be achieved using a voltage divider.
4. Decouple PAC GTL_REFV pin.

6.2.3 440LX AGPset GTL+ Bus Interface

1. For a dual end termination UP design, on-board termination resistors are required for the following signals: HD[63:0]#, A[31:3]#, HREQ[4:0]#, RS[2:0]#, HTRDY#, BREQ[0]#, BNR#, BPRI#, DBSY#, DEFER#, DRDY#, ADS#, HIT#, HITM#, HLOCK#, CPURST#. The second set of termination resistors are provided on the Pentium II processor. For single end termination designs see appendix F.
2. For a DP design on-board termination resistors are NOT required for the following signals: HD[63:0]#, A[31:3]#, HREQ[4:0]#, RS[2:0]#, HTRDY#, BREQ[0]#, BNR#, BPRI#, DBSY#, DEFER#, DRDY#, ADS#, HIT#, HITM#, HLOCK#, CPURST#. The second set of termination resistors are provided on the second Pentium II processor or termination card. An empty Slot 1 connector is not allowed.
3. The following GTL+ signals on the Slot 1 connector may be left as no connects for both UP and DP designs: HA[35:32], DEP[7:0], RSP#, RS#, AERR#, BERR#, AP[1:0]#, BPM[1:0]#, BP[3:2]#, BINIT#. On-board termination resistors are not required since they are provided on the Pentium II processor(s).

6.2.4 440LX AGPset DRAM Interface

1. Externally buffer the CKE signal from the PAC to the DRAM array. A CMOS buffer (74LVC245) should be used.
2. Route, in a mixed DRAM array, to support both EDO and SDRAM, MAA12 (*and MAB12 when using configuration #2*) from the PAC to pin 39 and pin 126 of the DIMM sockets to support 64-Mbit SDRAM (BA1 signal) and EDO (A12 signal).
3. Route MAA11 (*and MAB11 when using configuration #2*) from the PAC to pin 122 of the DIMM sockets. Pin 122 is BA0 for SDRAM and A11 for EDO.
4. Route MAA13 (*and MAB13 when using configuration #2*) from the PAC to pin 123 of DIMM sockets. Pin 123 is A11 for SDRAM and A13 for EDO.
5. When using memory configuration #1, route a buffered copy of MAA[13:2] to each DIMM socket. Copies of MA[1:0] are provided in the configuration. Route MAA[1:0] to 2 DIMM sockets and MAB[1:0] to the other 2 DIMM sockets.
6. When using memory configuration #2, route MAA[13:0], along with RCSA[1:0]#, CDQA[7:0]#, SRAS0#, SCAS0#, and WE0#, to the furthest DIMM socket from the PAC. Also route MAA[13:0] to the middle DIMM socket with RCSA[2:3]#, CDQA[7:0]#, SRAS1#, SCAS1#, and WE1#. Route MAB[13:0] to the closest DIMM socket to the PAC with RCSA[4:5]#, CDQA[7,6,4:2,0]#, CDQB[5,1]#, SRAS2#, SCAS2#, and WE2#.
7. No series termination resistors are required on any memory interface signals in a 440LX memory design.

Design Considerations:

- Error Checking and Correction (ECC) or Error Checking (EC)—The 440LX supports either ECC, or EC when using x72-bit memory devices. The PAC can disable ECC or EC in the memory array.

6.2.5 440LX AGPset PCI Interface

1. 2.7 kohm (approximate) pull-up resistors to V_{CC} are required on PIRQ[A:D]#, FRAME#, TRDY#, STOP#, IRDY#, DEVSEL#, PLOCK#, PERR#, SERR#, CLOCKRUN, REQ64# and ACK64.
2. 5 kohm (approximate) pull-up resistors to V_{CC} independently bused are required on SDONE, SBO#, TMS and TDI on the PCI connectors.
3. 5 kohm (approximate) pull-down resistors independently bused (See the *PCI Local Bus Specification Rev 2.1* section 4.3.3 Pull-ups) are required on TRST# and TCK on the PCI connectors.
4. 2.7 kohm (approximate) pull-up resistors to V_{CC} are required on REQ[0:4]. These are 5V tolerant inputs to the PAC.
5. 8.2 kohm (approximate) pull-up resistors to $V_{CC3.3}$ are required on GNT[0:4]#, PHLDA# and PHOLD#. GNT[0:4]# and PHLDA# are outputs from the PAC.

Design Considerations:

- The 440LX AGPset supports up to 5 PCI masters with its REQ[4:0]# / GNT[4:0]# pairs. The PCI bus supports up to 10 PCI loads. The PAC and the PIIX4 each represent 1 load, other PCI components soldered on the motherboard add 1 load each, and each PCI connector adds approximately 2 loads. A design using four PCI slots will use all available PCI loads. If all 5 REQ[4:0]# / GNT[4:0]# pairs are used, simulation is required to ensure that the *PCI Local Bus Specification Rev. 2.1* timings are met.

6.2.6 440LX A.G.P. Interface

1. The A.G.P. interface is designed for a 3.3V operating environment, and both the master and target A.G.P. compliant devices must be driven by the same supply line.
2. The following A.G.P. signals must have pull-up resistors, approximately 8.2 kohm, to $V_{CC3.3}$: GFRAME#, GTRDY#, GIRDY#, GDEVSEL#, GSTOP#, GSERR#, GPERR#, GREQ#, GGNT#, SB_STB#, ADSTB-A, AD_STB-B, PIPE#.
3. When interfacing with a connector or device that uses the A.G.P. PIPE# or SBA# signals then pull GPAR# up to 3.3V using an 8.2 kohm resistor. If the device uses GFRAME# then no pull up is required.
4. Pull-up RBF# to $V_{CC}3$ with an 8.2 kohm resistor if using an A.G.P. connector, or if the A.G.P. compliant master on the motherboard can tri-state RBF#.
5. The A.G.P. specification does not require external termination resistors, for signal integrity. Termination resistors can be added to improve signal integrity provided that performance (timing) constraints are still satisfied.
6. A.G.P. interrupts may be shared with PCI interrupts similar to the recommendations in the *PCI 2.1 specification*. For example, in a system with 3 PCI slots and one A.G.P. slot, interrupts should be connected such that each of the four INTA# lines connects to a unique input on the PIIX4. It is recommended that the interrupts be staggered. It is also recommended that each PIRQ be programmed to a different IRQ, if possible.
7. In this reference design, the A.G.P. interrupts are pulled up to 3.3V, and a buffer is used to isolate the 5V environment from the A.G.P. bus.
8. In order to minimize the impact of any mismatch between the motherboard and the add-in card, an impedance of 65 ±15 ohm is strongly recommended.
9. At each component that requires it, A.G.P._V_{REF} should be generated locally from the A.G.P. interface V_{ddq} rail.
10. Decouple V_{REF} to ground to manage switching current.

6.2.7 440LX Miscellaneous Signals

1. Route ECCERR# through an open collector buffer to the EXTSMI# pin of PIIX4, with an 8.2 kohm (approximate) pull-up to 3V_STBY.
2. WSC# can be left as no connect for a “UP” design. In a “DP” design, it must be connected to the APICACK2# signal of the IOAPIC with an 8.2K (approximate) pull-up to VCC3.
3. CRESET# is used to control the reset values of the A20M#, IGNNE#, LINT[1:0] and determine the ratio of core and bus frequency. This signal is delayed to provide the two BCLK hold requirement. No additional delay logic is required.
4. Pull up TESTIN# to VCC3 with an 8.2K (approximate) pull-up resistor.

6.2.8 82371AB (PIIX4) PCI ISA/IDE Xcelerator

1. Place 1 kohm to 4.7 kohm pull-ups to $V_{CC3.3}$ on the INTR, NMI, and IGNNE# signals. These are open drain outputs on the PIIX4 and connect to the core frequency ratio strapping logic.
2. Place 330 ohm to 1 kohm pull-ups to $V_{CC2.5}$ on the SMI#, STPCLK# signals if they are directly connected to the Slot 1 connector. These are open drain outputs on the PIIX4.

6.2.9 82371AB (PIIX) ISA Signals

1. Place a 4.7 kohm pull-up on IOCHCK# to $V_{CC3.3.}$
2. Place 8.2 kohm pull-ups on IRQx, SD[15:0], MEMR#, MEMW#, IOR# and IOW# to $V_{CC3.3}$.
3. Place a 5.6 kohm pull-down on DRQx.
4. Place a 1 kohm pull-up on RFRESH#, IOCHRDY, SMEMR#, MASTER# and SMEMW# to $V_{CC3.3}$.
5. Pull-ups or pull-downs on signals routed to the processor see the Slot 1 section of this chapter.
6. The PIIX4 will support a maximum of 5 ISA slots.

6.2.10 82371AB (PIIX4) X-Bus Signals

1. XOE# and XDIR# are connected to the Ultra I/O device. The schematics that are in this document use FDC37C932FR Ultra I/O device. XOE# is connected to ROMCS# and the XDIR# is connected to ROMOE#. Any system using this Super I/O device should use the same layout.

6.2.11 Flash Signals and Layout

1. If adding a switch on VPP for write protection, switch to GND instead of VCC.
2. Connect the DU pin of the 2-Mbit devices to GND if anticipating to use the Intel SmartVoltage boot block flash memory family in the future.
3. Use A16 inversion for 1-Mbit devices and A17 inversion for 2-Mbit devices to differentiate between recovery and normal modes.
4. Use a 0.01 µf–0.1 µf ceramic capacitor connected between each VCC and GND, and between its VPP and GND. These high frequency, inherently low inductance capacitors should be placed as close as possible to the package leads.

6.2.12 82371AB (PIIX4) USB Signals

1. USB signals P0+, P0-, P1+, P1- require a 15 kohm ± 5% pull-down resistor on PIIX4 outputs. The PIIX4 provides two USB ports. Any unused USB port must still be terminated with 15 kohm pull-down resistors on both the P+/P- data lines.
2. The USB Clock, 48 MHz, with a duty cycle of better than 40/60% goes into pin J3 (CLK48) of the PIIX4. The PIIX4 does not support a 24-MHz clock rate.
3. 27 ohm series termination resistors are required on the USB Px+/Px- lines and should be placed as close as possible to the PIIX4.
4. 47 pf capacitors to ground are required on the USB Px+/Px- lines. The capacitors must be placed on the PIIX4 side of the (27 ohm) series termination resistors and as close as possible to the PIIX4.
5. Intel recommends ferrite beads and bypass capacitors on V_{CC} and V_{SS}, the USB power and ground lines. These are recommended for EMI purposes.

Note:

For more information on USB signals and Layout Guidelines see Appendix A.

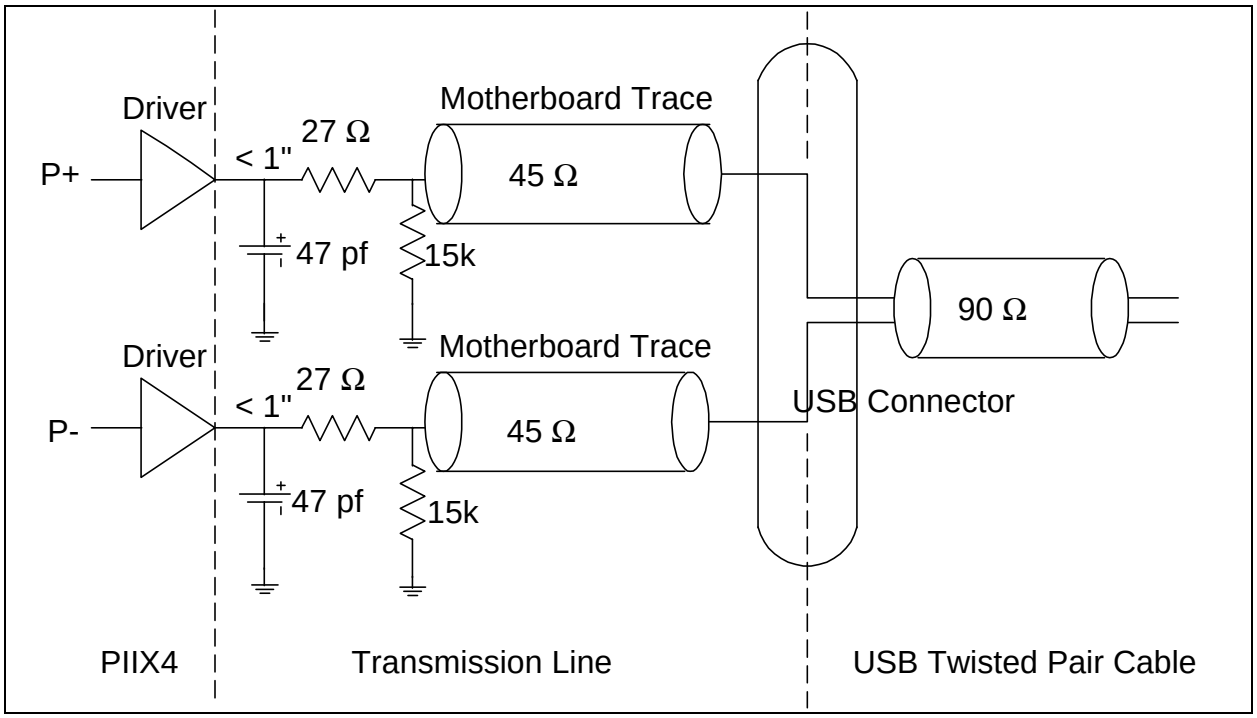


Figure 6-2. USB Data Signals

Design Considerations:

- Clock device - Clock synthesizer vendors now offer devices with 48-MHz outputs for use with USB controllers. These are preferred over older clock synthesizer devices which had 24 & 12-MHz outputs. Frequency tolerance must be less than or equal to ±2500 ppm. Cycle-to-Cycle Clock Jitter must be less than or equal to ±500 pS.

6.2.13 82371AB (PIIX4) IDE Interface

1. PIORDY# and SIORDY# must have 1 kohm (approximate) pull-up resistors to VCC.
2. PDDREQ and SDDREQ require a 5.6 kohm (approximate) pull-down resistor to VCC.
3. IDEACTP# and IDEACTS# each need a 10 kohm (approximate) pull-up resistor to VCC.
4. All signals running to the IDE connectors (except for PIORDY#/SIORDY#) require 33 ohm (approximate) series terminating resistors.
5. Pin 28 of the IDE connectors (CSEL) requires a 470 ohm pull-down resistor. The state of the cable select pin determines the master/slave configuration of the hard drive.
6. There is no internal pull up or down on PDD7 or SDD7 of the PIIX4. The ATA-3 specification suggest a 10 kohm pull-down on DD7 in section 4.3.1. Devices shall not have a pull-up resistor on DD7. It is recommended that a host have a 10 kohm pull-down resistor on PDD7 and SDD7 to allow the host to recognize the absence of a device at power-up. It is intended that this recommendation become mandatory in the next revision of the ATA standard.

6.2.14 82371AB (PIIX4) Power Management Interface

1. EXTSMI# is connected to ECC_ERR of the PAC, and pulled up to 3V_STBY with a 8.2 kohm (approximate) resistor.
2. The following signals are not supported in the Pentium II/440LX/PIIX4 platform and can be left as no connect:
   SUSA#, SUSB#, CPU_STP#, PCI_STP#, ZZ, SUS_STAT[1:2]#, SUSCLK
3. To control the supply of trickle current, SUSC# should be connected to pin#14 of the ATX power supply via an inverter.
4. PWRBT# is connected to the soft-switch button on the front panel via external de-bounce circuitry.
5. RSMRST# is powered from 5 VSB (5 volt stand-by) of the ATX power supply through an RC delay and Schmitt trigger. The RC delay circuit provides the necessary 1 ms delay for RSMRST#.
6. Connect SMBCLK, SMBDATA to 8.2 kohm (approximate) pull-up resistors to 3V_STBY, and route to all DIMM sockets and the A.G.P. connector.
7. SMBALERT# is connected to 3V_STBY with an 8.2 kohm (approximate) resistor.
8. RI# is connected to a modem (if one is used). RI# should be pulled-up to 3V_STBY with an 8.2 kohm (approximate) pull-up resistor if it's not used. See note after this section.
9. BATLOW# is used for the battery monitoring logic and needs an 8.2K pull-up (approximate) resistor to 3V_STBY if it is not used.
10. LID is used for the lid monitoring logic and needs an 8.2k pull-up (approximate) resistor to 3V_STBY if it is not used.
11. When not used in a thermal protection mode, THRM# must be pulled-up to the core power plane with an 8.2 kohm resistor.

Note:

SCI on RI# will not cause a problem for PIIX4 systems until July 1, 1998. Mobile systems will be converted to PIIX4E by this time (for throttling). LX and TX desktop systems that are submitted to WHQL after July 1, 1998 will not pass ACPI unless they connect the RI# event to a pin other than RI# so that an SCI is generated.

Design Consideration:

The following should be considered when implementing a RESET BUTTON for desktop based systems.

The system reset button has typically been connected indirectly to the PWROK input of the PIIX4. This technique will not reset the suspend well logic, which includes the SM Bus Host and Slave controllers. To reset the hardware in the suspend well, the reset button should be connected to the RSMRST# input

of the PIIX4. Assertion of RSMRST#, via a reset button, will result in a complete system reset. RSMRST# assertion will cause SUS[A-C]# to assert which results in the deassertion of PWROK if SUS[A-C]# controls the power supply PS-ON control signal. The deassertion of PWROK will cause the PIIX4 to assert PCIRST#, RSTDRV, and CPURST.

6.2.15 82093AA (IOAPIC)

1. An I/O APIC is required for a “DP” system and optional for a “UP” system.
2. The I/O APIC is a 5V device. All V_{CC} pins must be connected to 5V. Pins 19, 51 and 64 are 5V power, and pins 1, 33, and 52 are ground pins.
3. APICCLK—May be 2.5V, 3.3V or 5V levels. If it is shared with the Slot 1 PICCLK then it must be 2.5V. The maximum frequency is 33 MHz, minimum is 25 MHz.
4. APICACK2# (pin 8)—This pin is connected to the PAC WSC# signal.

Design Considerations:

- CLK—Is compatible with 3.3V or 5V input levels. It is typically connected to the PCI clocks that are 5V. The maximum frequency is 33 MHz, minimum is 25 MHz.
- SMI Support—The option to route through the IOAPIC is recommended depending on the OS intended for use on the platform.
- RTC Alarm Interrupt—When an IOAPIC is enabled, the IRQ8# output signal on the PIIX4 reflects the state of IRQ8. IRQ8# resides in the PIIX4 suspend well and connects to INTIN8 on the IOAPIC. If the system is put in a STD or SOFF state, the PIIX4 will continue to drive IRQ8 to the IOAPIC which could damage the IOAPIC if it is not powered. For this reason a 74LVC125 buffer is included in the schematics to isolate the IOAPIC’s INTIN8 signal from the PIIX4’s IRQ8# signal when the system is suspended.
- System Timer Interrupt—When an IOAPIC is enabled, the PIIX4 IRQ0 output signal reflects the state of the system timer interrupt. This signal should be connected to INTIN2 on the IOAPIC (note that the schematics only show a pull-up on this signal).
- SCI and SMB Interrupts—The IRQ9OUT# output signal on the PIIX4 reflects the state of the internally generated IRQ9 interrupt. The SCI and SMB interrupts are hardwired to IRQ9 in the PIIX4. For ACPI compliance, this signal must be connected to the IOAPIC (note that the schematics leave this signal as a no connect). There are two different routing options:

  INTIN9: IRQ9OUT# can be connected to INTIN9 on the IOAPIC. The ACPI BIOS will report to the OS that the SCI uses IRQ9 for both PIC and APIC enabled platforms. However, for this solution ISA IRQ9 must be left unconnected. This could create an ISA legacy incompatibility with ISA cards that must only use IRQ9. Note that this conflict exists in all PIC enabled systems. The PIIX4 automatically masks ISA IRQ9 when SCI_EN is set.

  INTIN20 - INTIN22 (or any other available interrupts): IRQ9OUT# can be connected to any available IOAPIC interrupt. This solution eliminates the IRQ9 ISA legacy conflict described in the INTIN9 routing option. However, this routing option creates a new issue. The ACPI BIOS needs to report to the OS which interrupt is used to generate an SCI. In a PIC enabled OS (like Memphis) the platform would use the PIIX4 internal IRQ9. In an APIC enabled OS (like NT) the platform would use INTIN20, for example. The ACPI BIOS has the job of telling the OS which one to use, but the BIOS does not know which OS will load. If the platform only supports an APIC enabled OS (NT-only) there is no issue since the BIOS will just report IRQ20. If the platform needs to support both PIC and APIC operating systems (NT & Memphis), the BIOS will require a setup screen option that selects between APIC OS (IRQ20) and PIC OS (IRQ9) so the BIOS can properly report to the OS which interrupt is assigned to the SCI.

6.2.16 Boot Block Flash Design Considerations:

- Intel recommends the use of a 2-Mbit Boot Block device for BIOS non-volatile storage. Many designers are finding it difficult to keep the amount of BIOS code small enough to fit into a 1-Mbit Flash. Legacy support for USB keyboards requires additional code size support.

6.2.17 Power On RESET

1. Do not connect PWRGOOD to logic directly on board. Route it through a Schmitt trigger device to square-off and maintain its signal integrity to the system.
2. Incorporate VRM PWRGOOD output into power on reset logic.

6.3 Software/BIOS

Please see the *Pentium Pro Processor BIOS Writer's Guide* for details regarding the following responsibilities of the BIOS.

1. The Pentium II processor L2 cache must be initialized and enabled by the BIOS.
2. The STPCLK# feature must be enabled in the EBL_Power_On MSR for systems utilizing the STPCLK# pin to place the processor into low power mode.
3. The BIOS must load the BIOS Update to the Pentium II processor as early as possible in the POST. Use the BIOS update signature mechanism to verify that the processor has accepted the BIOS update.
4. It is recommended that the BIOS implement the minimum update API interface to allow the BIOS Update stored in BIOS to be updated. Of the two Intel-defined update APIs, it is recommended that the full INT15h interface be implemented. An API calling utility and test tool is available for this interface. Please contact your local Intel Field Sales representative for a copy.
5. Before starting a Flash update routine, use the MTRRs to disable caching, or only allow WT mode. This prevents a WBINVD instruction from writing stale data to the Flash memory.
6. Leave MTRR 6 & 7 un-programmed; they are reserved for operating system use.

6.3.1 Design Considerations:

- For UP systems to support both the current Pentium II processor and future processors it is highly recommended that storage space for two (or more) BIOS Updates be provided. This will allow manufacturing flexibility to install either Pentium II processor or future Intel Pentium II processors, the BIOS detects the processor and loads the correct BIOS Update.
- For DP systems it is recommended that storage for two (or more) BIOS Updates be reserved for the case where two different Pentium II processors are installed. This allows the support of two different Pentium II processors.

6.4 Thermals/Cooling Solutions

1. Provide adequate heatsink and air ventilation to ensure that the Pentium II processor T_{PLATE} specification documented in the *Pentium II Processor/Slot 1 Data Sheet* is met. Refer to the *Pentium II Processor/Slot 1 Data Sheet* and *AP-525 Pentium Pro Processor Thermal Design Guidelines* for thermal design information.
2. Provide adequate air ventilation, for the Pentium II Boxed processor to ensure that the air intake temperature to the fan/heatsink is less than the maximum allowable fan preheat temperature (T_{PH}) at the system maximum ambient temperature, measured 0.3" above the center of the fan. See the *Pentium II Processor/Slot 1 Data Sheet* for the T_{PH} Specification.
3. Verify that all major components have proper airflow.

6.4.1 Design Considerations:

- Make sure the air flow to and from the processor is not obstructed (e.g., by I/O cards, VRM etc.).
- There should be nothing between the processor and the air intake that may preheat the air flowing into the fan/heatsink.
- Eliminate air recirculation paths when using a system fan.
- Monitor the air flow through the Power Supply Unit (PSU)/system fan.
- Check the maximum ambient operation temperature of the system.

6.5 Mechanicals

1. The physical space requirements of the Pentium II processor and heatsink must be met. Refer to the *Pentium II Processor/Slot 1 Data Sheet* for details.
2. For the Boxed Pentium II processor: The physical space requirements of the Boxed Pentium II processor fan/heatsink must be met. Please see the *Pentium II Processor/Slot 1 Data Sheet* for details.

6.5.1 Design Considerations

- The Pentium II processor retention mechanism, retention mechanism attach mount and heatsink support is an optional support structure for retaining the Pentium II processor cartridge in the system during shock and vibration situations. Meet the motherboard keep out zones and mounting hole requirements. Please see the *Pentium II Processor/Slot 1 Data Sheet* for details.
- The Boxed Pentium II processor requires the implementation of the heatsink support holes for the heatsink support structure as defined in *the Pentium II Processor/Slot 1 Data Sheet* in order to properly support the Boxed Pentium II processor fan/heatsink.

6.6 Layout checklist

6.6.1 Routing and Board Fabrication

1. The exact value of the series resistor is dependent on the board layout and should be determined through simulation or lab measurement.
2. The skew between any two HCLK loads must be less than 500 ps max and -250 ps min (follow the CLK skew and layout recommendations in this document, or simulate). The skew between PCLKs must be less than 2.0 ns. The difference between rising edges of HCLK and PCLK must be between 0.5 and 6.0 ns.
3. Refer to chapter 5 of this document for board stack-up, layout and routing recommendations. The trace length recommendations for the host bus traces must be compensated to allow for the trace lengths on the Pentium II processor. The Pentium II processor trace lengths are provided in the Pentium II Processor Card IBIS Models. Please contact your local Field Sales representative for a copy of the model.
4. Make the characteristic impedance of the GTL+ bus between 50 ohm and 80 ohm.
5. Use an Intel qualified Slot 1 connector and vendor.
6. VRM header 8.1 Support: Make sure that the $V_{CC_{CORE}}$ trace/power plane is sufficient to ensure $V_{CC_{CORE}}$ meets specification. Please see the *Pentium II Processor/Slot 1 Data Sheet* for trace/power plane resistance and length requirements.
7. Route V_{TT} with at least a 50 mil (1.25 mm) wide trace.
8. Isolate V_{REF} traces to minimize the chance of crosstalk.
9. Route $V_{CC_{CORE}}$ from the voltage regulator to Slot 1 an “island” as opposed to a trace.
10. Make decoupling capacitor traces as short and wide as possible.

7

Debug Recommendations

CHAPTER 7
DEBUG RECOMMENDATIONS

7. Debug Recommendations

This section provides tool information, logic suggestions, technical support options and a summary of the problems which have been found to be associated with system debug. Although not comprehensive in scope, the recommendations are included to preclude unnecessary expenditures of time and effort during the early stages of debug. While the methodologies suggested are those which Intel believes are most likely to be successful, they are not a substitute for correct design practices nor are they a substitute for other Intel references.

7.1 Slot 1 Test Tools

The Slot 1 Test Kit, available Q3 ’96, consists of the following test tools:

The Slot 1 Electrical/Mechanical/Thermal (EMT) Test Tool, which provides mechanical, thermal and voltage transient testing capabilities.

The Slot 1 Continuity Test Tool (CTT), which provides continuity testing capabilities for the Slot 1 connector.

Please see the *Slot 1 Test Kit User’s Guide* for more information on these tools.

7.2 Debug/Simulation Tools

7.2.1 Logic Analyzer Interface (LAI)

Logic analyzer interface modules provide a way to connect your logic analyzer to signals on the Pentium II processor system bus. Two available LAI vendors:

1. Hewlett-Packard Co. for their HP-16500B* series logic analyzers. Please contact your local Intel Field Sales representative to learn the procedure to obtain this equipment. This product is purchased directly from Hewlett-Packard.
2. Tektronix for their DAS/NT* and DAS/XP* series logic analyzers. Please contact your local Field Sales representative for availability of the LAI562T interface module from Intel. The DAS* software is available directly from Tektronix.

Please contact your local Intel Field Sales representative to complete the proper non-disclosure agreement required to receive the LAI.

7.2.2 In-Target Probe (ITP)

The ITP562 provides software debug capability allowing the setting/clearing of hardware/software breakpoints, assembly/disassembly of code, display/modification of the processor register set, display/modification of system memory, display/modification of I/O space and includes a macro language for custom debug procedure creation, etc.

Contact your local Intel Field Sales representative for availability, the proper software license agreement and non-disclosure agreement required to receive the ITP.

7.2.3 Bus Functional Model (BFM)

A bus functional model for the Pentium II processor host bus is available from third party vendors and requires a special non-disclosure agreement. Please contact your local Intel Field Sales representative for information on the bus functional model vendors and to complete the appropriate non-disclosure agreements.

7.2.4 IBIS Models

IBIS Models are available from Intel for:

1. Pentium II processor
2. 440LX AGPset
3. PIIX4 PCI ISA IDE Xcelerator

Please contact your local Intel Field Sales representative for a copy of these models and to complete the appropriate non-disclosure agreements.

7.2.5 FLO*THERM** Model

A FLO*THERM* Model is available for the Pentium II processor. Please contact your local Intel Field Sales representative for a copy of this model and to complete the appropriate non-disclosure agreements.

7.3 Debug Features

The features mentioned in this section are for debug purposes only on initial prototype systems. They are not required for production level systems. Some of these features and desirable test functions you may incorporate onto production boards. These features are required to allow test equipment connections for debugging purposes.

7.3.1 LAI Issue

The LAI562 integration tool has been designed such that an extra load will be presented on the CMOS signals connected to the Slot 1 connector. The following list of signals are affected:

PREQ#, TCK, TDI, TDO, TMS, TRST#, INIT#, FLUSH#, STPCLK#, PICCLK, PICD[1:0]#, LINT[0]/INTR, LINT[1]/NMI, IERR#, SMI#, PWRGOOD, THERMTRIP#, SLP#, FERR#, IGNNE# and A20M#.

The following circuit describes the CMOS probe signals of the LAI562:

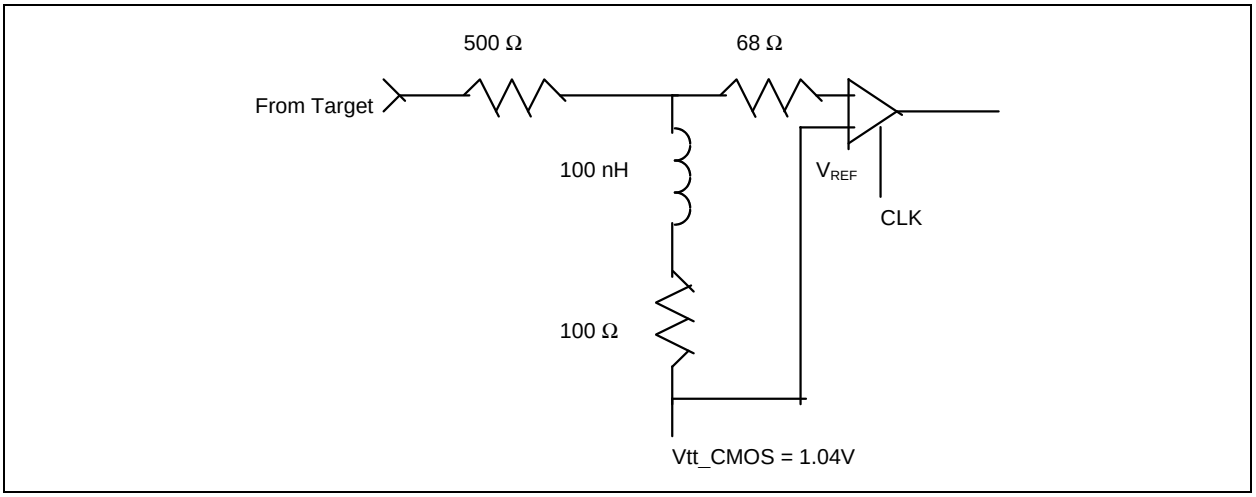


Figure 7-1. LAI Probe Input Circuit

The extra loading of the LAI562 requires stronger pull-up values on the target system. However, due to the current limitations of some signal drivers, this stronger value may not be feasible. Calculation of the correct pull-up resistor value for each of the CMOS signals should include a load analysis based on the pull-up voltage, pull-up voltage tolerance, pull-up resistor tolerance, V_{IH} and V_{IL} specifications, driver current rating, input current leakage, input timings, etc. The resulting values may conflict.

As a result of the extra loading the following compromise pull-ups to $V_{CC2.5}$ are recommended. The actual value required by your system may vary depending on the logic connected and the drive strength of the signal to the Slot 1 connector.

Inputs to the Slot 1 connector from the ITP562 Port:

PREQ#	150–330 ohm
TDI	150–330 ohm
TMS	150 ohm
TRST#	150–330 ohm (A 470 ohm (approximately) pull-down is recommended, but a pull-up may be used)

Inputs to the Slot 1 connector from the PIIX4:

STPCLK#	410 ohm
SMI#	410 ohm
SLP#	150–330 ohm

Outputs from the Slot 1 connector:

TDO	150 ohm
IERR#	150–220 ohm
THERMTRIP#	150–220 ohm
FERR#	150–220 ohm

Inputs to the Slot 1 connector, from system logic (assuming a 14 mA driver):

PWRGOOD	150–330 ohm
INIT#	150–330 ohm

LINT[0]/INTR 150–330 ohm

LINT[1]/NMI 150–330 ohm

IGNNE# 150–330 ohm

A20M# 150–330 ohm

Bi-directional signal to/from the Slot 1 connector:

PICD[0]# 150 ohm

PICD[1]# 150 ohm

Inputs to the Slot 1 connector, only pullup:

FLUSH# 330 ohm

7.3.2 Debug Logic Recommendations

Debug Recommendations are intended to assist in the development of the Pentium II processor systems and products utilizing it. The following are strongly recommended for early prototype designs only.

1. When debugging provide a push button reset circuit. Do not rely on power-on reset from the power supply. A push-button reset usually results in more repeatable results when debugging initialization problems because when it resets the system it does not clear all discrete devices within the chips. Therefore increasing the probability of the chips booting with the same initialization issue.
2. Include a Pentium II processor debug port connector. See the Integration tools chapter of the *Pentium II Processor/Slot 1 Data Sheet* for schematics and a signal checklist. Be sure it is the proper 0.050” x .100” (1.27 mm x 4 mm) spacing connector.
3. Provide the capability to measure the processor’s case temperature (Tplate) to ensure that the maximum temperature specification per the *Pentium II Processor/Slot 1 Data Sheet* is not violated.
4. Place an SMA style (or similar) coaxial connector on the power plane between the VRM Header or on-board voltage regulator and Slot 1 connector so that power plane noise can be monitored on systems. An SMA to BNC cable may be needed to connect to an oscilloscope also. This footprint should only be populated during design evaluation.
5. The ITP562 requires a complete boundary scan chain. For a DP system, it is recommended to place jumpers on the motherboard to allow the boundary scan chain to bypass a Slot 1 connector with a termination card.

Debug Considerations:

- As technology drives lower power modes, the $V_{CC_{CORE}}$ current demand becomes very small. This can sometimes cause a regulator to go out of regulation. Place pads for a load resistance on the $V_{CC_{CORE}}$ regulator in the event the regulator cannot function with extremely low current.
- After meeting the guidelines in the *Pentium II Processor/Slot 1 Data Sheet*, add as many extra high frequency and bulk decoupling capacitance sites as will fit near the processor slot.
- Intel recommends using industry standard Voltage Regulator Modules designed for the Pentium II processor. VRM modules designed for the Pentium Pro processor utilizing voltage ID should also work for the initial Pentium II processor samples to aid in early debug. However, these previous VRM modules may not support future processors for Slot 1. The Pentium Pro processor VRM module specification does not meet the maximum current requirements of a Pentium II processor. **Note:** There is a VRM Header pinout change required to support the VRM designed for use with Slot 1.
- For a back-up plan, have a buffered crystal oscillator method of processor clock distribution. This will be useful in case there are jitter specification issues due to the number of components containing internal PLLs on the processor card.

- Special Function Pins: VID[4:0]

  PIN TYPE: Open or ground-short

  PIN FUNCTION: Voltage ID pins (VID[4:0]). These pins are used to vary the voltage set point of the DC to DC converter that supplies power to the processor.

  PIN NUMBERS: A121, B119, A119, A120, B120

Provide jumpers as shown in Figure 7-2, or 0 ohm resistors. This allows changing the voltage ID for the part.

Note:

Some VRM modules may not be able to support the pull-up resistors shown in Figure 7-2. Contact your VRM vendors to understand their pull-up requirements.

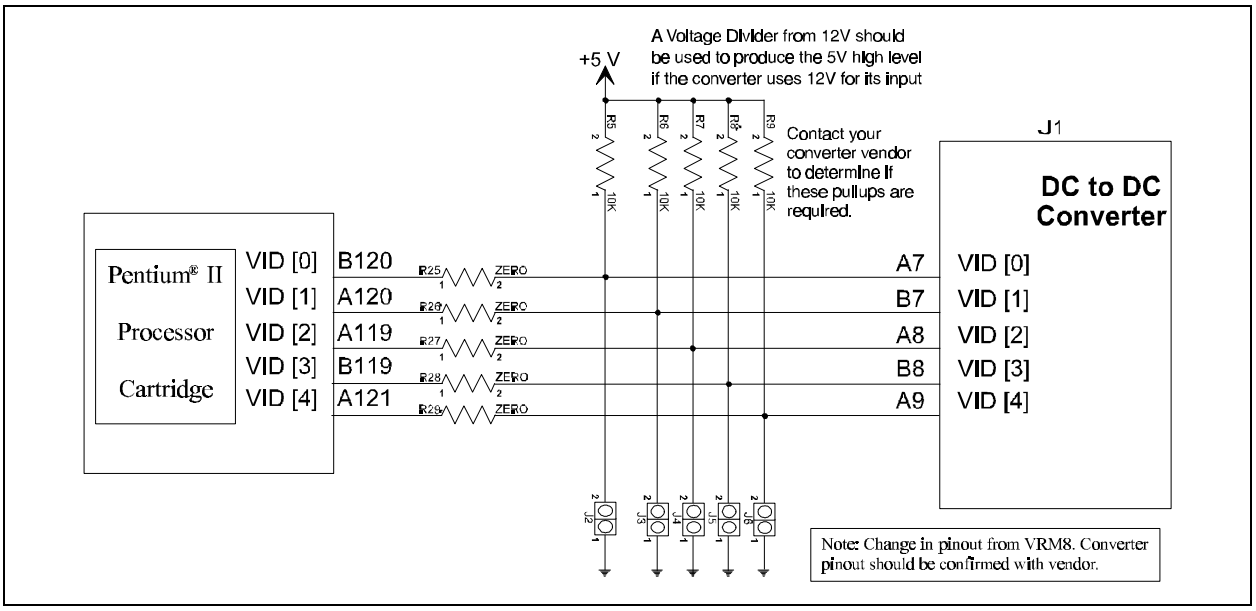


Figure 7-2. VID Circuit

7.3.3 Debug Layout

1. Pay close attention to the keep out zones for the Logic Analyzer Interface (LAI) described in the Integration Tools section of the *Pentium II Processor/Slot 1 Data Sheet.* These keep out zones are required to ensure that the LAI can be installed within a system.

Design Considerations:

- Plan as much space as possible for the Pentium II processor. This will allow for additional cooling or other requirements for early Pentium II processors.

7.3.4 Debug Procedures

- When using an ITP562 In-Target Probe for the Pentium II processor, a common error is that the boundary scan chain order in the ITP562.INI input file is not correct. Please check the file to ensure that the scan chain connections on your motherboard match the order provided. This file needs to change based on what components are in the boundary scan chain. In DP systems, the processor with PREQ0# and PRDY0# is considered processor 0 even if it isn't the first one in the chain.
- TCK noise may limit ITP speed or cause functional problems. The TCK speed can change from 10 MHz to 1250 Hz using the keyword, TCLK = "value," in the [Debug Port] section of the ITP562.INI file. Refer to the ITP HELP menu "Changing the TCLK Signal Frequency" for the valid values. If there are difficulties initializing the ITP562 slow TCK.

- ITP macros are available for the 440LX AGPset to assist in debugging your system. A number of macros are provided. Some of the macros are utilities to read/write any PCI configuration register, a macro display POST codes and stop on a specified code, macros to dump the PAC and PIIX4 register sets as well as processor specific registers. Contact local Intel Field Sales representative for a copy of these utilities.
- TDO out of each processor should have a 150 ohm pull-up. PICD0# and PICD1# should each have a 150 ohm pull-up (IERR# might be asserted during the APIC/MP message generation if an insufficient pull-up is used.).
- Watch out for incorrect clock voltages. BCLK, TCK, and PICCLK are all $V_{CC_{2.5}}$ signals.
- PICCLK must be driven even if APIC is not used. The APIC bus executes MP initialization even in a uni-processor system.
- APIC may be disabled in BIOS for initial debug by clearing bit 11 in the APIC base MSR (0x1Bh).
- Be sure boundary scan chains are properly reset using the TRST# pin of each device in the debug port chain.
- The Global Descriptor Table (GDT) must be aligned. The GDT must be located on a DWORD boundary, or else setting the PE bit and branching will cause a SHUTDOWN transaction.
- The ITP “pins” command may be used to check reset configuration pin states. Be aware, however, that observing pin state during reset will not reveal anything about the stability or timing of the configuration signals around the reset edge.
- You can expect the following Pentium II processor bus activity after reset: BNR# stops toggling approximately 2.8 million BCLKs after the deassertion of RESET#, if BIST is not configured to run. If BIST is configured to run, BNR# will continue to toggle until BIST completion. After BNR# stops toggling, the PICD[1:0]# signals begin the MP initialization to determine the bootstrap processor. In a single processor boot, two 21-cycle short messages are transmitted on the APIC. (Refer to the *Pentium Pro Family Developer’s Manual, Vol. III.*) The following fields are expected and all others are “don’t care.” **Please note that PICD[1:0]# are active low so the pin electrical levels will be the complement of the numbers presented here**.

  Interrupt Vector = 0x4N for the first cycle and 0x1N for the second cycle.

  Where “N” is the processor number

  DM = 0, D3-D0 = 1111 (all including self shorthand)

  Trigger Mode = 1 (edge)

  Level = 0 (deasserted)

  Delivery Mode = 000 (fixed)

A

USB in a 440LX System

APPENDIX A
USB IN A 440LX SYSTEM

A.1 PIIX4 Implementation

The PIIX4 contains a Universal Serial Bus (USB) Host Controller which moves data between the main system memory and devices on the USB. The host controller also includes the root hub with two USB ports. This permits the connection of two USB peripherals or hub devices directly to the PIIX4. The PIIX4 Host Controller completely supports the standard Universal Host Controller Interface 1.0 (UHCI) and takes advantage of the UHCI software drivers.

The PIIX4 fully supports the USB Specification, Revision 1.0. The PIIX4 supports both full speed and low speed signaling: 12 Mbps and 1.5 Mbps, and can differentiate between full speed and low speed devices connected to its USB ports.

The key electrical requirements of USB for a motherboard design are:

- The rise and fall times of 12 Mbps data signals are 4 to 20 ns.
    - 90% =< (rise time/fall time) X 100% =< 110%
    - The crossover voltage should be between 1.3 and 2.0 volts.
- The rise and fall times of 1.5 Mbps data signal are 75 to 300 ns
    - 80% =< (rise time/fall time) X 100% =< 120%
    - The crossover voltage should be between 1.3 and 2.0 volts.
- 45 ohm signal impedance for the full speed differential signal.
- Single-ended zero state on USB ports when no function is attached.
- 500 mA minimum of DC supply current for each USB port.
- The voltage supplied by host is 4.65V to 5.25V.

A.2 USB Motherboard Layout Guidelines

The goal of the following routing guidelines are to minimize the effects of ringing, crosstalk, and EMI radiation in the USB data signal lines. It is very important to ensure that high frequency system signals do not couple to the USB signals and radiate out on the USB cable. This is done by carefully matching the motherboard circuitry impedance to that of the twisted pair USB cable, by controlling signal rise and fall times, and by careful routing of the USB signals on the motherboard.

A.2.1 USB Data Signals Layout Guidelines

Following are general guidelines for the USB interface:

- The unused USB port should be terminated with 15K pull-down resistors on both P+/P- data lines.
- 27 ohm series resistors should be placed as close as possible to the PIIX4 (<1 inch). These series resistors are there for source termination of the reflected signal.
- 47 pF capacitors must be placed as close to the PIIX4 as possible and on the PIIX4 side of the series resistors on the USB data lines (P0±, P1±). These caps are there for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15 kohm ±5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (P0±, P1±), and are REQUIRED for signal termination by USB specification. The length of stub should be as short as possible.
- The trace impedance for the P0±, P1± signals should be 45 ohm (to the ground) for each USB signal P+ or P-. The impedance is 90 ohms between the differential signal pairs P+ and P- to match the 90 ohm USB twisted pair cable impedance. Note that twisted pair characteristic impedance of 90 ohm is the series impedance of both wires, resulting in an individual wire presenting a 45 ohm impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines must be routed as ‘critical signals’ (i.e., hand routing preferred). The P+/P- signal pair must be routed together and not parallel with other signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. Do not worry about crosstalk between the two P+/P- signal traces. The P+/P- signal traces must also be the same length. This will minimize the effect of common mode current on EMI. (Common mode current is caused by differential signals whose currents are not perfectly matched.)

Figure A-1 illustrates the recommended USB signals schematic:

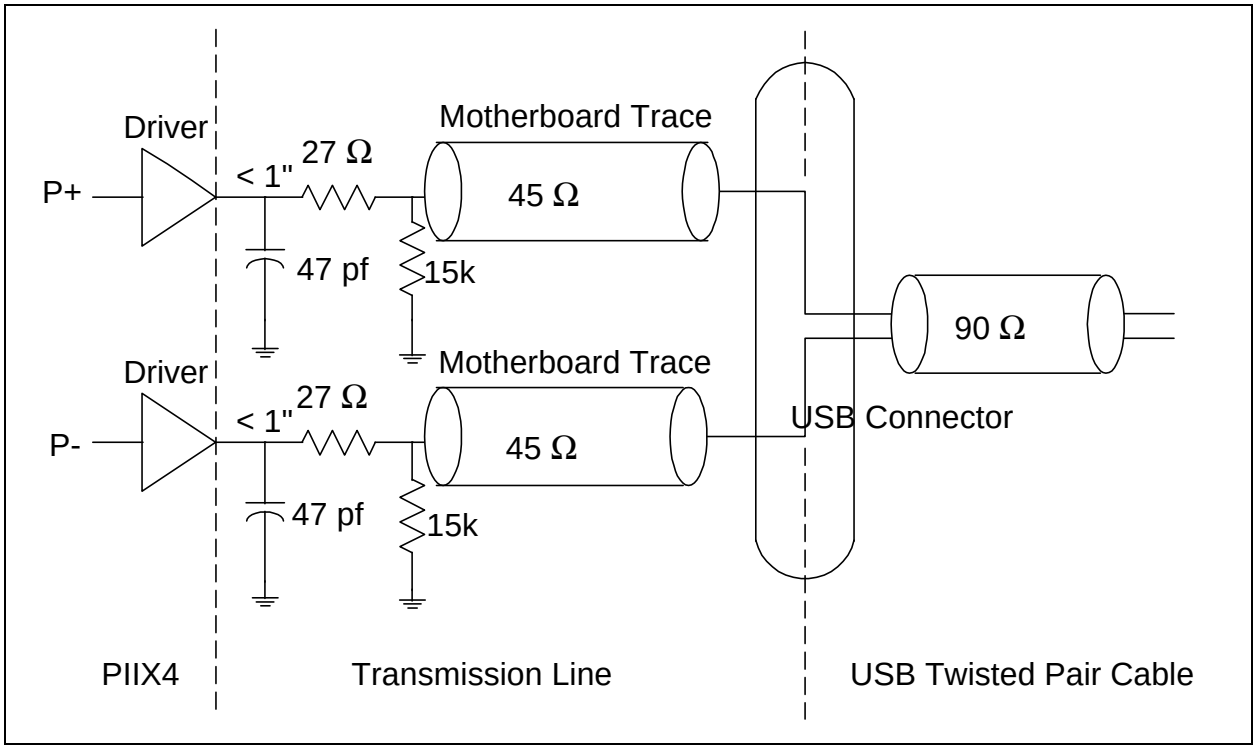


Figure A-1. USB Data Signals

Figure A-1b illustrates a possible configuration for having a 45 ohm transmission trace. The system designer is responsible for ensuring that a particular configuration meets their requirements.

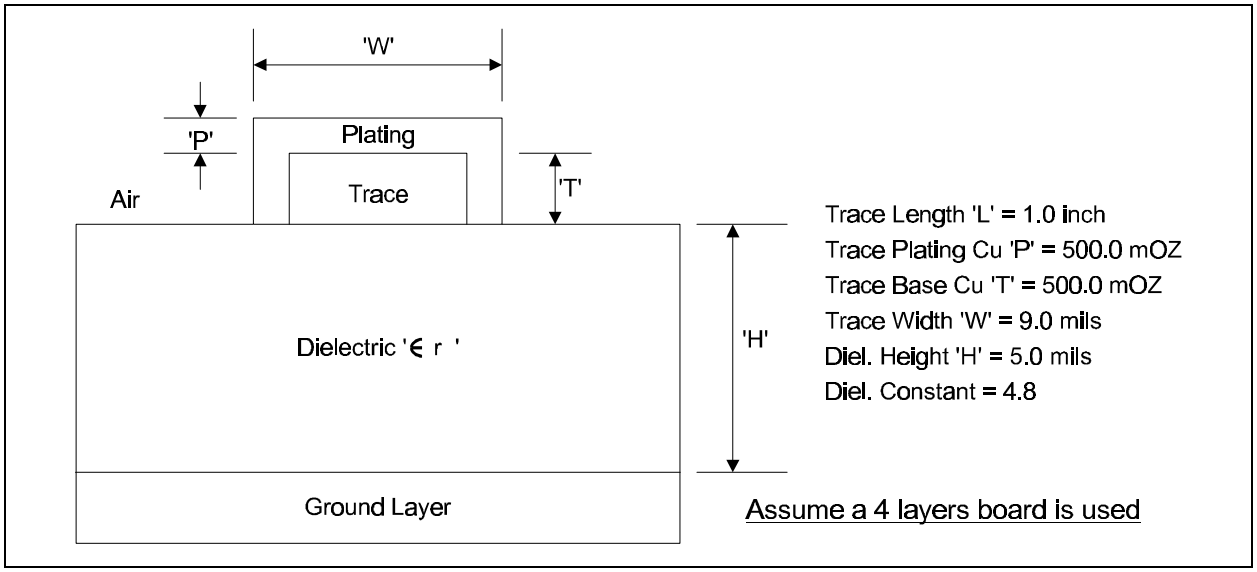


Figure A-1b. Possible 45 ohm Trace

The results from Figure A-1b are:

Impedance 'Z0' = 45.4Ω
Line Delay = 160.2 ps
Capacitance = 3.5 pF
Inductance = 7.3 nH
Res @ 20° C = 53.9 mΩ
Trace Height = 1.4 mil

A.2.2 USB Power and Distribution Layout Guidelines

Following are general guidelines for USB power line and ground line:

- The VCC power lines should be bypassed with a 68 µf or 150 µf tantalum capacitor depended on the layout topologies. It should be placed between fuse and ferrite bead on VCC. The tantalum capacitors should have a low dissipation factor to allow decoupling at higher frequencies. Please refer to section A.2.3 for the recommended topologies.
- Ferrite beads (and optional bypass capacitors) are recommended on each VCC and VSS, the USB power and ground lines, to minimize EMI radiation. They should be placed as close as possible to the USB connector. The recommended value of ferrite beads is 100 ohm at 100 MHz. It is important to connect bypass capacitors to chassis ground if they are used. The capacitor values should be between 0.01 µF and 0.10 µF.
- Voltage divider circuits should be used to drive the status of USB power line to OC[1:0]# inputs. OC[1:0]# signals are 3.3V inputs and have a leakage current of maximum ±1 µA. The recommended value (maximum) of resistors are 470K and 560 kohms. Use a 0.001 µf to 0.01 µf capacitor for noise filtering. These resistors should be placed on the motherboard if the riser card option is used for USB connectors.
- PolySwitch fuses, standard fuses, or some type of solid state switch should be used on each power line for overcurrent protection. USB spec requires that current be limited to 5 units load (1 unit = 100 mA) for each USB port. However, the circuit protector must be chosen so that it will not trip for power on or dynamic attach transient current. The reasonable value for the trip current is 1.5A to 2.0A, and it can not exceed 5A.

Table A-1. DC Electrical Characteristics on VCC

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage (Powered Host)	VCC	4.65	5.25	V	1
Supply Current (Powered Host)		500		mA	2,3

NOTE:

1. The minimum supply voltage is 4.65V on USB port after voltage drop on power line and connector. The voltage drop on power line consists of trace resistance, the resistance of the fuse, and DC resistance of ferrite beads yielding a total voltage drop of about 100 mv. The lowest transient voltage (AC) that may appear at the host is 4.20V.
2. The supply current cannot exceed 5.0A. The recommended trip current (minimum) is 1.5A–2.0A.
3. The recommended time not to trip is 100 µs minimum for solid state switch circuit for power on and dynamic attach transient current.

The Figure A-2 illustrates the recommended USB power line and ground circuit:

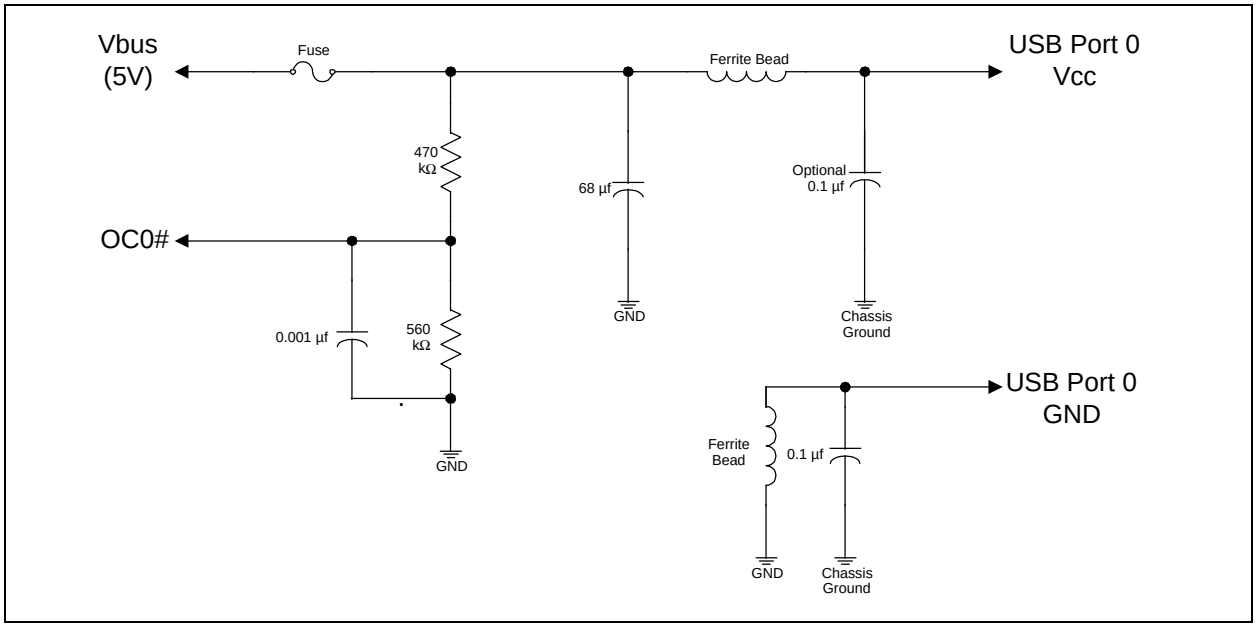


Figure A-2. USB Power Line VBUS and Ground Line

A.2.3 USB Power Line Layout Topologies

The following power line layout topologies are typical of those found in the platforms. The system designers need to carefully evaluate each recommended topology and choose the appropriate one to meet USB voltage drop and droop requirements.

A.2.3.1 Option #1 An Optimal Design—Implemented

Figure A-3 represents an optimal design for a downstream USB power connection. IR drop is minimized through use of separate fuses and ferrite beads. Each port has dedicated bulk capacitance. When a hot plug occurs on one port its effect on the second port is minimized because C1, C2 and CMB form a three-way capacitive divider. The per port ferrite beads also have a small resistance, and that resistance acts as an inrush current limiter. Note that the recommended value of C1 and C2 tantalum capacitors is 68 µf, and CMB represent the motherboard capacitance. It is also important that C1 and C2 are located within 1 inch of USB connectors.

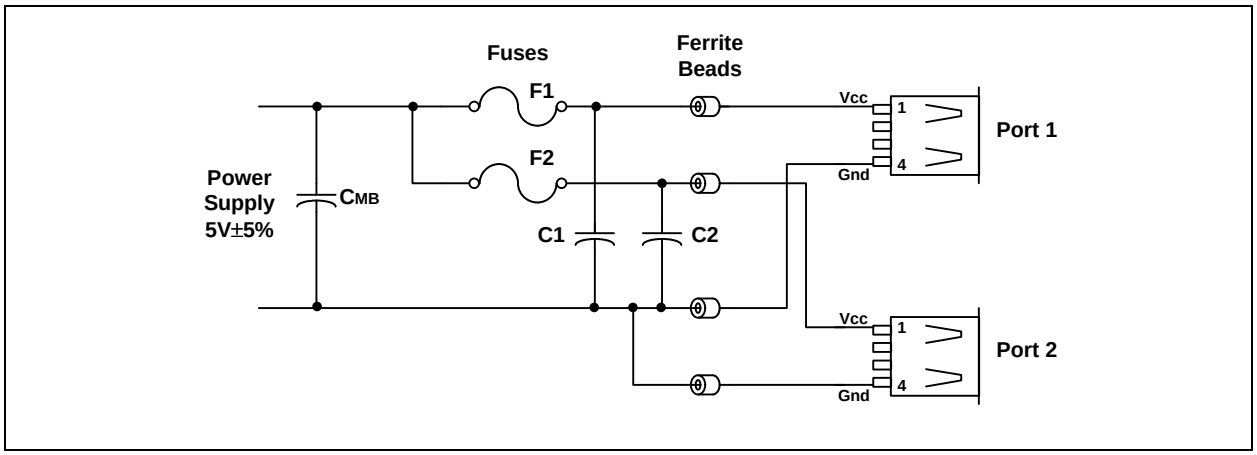


Figure A-3. Best Downstream Power Connection

A.2.3.2 Option #2 An Effective Design—Recommended

Figure A-4 is a less expensive but still effective implementation of a USB power output stage. The principal difference is that the per port capacitors and fuses are now shared. If F1 is increased to compensate for the need to carry twice the current then the DC voltage drop through this output circuit remains the same. Droop voltage response will not be quite as good as Figure A-3, because C1 must now both supply current to both the peripheral already plugged in as well as the peripheral just hot plugged. The resistance of the ferrite beads becomes more critical in this instance because their resistance limits the inrush current seen by C1. The recommended value of C1 tantalum capacitors is 150 µf, and CMB represent the motherboard capacitance. It is important that C1 is located within 1 inch of USB connectors.

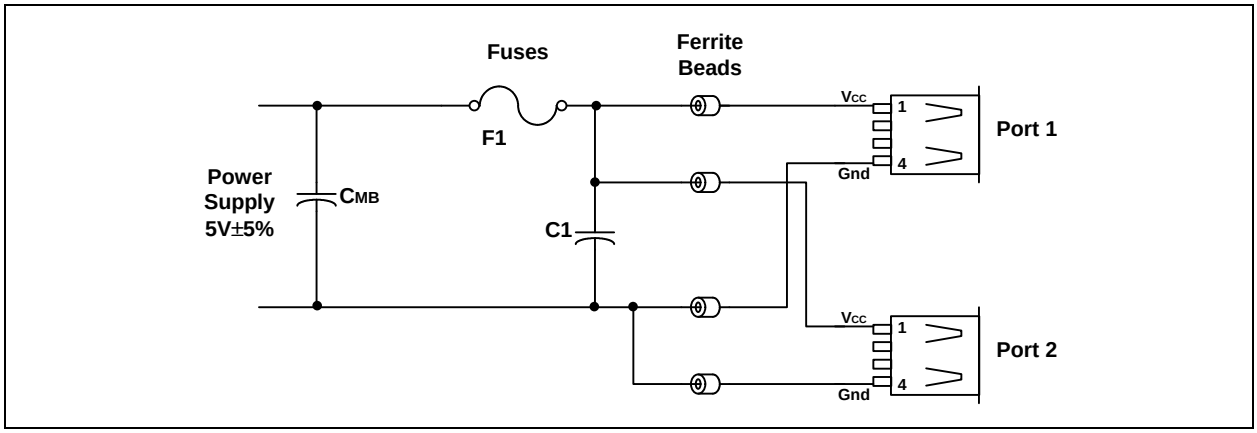


Figure A-4. Good Downstream Power Connection

A.2.3.3 Option #3 A Less Effective Design

This output circuit is less effective in meeting the VDROOP specification because the bulk capacitor is on the upstream side of the fuse, resulting in a high series resistance between the capacitor and the port. When a peripheral is hot plugged the fuse does tend to limit inrush current, but it also limits the ability of C1 to source current to the port. The recommended value of C1 tantalum capacitors is 150 µf, and CMB represent the motherboard capacitance.

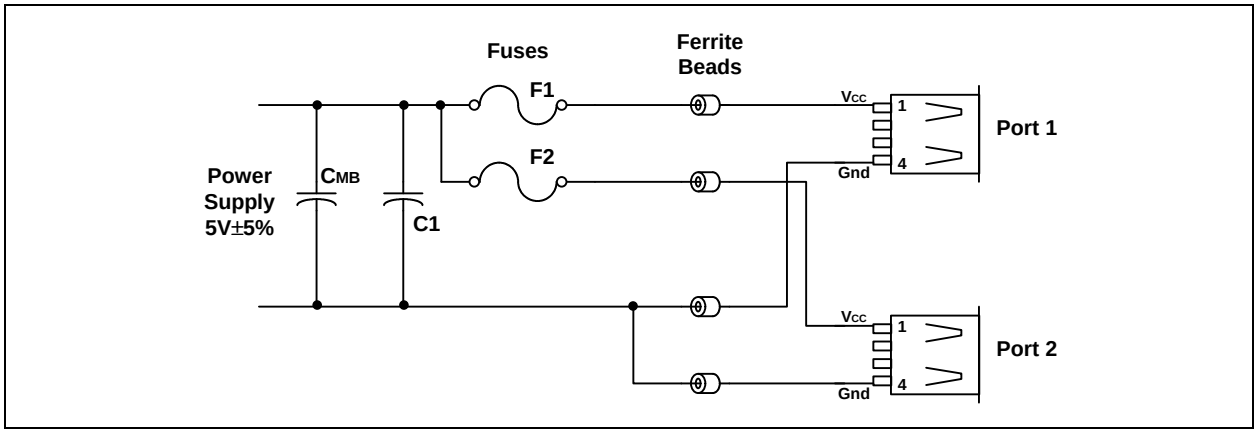


Figure A-5. Acceptable Downstream Power Connection

A.2.4 Power Line Layout Topologies Which Are Not Recommended

Figure A-6 through Figure A-8 illustrate unacceptable layout configurations. Topologies of this sort have been tested and were found to fail VDROOP tests. In all cases, the major problem was that the ratio of the impedance that controls inrush current and the impedance that limits how fast C1 can supply charge is too large. In particular, the circuit in Figure A-6 suffers from having a high impedance in series with the bulk capacitance.

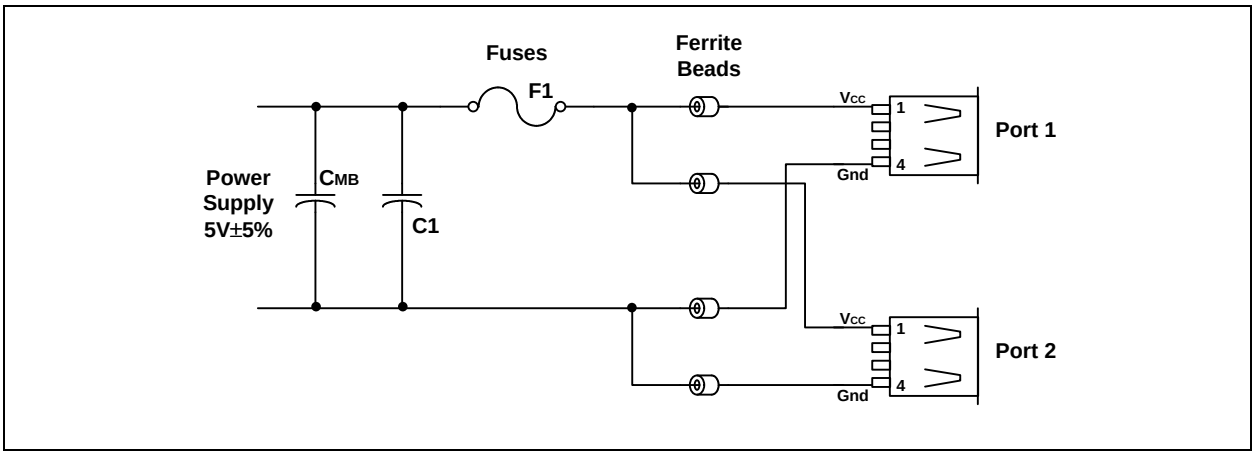


Figure A-6. Unacceptable Downstream Power Connection

The circuits in Figure A-7 and Figure A-8 suffer the problem that there is no inrush current isolation offered by per port ferrite beads. Whatever voltage drop occurs on port 1 also gets reflected onto port 2. The bulk capacitors are also isolated from the ports by the relatively high resistance of the fuse.

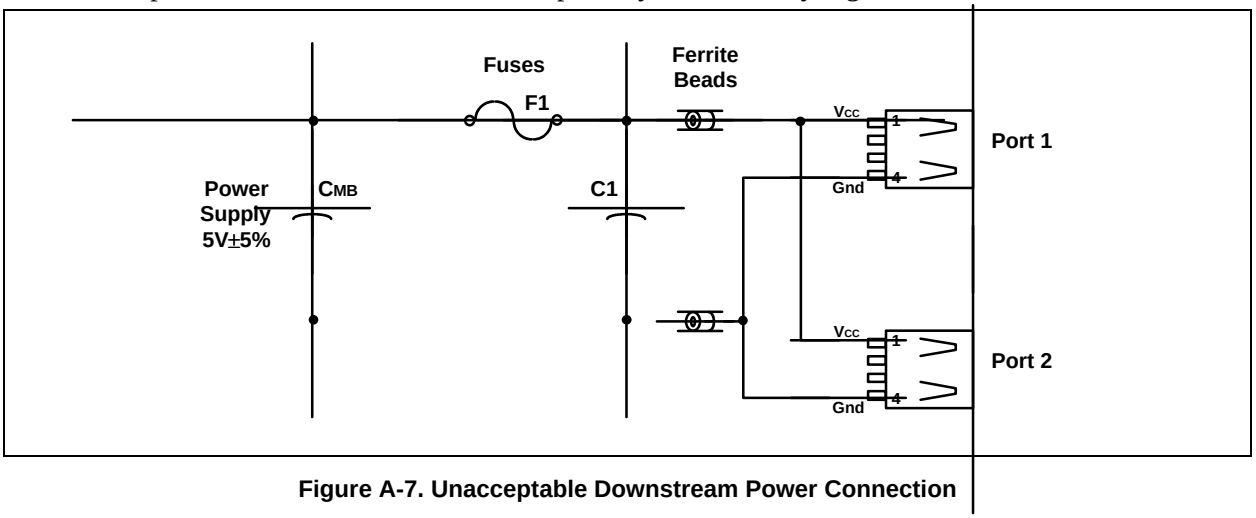


Figure A-7. Unacceptable Downstream Power Connection

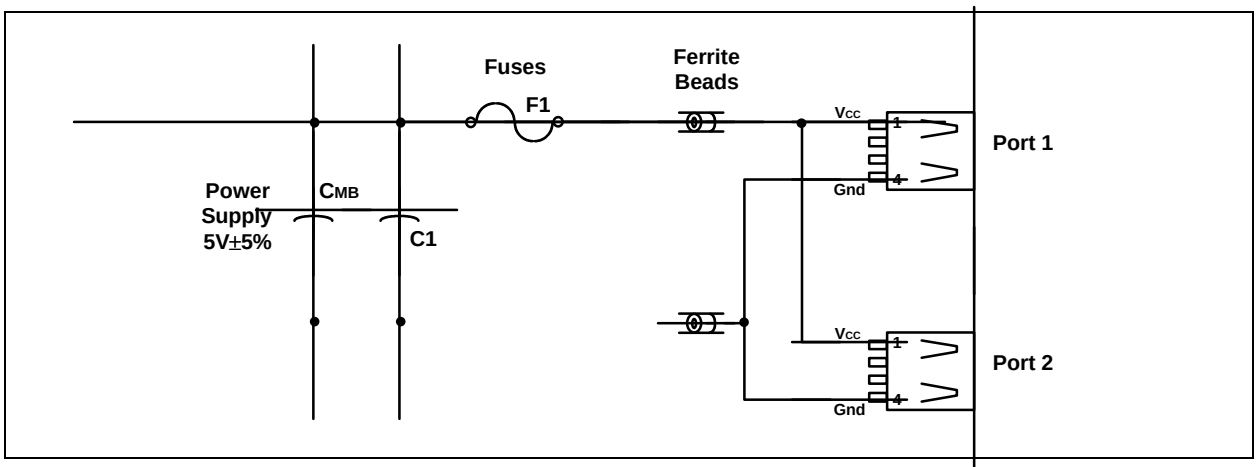


Figure A-8. Unacceptable Downstream Power Connection

A.3 Options for USB Connector and Cable Implementation

A.3.1 Recommended Options

There are three options recommended for attaching the USB signal and power lines to the external connector.

A.3.1.1 Option #1 USB Connector On Motherboard

The first is the simplest, as the connector attaches directly to the motherboard and no further design considerations are necessary.

A.3.1.2 Option #2 USB Connector On Riser Card

The second involves use of a printed circuit riser card to connect the USB lines from a motherboard header to a USB connector installed into a standard PC slot tab. The printed circuit riser card must be designed following the guidelines mentioned in the previous section A.2 and the following:

- The trace impedance for the P0±, P1± signals should be 45 ohms (to the ground) for each USB signal P+ or P-. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- There should be no series resistor on the riser card.
- The ferrite beads (and bypass capacitors if used) for EMI suppression should be placed on the riser card because they need to be as close as possible to USB connectors.
- The 68 µf or 150 µf tantalum capacitor should be placed between fuse and ferrite bead for each USB port on the riser card. Please refer to section A.2.3 for the recommended layout topologies.

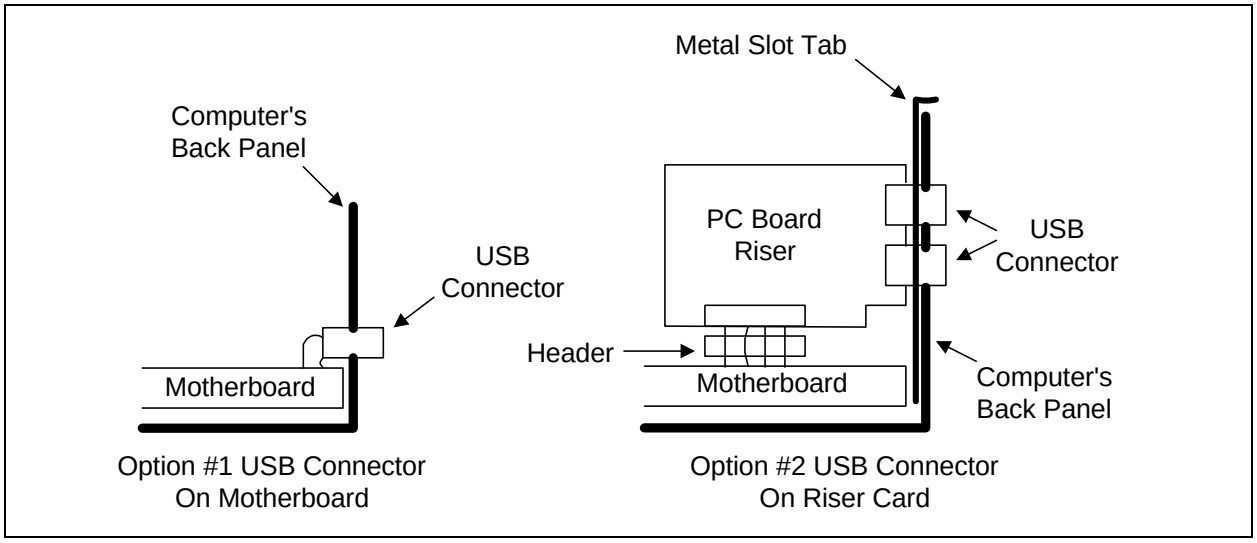


Figure A-9. Options For USB Connector

For the printed circuit implementation, it is important that the previously described guidelines for USB signal pairs on the motherboard and the riser card are 90 ohms. The following figure shows the impedance model of USB transmission lines with use of a riser card.

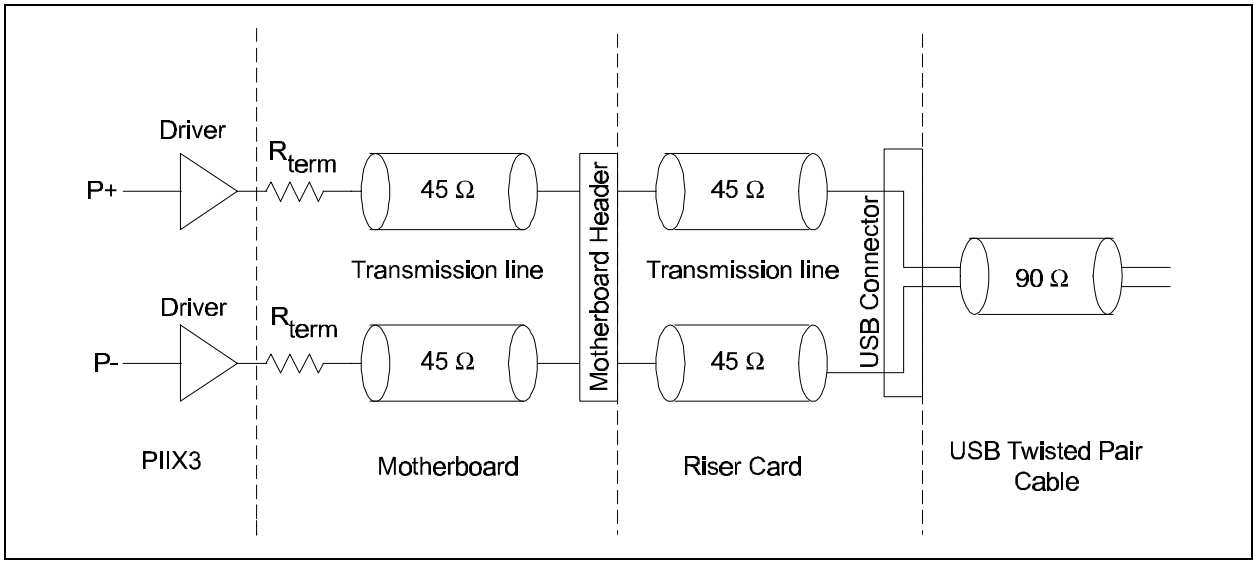


Figure A-10. USB Data Signals With Riser Card

A.3.1.3 Option #3 Use A Full Speed USB Cable

The third option involves use of a full speed USB cable to connect the USB lines from a motherboard header to a standard SHIELDED USB connector on the computer's back panel. A full speed USB cable is a shielded, twisted pair cable with a characteristic impedance (Z_0) of 90 ohm ±15%. The length of the cable needs to be as short as possible. It is recommended that the total length of the motherboard trace and the cable should not exceed ONE foot. Please refer to Chapter 6 in the *USB Specifications* for the detailed requirements on a full rated cable.

A.3.2 Not Recommended Options

A.3.2.1 Flat Ribbon Cable or Unshielded Twisted Pair Cable

The flat ribbon cable or an unshielded twisted pair cable should not be used to replace the printed circuit riser card due to adverse effects on circuit characteristics and EMI radiation. A system using these methods has high probabilities of failing EMI testing and having signal integrity problems.

A.3.2.2 Cable/Riser Card Combination

The cable/riser card combination is not recommended. This involves use of a cable to connect the USB lines from a motherboard header to a header on a riser card with USB connector on the riser card. A flat ribbon cable or an unshielded twisted pair cable is not recommended due to adverse effects on circuit characteristics and EMI radiation. It is also not recommended to use a full speed USB cable/riser card combination because it requires the match of the signal impedance between all three segments of the USB signals which ideally should be one segment on the motherboard. A system using these methods has high probabilities of failing EMI testing and having signal integrity problems.

A.4 USB on AGP Implementation

Besides routing the two USB signal pairs from the PIIX4 to two USB connectors, it is possible to route one signal pair to one USB connector and the other pair to an A.G.P. connector. This implementation is called USB on A.G.P.

A.4.1 USB Data Lines P+/P- and Power lines

To support USB on AGP, USB should be included on AGP add-in cards. When USB is included on the add-in card, there are two key issues that must be considered: signaling and power delivery. Each USB signal line on the add-in card should be designed to 45 ohm ± 15% to match the impedance of the USB driver and cable in order to preserve the signal integrity. Additionally, the power lines should be properly bypassed to decouple noise.

A.4.2 Motherboard Layout Options

There are two options that can be chosen for the motherboard. The zero-ohm stuffing option and the jumper.

A.4.3 Zero-Ohm Resistor Stuffing Option

Place zero-ohm resistors on the USB data signal. Provide two options during manufacturing. The first option connects USB from the PIIX4 to AGP. The second option connects USB to a connector on the motherboard. With each implementation, the system design engineer needs to ensure that the signal quality on USB signal pair (P+/P-) such as rise and fall time meet the USB specification requirements.

Figure A-11 illustrates how to implement the recommended zero-ohm resistor stuffing option.

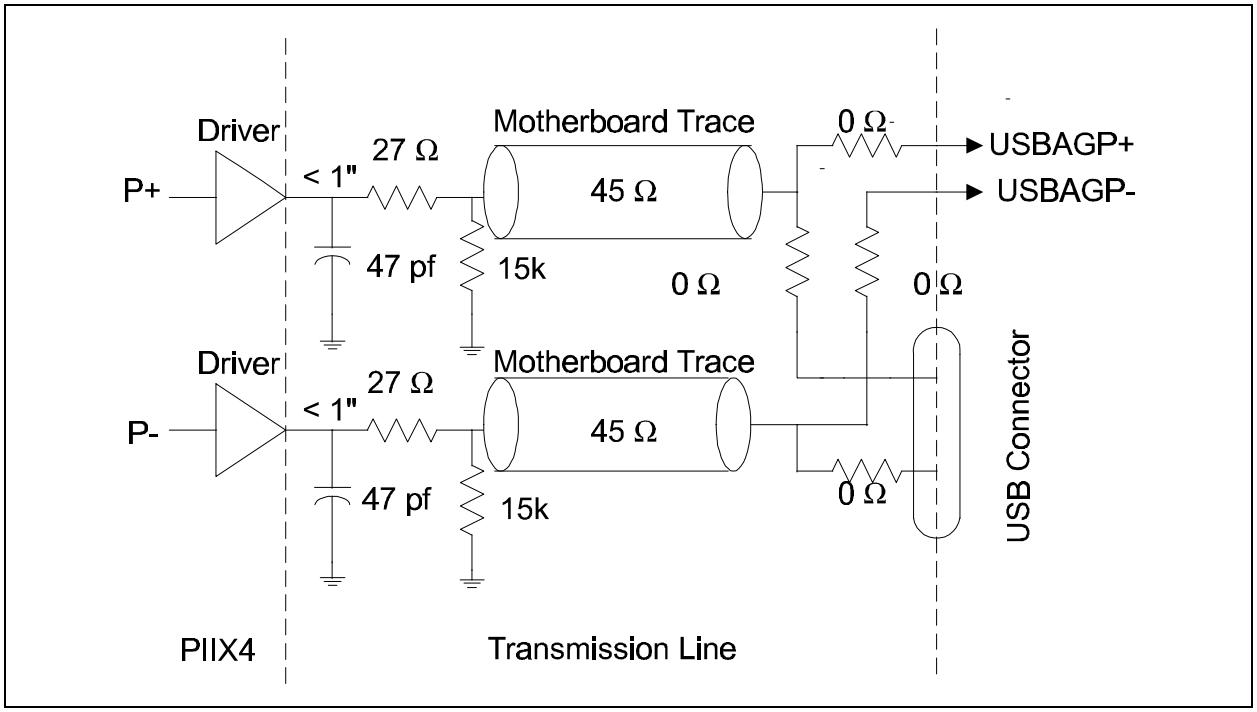


Figure A-11. USB Data lines in zero-ohm resistor stuffing option

A.4.4 Jumper Option

Placing jumpers on the motherboard. Choosing the correct jumper setting will steer one of the two USB signal pairs to either a USB connector or an AGP connector. The motherboard layout must support both configurations. In either jumper setting, the system design engineer needs to ensure that the signal quality on the USB signal pair (P+/P-) such as rise and fall time meet the USB spec requirements.

Figure A-12 illustrates how to implement the jumper option.

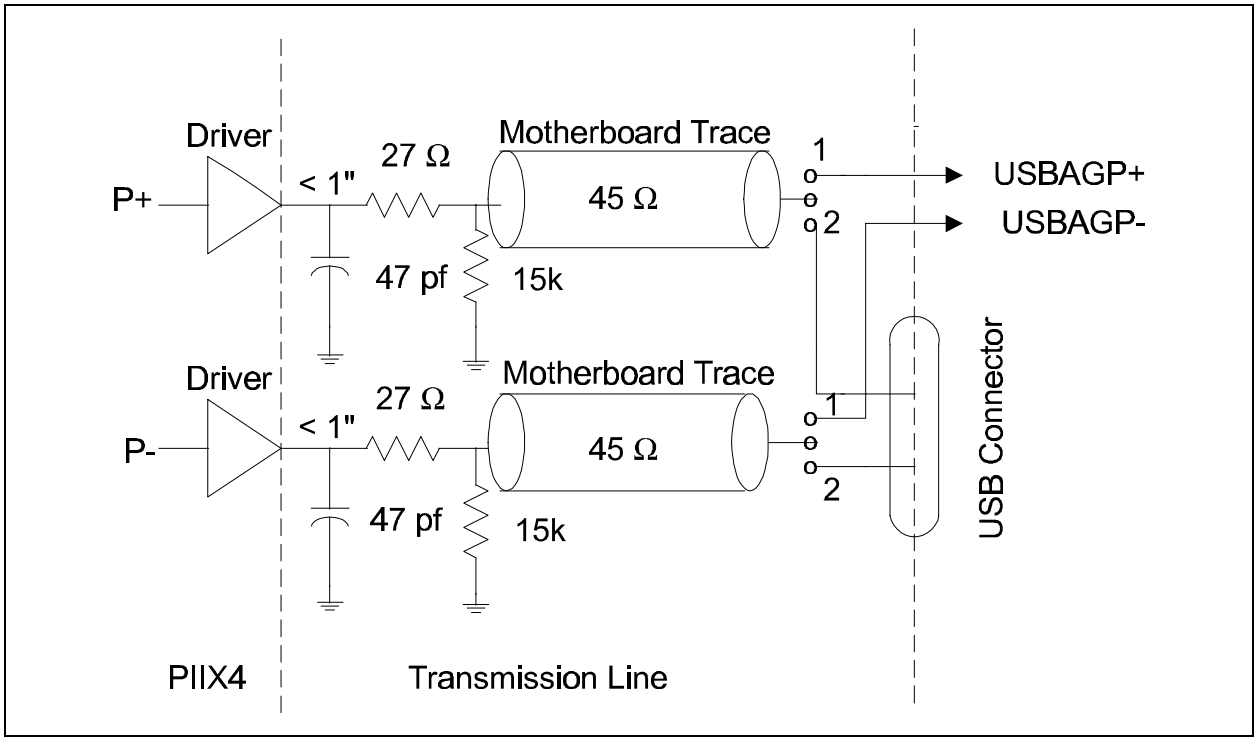


Figure A-12. USB data lines in jumper option.

A.4.5 Overcurrent Protection and Detection

An AGP card that supports USB and provides power for the USB cable, must implement overcurrent protection to comply with regulatory safety requirements (UL, CSA, etc.). To provide a means for an AGP card to report an overcurrent condition, the AGP connector has the OVRCNT# pin (pin B1 on the AGP connector), which should be connected to one of the two OC# pins on the PIIX4. The OVRCNT# pin on the AGP connector specifies a maximum voltage of 3.6V.

Figure A-13 illustrates the overcurrent protection and detection in zero-ohm stuffing option. Note that the devices inside the dashed line are populated on the motherboard only if the USB-only implementation is selected (by choosing the appropriate stuffing option for the zero-ohm resistors).

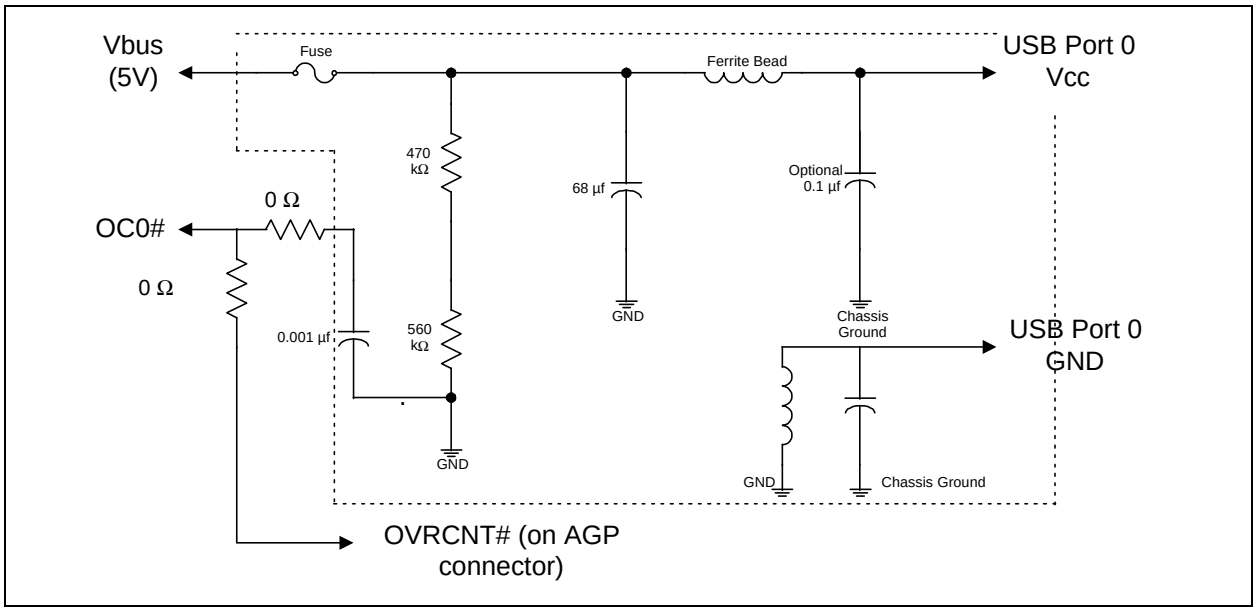


Figure A-13. Illustration of overcurrent protection in zero-ohm option

A.5 USB BIOS Implementation

PIIX4 contains a Universal Serial Bus interface with both host and hub control functions and two programmable USB ports. USB functionality is controlled by PIIX4 Function 2 (USB) configuration registers. This section is prepared to assist BIOS engineers in supporting PIIX4 USB function and is broken up into two parts. The first part contains USB BIOS programming requirements for not supporting USB legacy devices. The second part contains USB BIOS programming requirements for supporting USB legacy devices. In both cases, the USB interrupt needs to be set properly as shown below.

Interrupt Steering

Register Name: PIRQD Route Control Register

Offset: Function 0, 63h

Default Value: 80h(disabled)

The Universal Serial Bus (USB) Module interrupt is hardwired to the PIRQD# signal. PCI programmable interrupts (PIRQD#) needs to be internally routed to one of 11 interrupts (IRQ[15,14,12:9,7:3]) using the PIRQD Route Control Register. When the USB is enabled, the USB Host Controller in PIIX4 uses the PIRQD# input to the internal interrupt controller.

Level Triggered Mode

Register Name: Edge/Level Triggered Register

I/O Address: 4D0–4D1h

Default Value: 00h(edge triggered mode)

The PIRQx# lines are defined as active low, level sensitive to allow multiple interrupts on a PCI Board to share a single line across the connector. When a PIRQx# is routed to a specified IRQ line, the software must change the IRQ's corresponding ELCR bit to level sensitive mode.

A.5.1 Systems/Motherboards WITHOUT USB Legacy Support

For the systems or motherboards which DO NOT support USB legacy keyboard, the BIOS needs to enable the USB Function, select the USB Clock, and program the SOF Modify Register as shown below.

Program SOF Modify Register

Register Name: Start Of Frame(SOF) Modify Register

Offset: Function 2, base+(0Ch), bit 6:0

This one byte register is used to modify the value used in the generation of SOF timing on the USB. Only the seven least significant bits are used. Guidelines for programming this register are described in the section A.5.3 of this document. Additional information can be found in Chapter 7 of the *USB Specification.*

A.5.2 Systems/Motherboards WITH USB Legacy Support

The PIIX4 host controller must be enabled properly as described in section A.5.2.1 in order to determine if a legacy keyboard and/or mouse are present on the USB interface. The BIOS must be able to activate USB legacy devices early in the boot process. Before the operating system is loaded, the POST routine must detect, enumerate, and configure USB legacy devices as described in section A.5.2.2.

A.5.2.1 Enable and properly initialize USB function with the following registers:

Program SOF Modify Register See section A.5.1 & A.5.3

Register Name: Start Of Frame(SOF) Modify Register

Offset: Function 2, base+(0Ch), bit 6:0

Index Register Base Address

Register Name: I/O Space Base Address

Offset: Function 2, 20–23h, bit 15:5

The I/O Space Base Address Register contains the base address for the USB Index Registers. The BIOS should initialize and allocate the I/O space for the USB function. The I/O Space Base Address Register looks like the following:

A.5.2.1.1.1 I/O Space Base Address Register (PIIX4 Function 2 Offset 20–23h)

Bits 31:16	Bits 15:5	Bits 4:2	Bit 1	Bit 0
Reserved	**Read/Write**	**Read Only**	**Reserved**	**Reserved**
Read 0	Serial Interface Index Register Base Address	Read 0	Read 0	Read 1

I/O Space Enable (IOSE)

Register Name: Command Register

Offset: Function 2, 04–05h, bit 0. 1=Enable. 0=Disable.

This bit controls the access to the I/O space registers. If this bit is set, access to the host controller IO registers is enabled. The base register for the I/O registers must be programmed before this bit is set.

Bus Master Enable(BME)

Register Name: Command Register

Offset: Function 2, 04–05h, bit 2

This bit controls the PIIX4's ability to act as a master on the PCI bus for the host controller transfers. A value of 0 disables the device from generating PCI accesses. A value of 1 allows the device to behave as a USB host controller bus master. This bit must be set to 1 before serial bus transactions can start.

Allocate Interrupt Line

Register Name: Interrupt Line Register

Offset: Function 2, 3Ch, bit 7:0

Allocate a free interrupt, route it through the PIIX4, and configure it as level sensitive. Write this interrupt number into this register so it is accessible to USB software layers. The value in this register has no affect on PIIX4 hardware operations.

A.5.2.2 USB Legacy Keyboard Support for the PIIX4

Please refer to Universal Host Controller Interface(UHCI) Design Guide for information concerning legacy keyboard support.

A.5.3 START OF FRAME (SOF) Modify Register

I/O Address: Base + (0Ch)

Default: 40h

This 1-byte register is used to modify the value used in the generation of SOF timing on the USB. Only the seven least significant bits are used. When a new value is written into the these 7 bits, the SOF timing of the next frame will be adjusted. This feature can be used to adjust out any offset from the clock source that generates the clock that drives the SOF counter. This register can also be used to maintain real time synchronization with the rest of the system so that all devices have the same sense of real time. Using this register, the frame length can be adjusted across the full range required by the USB specification.

Frame Length (# 12 MHz Clocks)	**SOF Reg. Value**
(decimal)	**(decimal)**
11936	0
11937	1
.	.
.	.
11999	63
12000	64(default)
12001	65
.	.
.	.
12062	126
12063	127

The target frame period is 1.000 ms. For an exact 24.000-MHz or 48.000-MHz input frequency, the default divider from the 12-MHz data rate is 12,000 which produces a 1 ms frame period. However, we are allowing for the use of frequency synthesizers which provide frequencies with an offset error of up to 2200 ppm (part-per-million). This offset can be corrected by programming the SOF Modify Register with a compensating value. Please refer to section A.6.1 of this document for further explanation of the frequency offset.

1.00 ms frame period = USB data rate / (11936 + SOF Modify Reg. Value)	(eq. 4-1)
USB data rate(MHz) = (12 MHz) x (Frequency Offset(ppm) x 10^{-6} + 1)	(eq. 4-2)
(11936 + SOF Modify Reg. Value) x 10^{3} = (12 MHz) x (Frequency Offset(ppm) x 10^{-6} + 1)	(eq. 4-3)

If the frequency synthesizer driving the PIIX4 had a +1000 ppm frequency offset, then the PIIX4 would produce a data rate of 12.012 MHz, which is in spec. The 1.000 ms frame period can still be reached by programming the SOF Modify register to divide the data rate by 12,012.

SOF Modify Reg. Value = (12 x 10^{6} Hz) x (1000 ppm x 10^{-6} + 1) / 10^{3} - 11936 = 76 (decimal)

A.6 PIIX4 USBCLK Guidelines

A.6.1 Frequency Tolerance

The USB specification requires a data rate of 12 MHz ± 0.25% (2500 ppm) and an initial frame interval of 1.0 ms ± 0.05% (500 ppm). The data rate specification can be met with the PIIX4 by providing a USBCLK of 48 MHz with a 2500 ppm tolerance, including all sources of inaccuracy. The frame interval specification requires that the USBCLK frequency's unknown (variable) sources of inaccuracy are less than 500 ppm. Any known (fixed) offsets from 48 MHz can be compensated by programming the proper value into the PIIX4's SOF Modify Register.

The most straightforward method of providing USBCLK is from a canned 48.000-MHz crystal oscillator. It can provide a stable, exact frequency that is affected little by environment or loading. The default value of the SOF Modify register is sufficient to meet the frame interval timing.

Clock synthesizers provide a less expensive source of USBCLK. Most PC designs use a clock synthesizer for generating the CPU and I/O clocks. However, clock synthesizers are not as accurate and are susceptible to more environmental effects. They use a 14.31818-MHz crystal as the reference clock and a PLL to frequency multiply to the desired frequencies. The output frequency is an N-over-M integer ratio of the reference clock. It is generally not practical to use integers large enough that the output frequency is exactly 48 MHz. Frequency offsets from +2273 ppm to -1858 ppm have been seen from various manufacturers. Also, since clock synthesizers use a crystal as the frequency source, the crystal's tolerance and variations due to voltage, temperature, loading and aging have to be included when analyzing the suitability of using this source for USBCLK. (Some of this variation can be avoided if a 14.31818-MHz canned oscillator is used.)

System designers need to find out frequency offset values for 48 MHz and the crystal's variation due to capacitive loading, supply voltage, temperature, and aging from vendors. These values must meet the following:

-2500 ppm < Offset + crystal variables < +2500 ppm.

If multiple clock synthesizer vendors are chosen for a particular solution, system designers can do the following after finding out the offset values and crystal variation:

- Choose clock synthesizers to have a same offset or have their offsets + crystal variables within ± 500 ppm of each other so that a single value SOF programming works for all synthesizers.
- If one of clock synthesizers' offset is bigger than others, the OEM will have to change the BIOS value for the SOF Modify register programming depending on the offset value in order to meet the USB frame interval spec. Please see UHCI Design Guide for actual values to be programmed into the SOF Modify register to get the desired divisor.

For example, if the offsets of clock synthesizers are within ± 167 ppm of each other and if the variation for the 14.31818-MHz crystal is < ± 330 ppm, then the default value of SOF Modify register is OK. If the crystal variability is > ± 330 but < ± 500, then the SOF Modify register has to be programmed to divide by 12,002 to meet the 1.000 ms frame time.

A.6.2 PIIX4 USBCLK Requirements

This section outlines the recommended USB clock input specifications for a PIIX4 system design. The table below lists the AC timing requirements of the clock generation logic.

Table A-2. AC Timing Requirements

Symbol	Parameter	48 MHz		Units	Notes
		Min	Max		
Frequency Tolerance	USB CLK Frequency Tolerance		±2500	ppm	
tUKH	USB CLK high time	7		ns	1
tUKL	USB CLK low time	7		ns	2
tURISE	USB CLK rise time		1.2	ns	3
tUFALL	USB CLK fall time		1.2	ns	3
tJITTER	USB CLK Jitter, Cycle-to-Cycle		500	ps	4
tJITTER, Absolute	USB CLK Jitter, Absolute		±700	ps	
Duty Cycle	Measured at 1.5V	40	60	%	

NOTES:

1. tUKH is measured at 2.0V as shown in figure A-14.
2. tUKL is measured at 0.8V as shown in figure A-14.
3. tURISE and tUFALL are measured as a transition time through the threshold region Vol = 0.8V and
4. Voh = 2.0V.
5. Frequency Tolerance needs to be taken into the consideration in a particular implementation. See section A.5.3.

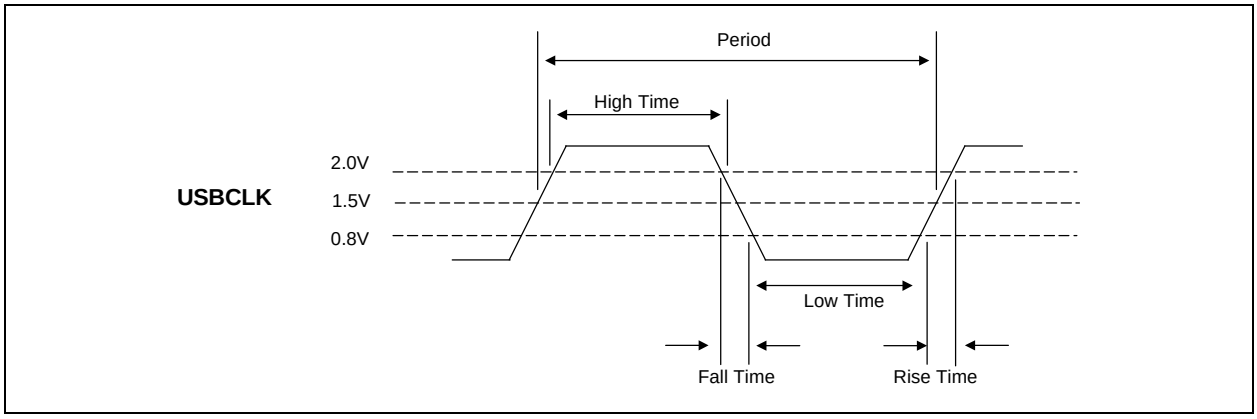


Figure A-14. USBCLK Waveform

A.6.3 USBCLK Jitter

In data acquisition or data recovery applications, clock jitter becomes an important system design consideration. The USB specification requires the source jitter for full speed data line to be less than 3.5 ns. This includes the jitter and skew caused by the frequency offset, from the source clock (USBCLK), and from other system variations such as buffer skew, noise effect, crosstalk effect, and loading conditions.

For a robust USB system, carefully consider the system variations if cycle-to-cycle USBCLK clock jitter is greater than 500 ps or frequency offset plus crystal variation is larger than 500 ppm. Choosing a USBCLK with a smaller clock jitter and frequency offset will provide a larger system jitter margin. The source clock jitter can be traded off against the frequency offset in a particular implementation as long as the 3.5 ns jitter budget is met.

The amount of the system jitter margin vs. source clock jitter and frequency tolerance is given in Figure A-15. The system jitter margin is obtained with the following equation.

System Jitter Margin(ns)=Source Data Jitter Budget(ns) - 7x(Frequency Tolerance(ppm)/12000) - USBCLK Jitter(ns) (eq.5-1)

For example, if clock synthesizers have USBCLK frequency tolerances within 500 ppm and cycle-to-cycle clock jitters within 500 ps, the system will have 2.708 ns system jitter margin.

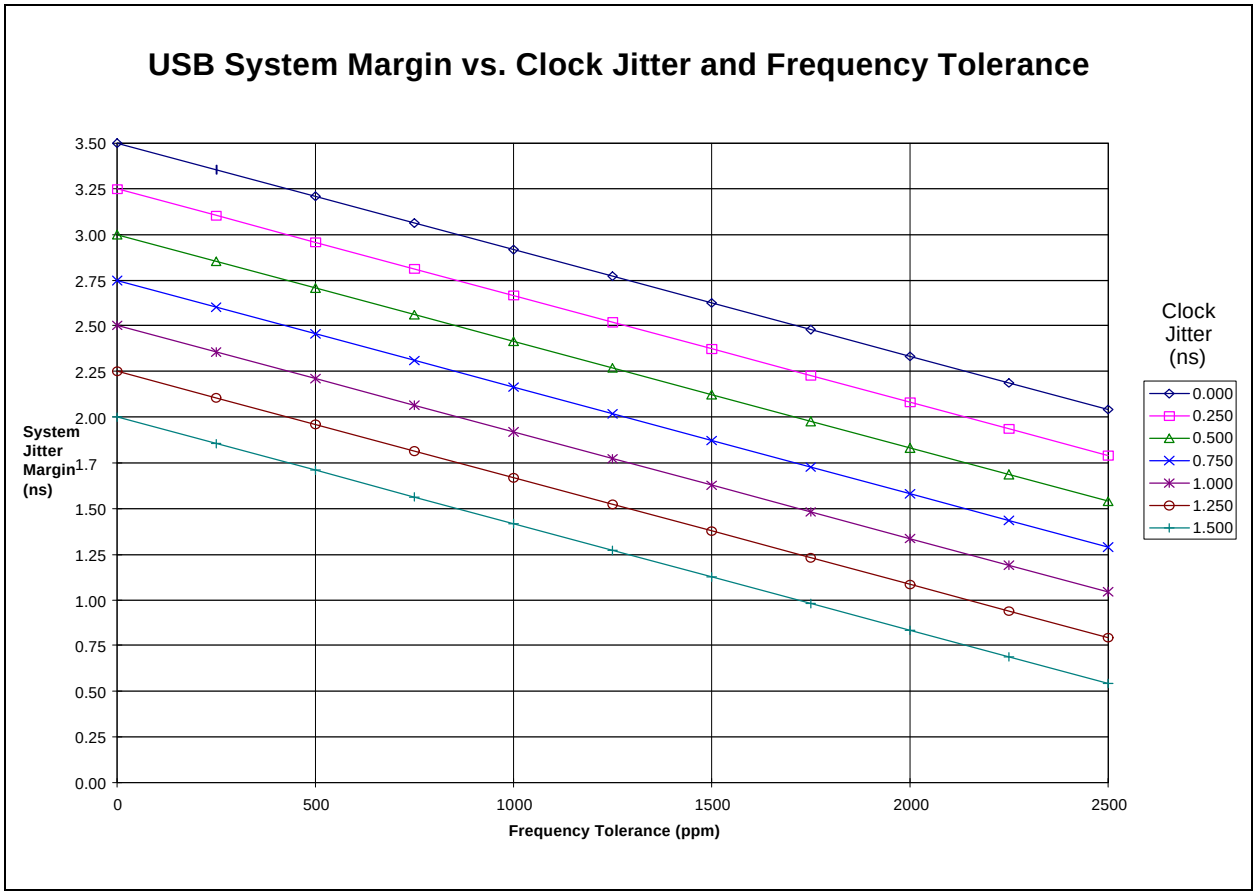


Figure A-15. System Margin vs USBCLK Jitter and Frequency Tolerance

A.6.4 System Considerations

The figures shown below are typical clock driver routing topologies.

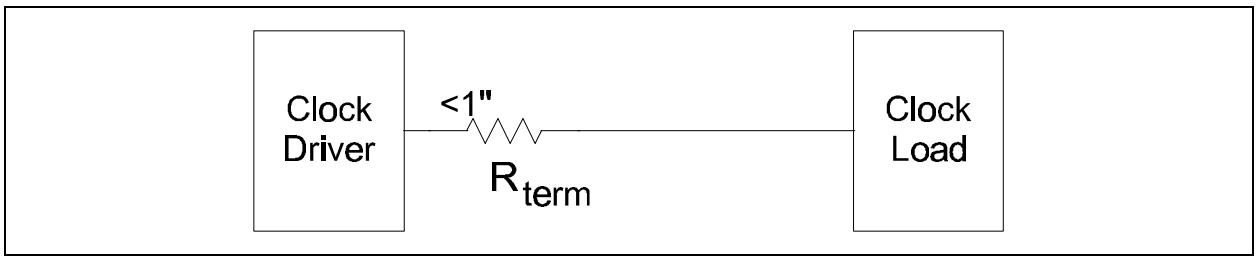


Figure A-16. Point to Point Route

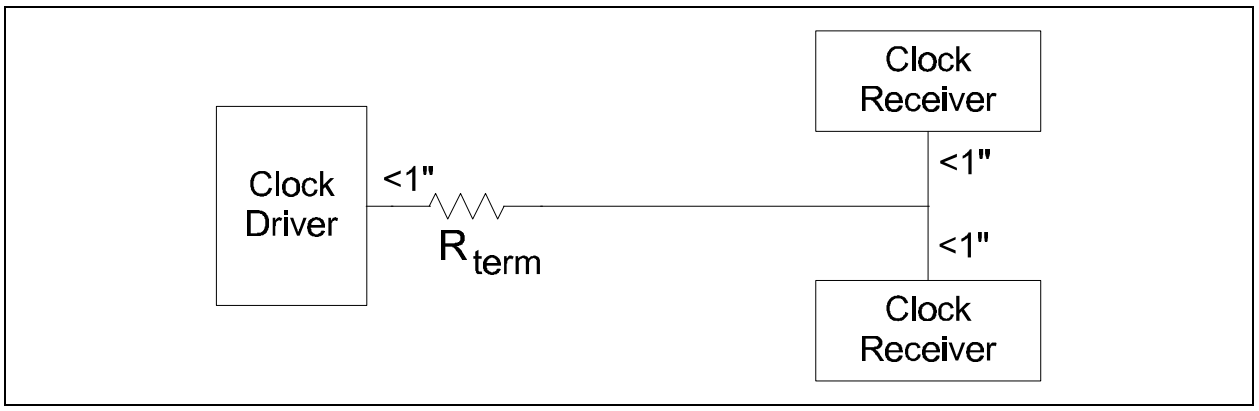


Figure A-17. Short Stub route, 2 balanced loads in close proximity, split at receiver

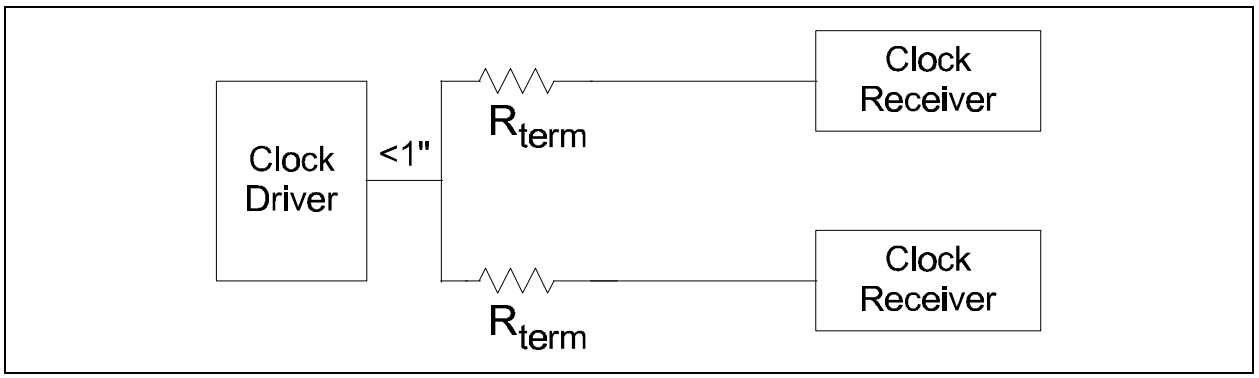


Figure A-18. Short Stub route, 2 unbalanced loads or large distances, split at driver

NOTES:

1. Series termination resistors may be required. Selection of layout topologies and buffer drive strength will determine termination requirements (resistor values).
2. Series termination resistors should be placed as close to the driver as possible (within 1 inch).

Table A-3. Maximum Expected Capacitive Loads on Clocks

Clock Type	Series Resistor Value[1]	Max. Trace Length[2]	Max. Rcvr Load	Notes
48 MHz	10Ω	15”	15 pF	2 motherboard loads

NOTES:

1. A 10 ohm resistor is used for 2 motherboard loads.
2. Trace length from the driver to the series resistor is assumed to a maximum of 1”.

A.6.5 USB Clock Source Vendors

Below is a list of company contacts which have a clock driver solution. The system designers are responsible for ensuring that a particular solution meets their requirements.

IDT Clock Synthesizer

Val Liva 408-654-6479

ICS Clock Synthesizer

Raju Shah 408-925-9493

Mike Kenneavy 408-467-1715

Cypress Semiconductor

Piyush Sevalia 408-943-2786

John Wenner 425-821-9202 x325

A.7 PIIX4 USB Design Checklist

A.7.1 Hardware Checklist

The system designer should also read and become familiar with the mechanical specification for the cables and connectors (Chapter 6) and the electrical specification (Chapter 7) in the *USB Specification*.

✓ box	
	READ and comprehend PIIX4 application note #1 V2.0, PIIX4 USB Design Guides and Checklist.

A.7.1.1 Motherboard Layout

✓ box	
	Terminate the unused USB port with 15K pulldown resistors on both P+/P- data lines.
	27Ω series resistors should be placed as close as possible to the PIIX4 (<1 inch).
	47 pf caps must be placed as close to the PIIX4 as possible.
	15K ±5% pulldown resistors on the USB data lines (P0±, P1±).
	The trace impedance for the P0±, P1± signals should be 45Ω (to the ground) each trace.
	The P+/P- signal pair must be routed together and not parallel with other signal traces. Double the space from the P+/P- signal pair to adjacent signal traces. The P+/P- signal traces must also be the same length.
	Ferrite beads and bypass caps are on VCC and VSS, the USB power and ground lines.
	A 120 µf tantalum capacitor between ferrite bead and EMI bypass cap on each power line.
	Use a PolySwitch or a standard fuse on VCC for each USB ports.

A.7.1.2 USB Connectors Checklist

✓ box		
	Recommended	USB connectors are attached to the motherboard directly.
	Or Use	USB connectors are on the riser card.
	Or Use	A full speed USB cable in the place of the riser card.
		The length of full speed cable should be as short as possible.
	NOT Recommended	(1) Flat ribbon cables or unshielded twisted pair cables.
		(2) or PC riser card and cable combination, where both a riser card and cable(any cable) are used.

A.7.1.3 USBCLK Checklist

✓ box		
	Clock Source:	Use a 48-MHz clock source.
	Duty Cycle:	Has a 40/60 duty cycle for 48 MHz.
	Frequency Tolerance:	<= ñ 2500 ppm
	Cycle-to-Cycle Clock Jitter:	<= 500 ps
	Series termination resistors are used on USBCLK routing (see motherboard layout guidelines section).	

A.7.2 BIOS Implementation Checklist

PIIX4 contains a Universal Serial Bus interface with both host and hub control functions and two programmable USB ports. USB functionality is controlled by PIIX4 Function 2 (USB) configuration registers.

✓ box	
	Read each PCIset's respective BIOS specification document

✓ box		Register Name	Function/Offset/IO Address
	Enable interrupt routing to one of the IRQ input	PIRQD Route Control Register	Function 0, Offset 63h
	Set Level Triggered Mode	Edge/Level triggered Register	I/O Address: 4D0–4D1h

A.7.2.1 Case 1) Systems/Motherboards WITHOUT USB Legacy Support

✓ box		Register Name	Function/Offset
	Adjust SOF Timing:	SOF Modify Register	Function 2, Base + (0Ch), Bit 6:0

A.7.2.2 Case 2) Systems/Motherboards WITH USB Legacy Support

Following registers are required to be initialized for USB function

✓ box		Register Name	Offset/Bits
	Assign I/O space:	I/O Space Base Address	Function 2, Offset 20h–21h, Bit 15:5
	Enable I/O Space:	Command Register	Function 2, Offset 04h–05h, Bit 0 = 1
	Enable Bus Mastering:	Command Register	Function 2, Offset 04h–05h, Bit 2 = 1
	Allocate a Free Interrupt:	Interrupt Line Register	Function 2, Offset 3Ch, Bit 7:0
	Adjust SOF Timing:	SOF Modify Register	Function 2, Base + (0Ch), Bit 6:0

A.8 USB Host Production Tester

Computer Access Technology Corporation

WWW: http://www.catc.com/

Kimberly McKay 408-727-6600

Price: $350–$700 Range

Computer Access Technology Corporation (CATC) is developing a USB Host Production Tester(HPT). The USB HPT is designed to test the functionality of the USB ports of USB capable motherboards and PCs as they come off the production line.

The HPT box can be configured by the HPT host software to behave as a full speed USB device or as a low speed USB device. The HPT software is a DOS program that runs a go, no go test on the USB Host PC unit under test. The program is limited to the production test function and does not run the complete USB software stack.

Please contact David J. Rogers, CATC's Director of Sales at (408) 727-6600, or send e-mail to DJR@CATC.COM with any questions or to request additional information. In the Asia/Pacific region, please contact the distributors below:

A.9 Main Distributors

DynaColor, Inc.
4F, No. 10, Lane 609, Sec. 5, Chung Hsin Rd,
Sanchung City
Taipei Hsien, Taiwan, R.O.C.
Mr. Charles Chuang
Phone: 886-02-278-1938 Ext. 6001
Fax: 86-02-278-1817
E-mail: dynacolor@ms2.hinet.net

Japan

TOYO Corporation
1-2, Hongokucho 1-chome
Nihonbashi, Chuo-ku
Tokyo 103
Mr. Junichiro Ishii
Phone: 81-33-245-1351
Fax: 81-33-271-4757
E-mail: toyocorp@po.iijnet.or.jp

Korea

Sepoong Industrial Co., Ltd.
3F, Joung Won Bldg.
1566-8, Seocho-Dong, Seocho-Ku
Seoul
Mr. Yewon Eom
Phone: 82-258-752-92

B

IDE Layout Clarification

APPENDIX B
IDE LAYOUT CLARIFICATION

B.1 Introduction

This document contains additional information in layout for the 82371AB (PIIX4). This information is to help clarify and give more information for laying out the PIIX4 in focusing on the IDE interface.

B.2 PIIX4 Implementation

B.2.1 IDE Routing Guidelines

This section contains guidelines for connecting and routing the PIIX4 IDE interface. The PIIX4 has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The current recommendations use 33 ohm resistors on all the signals running to the two ATA connectors, while the remaining signals use resistors between 22 and 47 ohm resistors.

Cabling

1. **Length of cable**: Each IDE cable must be equal to or less than 18 inches.
2. **Capacitance**: Less than 30 pF.
3. **Placement**: A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable it should be placed on the next closest connector to the end of the cable (6” away from the end of the cable).
4. **Grounding**: Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.

Motherboard

1. **PIIX4 Placement**: The PIIX4 should be placed as close as possible to the ATA connector(s).
2. **Resistor Location**: When the distance between the PIIX4 and the ATA connectors exceeds 4 inches the series termination resistors should be placed within 1 inch of the PIIX4. Designs that place the PIIX4 within 4 inches of the ATA connectors can place the series resistors anywhere along the trace.
3. **PC97 requirement**: Support Cable Select for master-slave configuration is a system design requirement for Microsoft* PC97. CSEL signal needs to be ground at host side by using a 470 ohm pull-down resistor for each ATA connector.
4. **Capacitance**: The capacitance of each pin of the IDE connector on the host should be below 25 pF when the cables are disconnected from the host.
5. **Series Termination**: The following resistor values are the current recommendations.

Signal	Resistor
PDD[15:0]	33 ohm
PDA[2:0]	33 ohm
PDIOR#	33 ohm
PDIOW#	33 ohm
PDDREQ	33 ohm
PDCS1#	33 ohm
PDCS3#	33 ohm
PDDACK#	33 ohm
IRQ14	22–47 ohm
RESET#	22–47 ohm

Signal	Resistor
SDD[15:0]	33 ohm
SDA[2:0]	33 ohm
SDIOR#	33 ohm
SDIOW#	33 ohm
SDDREQ	33 ohm
SDCS1#	33 ohm
SDCS3#	33 ohm
SDDACK#	33 ohm
IRQ15	22–47 ohm

- RESET comes from the PIIX4 RSTDRV signal through a schmitt trigger

One resistor per IDE connector is recommended for all signals. For signals labeled as 22–47 ohm, the correct value should be determined for each unique motherboard design, based on signal quality.

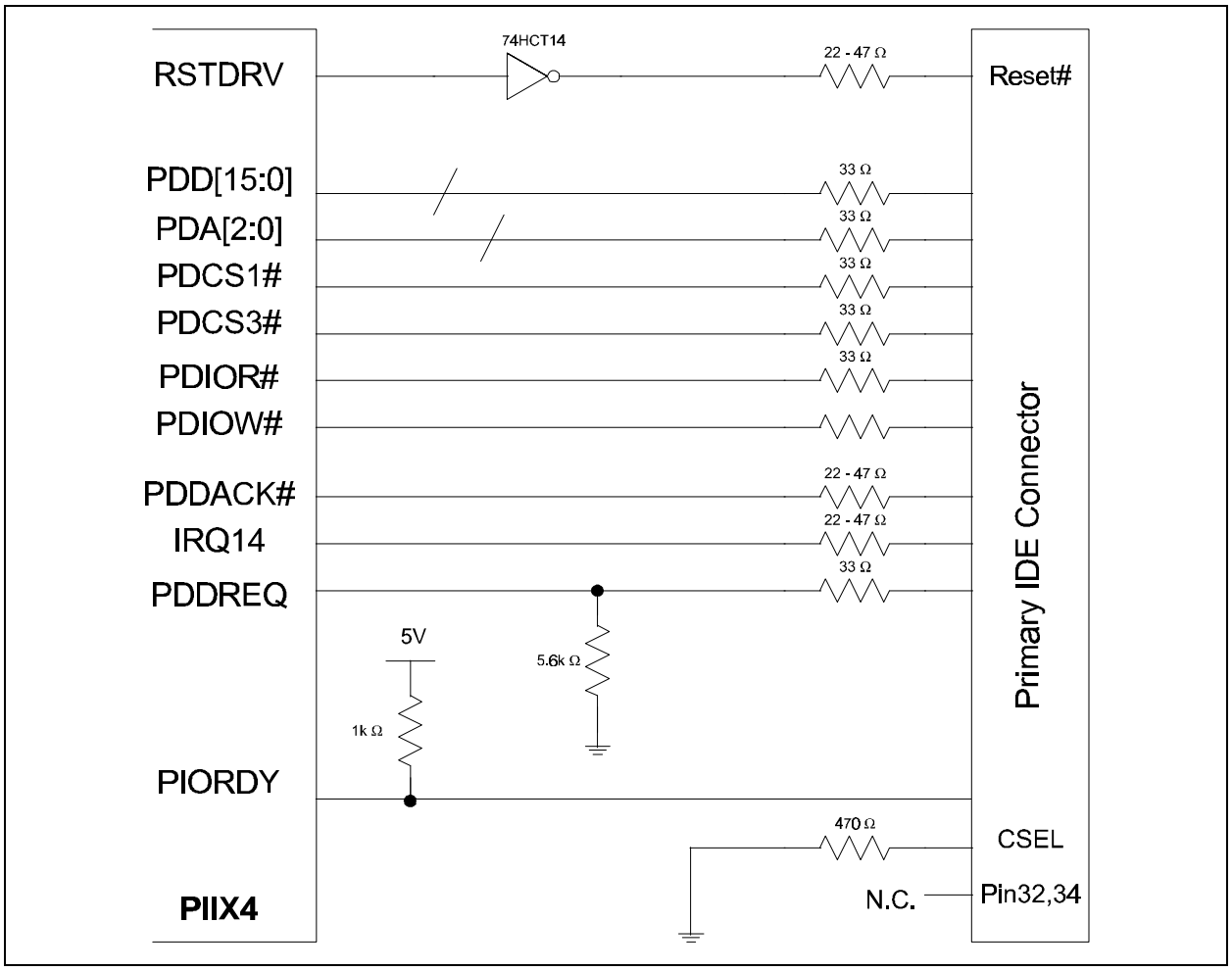


Figure B-1. Series Resistor Placement for Primary IDE Connectors

The design consideration shown in Figure B-1 illustrates the series resistor placement for trace lengths not exceeding 4 inches. Note that if the trace length between the PIIX4 and the IDE header exceeds 4 inches, the series resistors should be placed within 1 inch of the PIIX4. The series termination resistors are required in either design.

C

82371AB PIIX4
Internal RTC

APPENDIX C
82371AB PIIX4 INTERNAL RTC

C.1 Introduction

The 82371AB PIIX4 contains a Motorola MC146818A-compatible real-time clock (RTC) with 256 bytes of battery backed SRAM. This internal RTC module provides two key functions: keeping date and time and storing system data in its RAM even when the system is powered down.

This document presents how the PIIX4 RTC module is implemented, what affects the RTC accuracy, how RTC interrupts are implemented, and finally what are the differences between using an internal and an external RTC.

C.2 PIIX4 RTC Module Implementation

The PIIX4's internal RTC module provides two key functions: keeping track of date and time and storing system data, even when the system is powered down. The RTC has 242 bytes of general purpose RAM to store system data. Refer to section C.2.1, "RTC Registers and RAM," for a detailed discussion of the RTC RAM.

The RTC can also generate three types of interrupts: alarm interrupt, update ended interrupt, and periodic rate interrupt. Refer to section C.5, "RTC Interrupts," for more information on the PIIX4 RTC interrupts.

C.2.1 RTC Registers and RAM

C.2.2 RTC RAM Organization

The RTC battery backed RAM contains 256 bytes organized in two banks: the standard bank and the extended bank.

The standard bank has 128 bytes: 10 bytes indicating time and date information, 4 bytes used as four control registers (A, B, C, D)* which control the RTC function, and 114 bytes used as general purpose RAM.

The extended bank contains 128 bytes which are all used as general purpose RAM. Table C-1 is the summary of the RTC RAM organization.

Table C-1. Summary of the PIIX4 RTC RAM organization

	Standard RAM bank	Extended RAM bank
General purpose RAM	114 Bytes	128 Bytes
Control Registers	4 Bytes	None
Time and Date Registers	10 Bytes	None
Total	**128 Bytes**	**128 Bytes**

* See Section C.7 for a complete description of the RTC Control Registers

C.2.3 RTC RAM Access

Standard RAM is accessed through I/O locations 70h (index) and 71h (data). Refer to Table C-3 for the memory map of the standard RAM.

Extended RAM is accessed through I/O locations 72h (index) and 73h (data). The index of the 128 bytes of the extended bank is from 00h–7Fh.

Table C-2 is the summary of the I/O ports and index addresses for accessing the two RTC RAM banks.

Table C-2. Summary of I/O ports for accessing RTC RAM

	I/O index port	I/O data port	General purpose RAM index
Standard RAM	70h	71h	0Eh–7Fh
Extended RAM	72h	73h	00h–7Fh

Caution:

- Port 70h has a second function: bit 7 controls the enabling or disabling of NMI interrupt to the microprocessor; therefore, caution should be taken when writing to this port (bit 7 should not be changed).

Each bank of the RTC RAM can be enabled or disabled separately via the configuration space by setting bit 0 (for the standard bank) and bit 2 (for the extended bank) of the Real-Time Clock Configuration Register (RTCCFG). Refer to the Section C.8 for a complete description of the RTCCFG register.

Also, 8 bytes of RAM from index address 38h–3Fh of each bank can be locked or unlocked by setting bit 3 (for the standard bank) and bit 4 (for the extended bank) of the RTCCFG register. When the 8-byte range is locked, a write cycle to those locations will have no effect and a read cycle to those locations will not return valid data.

Caution:

- Bits 3 and 4 of the RTCCFG register are write-once bits that can only be reset by a hardware reset. No software means is possible to reset these two bits.
- Only PCI masters can access the internal RTC. ISA master access is not supported.

Table C-3. RTC standard bank memory map

Index Address	Name
00h	Seconds
01h	Seconds Alarm
02h	Minutes
03h	Minutes Alarm
04h	Hours
05h	Hours Alarm
06h	Day of Week
07h	Date of Month
08h	Month
09h	Year
0Ah	Control Register A
0Bh	Control Register B
0Ch	Control Register C
0Dh	Control Register D
0E–7Fh	114 bytes of general purpose RAM

C.2.4 RTC Time Keeping

C.2.4.1 Time keeping format

RTC keeps time in BCD or binary format. The format is determined by bit 2 of Control Register B. Hours can be represented either in 12 or 24 hour format which is determined by bit 1 of Control Register B.

Note: When changing the format, the time registers must be reinitialized to the corresponding format.

C.2.4.2 Accessing time registers

The time update occurs once per second if the SET bit of Control Register B is not asserted and the divide chain is properly configured (bits 6:4 of Control Register A). If a read from the time registers coincides with a time update cycle, the returned data may not be valid. Likewise, writes to time registers during a time update cycle may not complete properly.

Table C-4 recommends three alternate methods that should be used to safely access the time registers.

Table C-4. Methods to safely access time registers

Method	Description
1) Using SET bit of RTC Control Register B	Set bit 1 of RTC Control Register B to 1, which will abort the current time update and prevent subsequent update cycle from occurring until the bit is reset. Therefore, accessing the time registers before resetting the bit is safe.
2) Detecting update ended interrupt	The update ended interrupt indicates that an update cycle has just completed and the next update cycle will occur after 999 ms. Therefore, there is 999 ms available to access the time register safely.
3) Polling Update In Progress (UIP) bit of RTC Control Register A	If bit 7 (UIP) of Control Register A is detected low, there is at least 244 µs before the update cycle begins. Therefore, there is 244 µs available to access the time registers safely.

C.3 RTC External Connections

C.3.1 RTC Crystal

The PIIX4 RTC module requires an external oscillating source of 32.768 KHz connected on the X1 and X2 pins. Figure C-1 represents the internal and external circuitry that comprise the oscillator of the PIIX4 RTC.

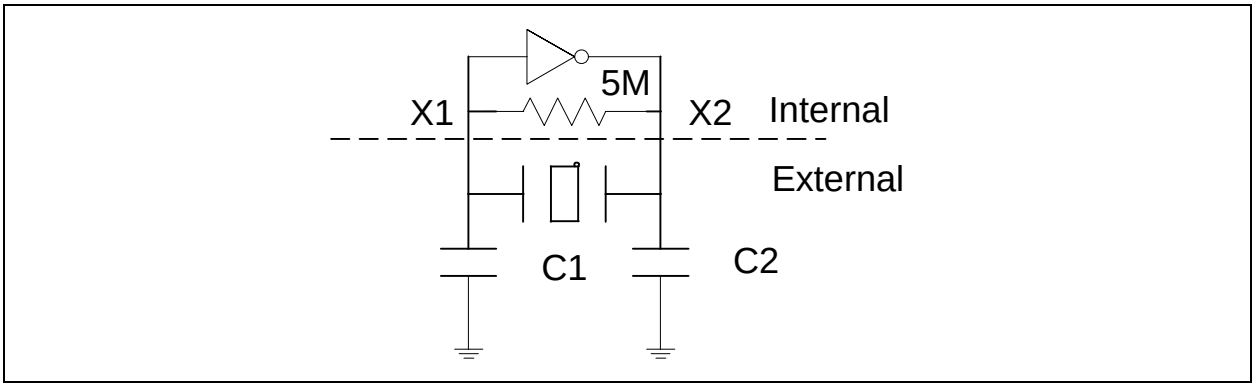


Figure C-1. External and Internal circuitry for the PIIX4 RTC

C1, C2 are the required external capacitors that affect the accuracy of the RTC. Choosing the right capacitor values is important to maintain the RTC accuracy. Section C.4 will present some guidelines for choosing these values.

Note: Even if the PIIX4 internal RTC is not used, it's still necessary to supply clock inputs to X1 and X2 of the PIIX4 because other signals are gated off that clock in suspend modes. However, in this case, the frequency accuracy (32.768 KHz) of the clock inputs is not critical; a cheap crystal can be used or a single clock input can be driven into X1with X2 left as no connect; Figure C-2 illustrates the connection.

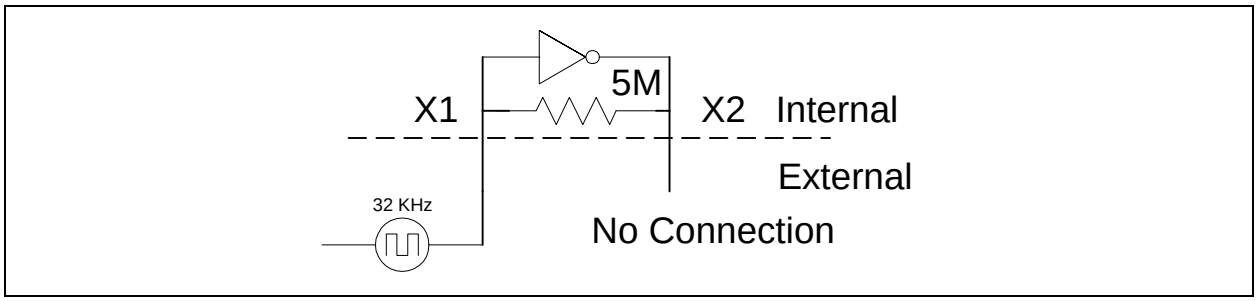


Figure C-2. Clock input connection to X1, X2 pins when not using internal RTC

C.3.2 RTC External Capacitor Values

To maintain the RTC accuracy, the external capacitor values should be chosen to provide the manufacturer's specified load capacitance (C_{load}) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values:

$$C_{load} = (C1 * C2)/(C1+C2) + C_{parasitic}$$

C2 can be chosen such that C2 > C1. Then C1 can be trimmed to obtain the 32.768 KHz.

C.3.3 RTC External Battery Connection

The RTC module requires an external battery connection to maintain its functionality and its RAM while the PIIX4 is not powered by the system.

The recommended batteries are: Duracell 2032, 2025 or 2016, which can give many years of operation.

Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 3 μA, the battery life will be at least:

170,000 μAh / 3 μA = 56,666h = 6.4 years.

The voltage of the battery can affect the RTC accuracy.

The battery must be connected to the PIIX4 via isolation diode circuit. The diode circuit allows the PIIX4's RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure C-3 is an example of a diode circuitry that is used.

As noted, a standby power supply should be used in desktop and mobile system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life.

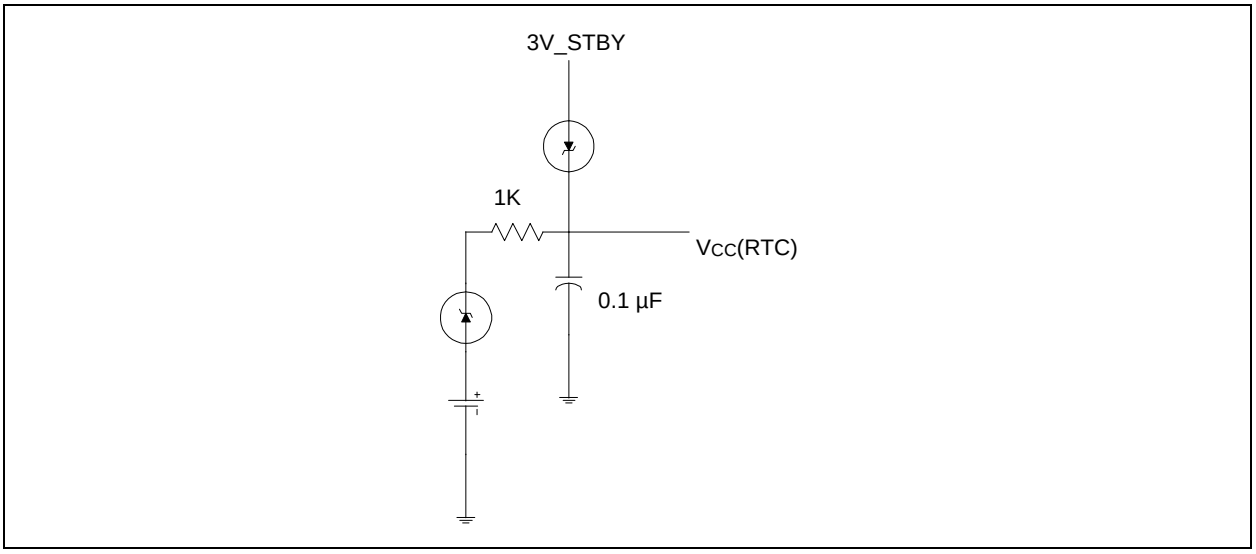


Figure C-3. A diode circuit to connect RTC external battery.

C.4 RTC Accuracy

The RTC accuracy can be affected by the following primary factors:

1. RTC voltage, VCC (RTC)
2. External crystal load capacitance
3. PIIX4 temperature
4. Crystal temperature

C.4.1 RTC Voltage versus RTC Accuracy

The RTC accuracy can be affected by the RTC voltage. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy (less than ±10 ppm*) can be obtained when the RTC voltage is in the range of 3.0V to 3.3V.

C.4.2 RTC External Capacitance Load versus RTC Accuracy

When the external capacitor values are combined with the capacitance of the trace, socket, and package, the closer that value can be matched to the actual load capacitance of the crystal used, the higher the RTC accuracy is. Refer to section C.3.2 for some guidelines to calculate the external capacitance.

C.4.3 PIIX4 Temperature versus RTC Accuracy

Generally, within the operating temperature of the PIIX4, the higher the PIIX4 temperature is, the lower the RTC accuracy is.

C.4.4 Crystal Temperature versus RTC Accuracy

The crystal temperature itself can affect the RTC accuracy; the higher the crystal temperature is, the lower the RTC accuracy becomes.

* ppm: parts per million. For example, +2 ppm means that for every one million seconds, there is a loss of two seconds. In other words, for one year, there is a loss of about 1.05 minutes.

C.5 RTC Interrupts

C.5.1 Types of RTC Interrupts

RTC can generate three types of interrupts: alarm interrupt, periodic interrupt, and update ended interrupt.

One of these interrupts is generated when the corresponding enable bit in Control Register B is set and an interrupt condition occurs. A read from Control Register C clears the active interrupt.

C.5.2 Alarm Interrupt

The alarm interrupt is controlled by bit 5 of the Control Register B. When enabled, the alarm interrupt occurs immediately after the time update of the seconds, minutes and hours which match the alarm settings.

- The alarm interrupt of the internal RTC, when enabled, is a resume event (via PIIX4's IRQ8#) to wake up the system from different power management states. For external RTC implementations, the external IRQ8# must be tied to one of the other resume input signals (GPI[1], LID, EXTSMI#, RI#) for the resume functionality.

C.5.3 Periodic Interrupt

The periodic interrupt is controlled by bit 6 of Control Register B. The desired period for the interrupt to occur is set by bits 3:0 (RS bits) of Control Register A.

C.5.4 Update Ended Interrupt

The update ended interrupt is controlled by bit 4 of Control Register B. When enabled, the interrupt occurs when an update cycle ends and the interrupt also indicates that the next update will occur after 999 ms.

- To avoid accessing invalid data from the time and date RAM locations (0–9), it is advised for the programmer to detect the update ended interrupt before reading from or writing to these RTC RAM locations. Refer to Table C-4 for more information.

C.5.5 RTC Interrupt Connections and IRQ8# Usage

The RTC interrupt is connected to ISA IRQ8#, and is internally routed within the PIIX4.

If the internal RTC is enabled (bit 0 of the RTCCFG is set—see 82371AB PIIX4 Data Sheet), the PIIX4's IRQ8# pin should be programmed as a general-purpose input, GPI[6] (by setting bit 14 of the PIIX4's General Configuration Register). However, if an external APIC is used, the PIIX4's IRQ8# becomes an output and must not be programmed as a general-purpose input.

Table C-5 summarizes the PIIX4's IRQ8# pin configuration depending on different usage of the RTC and APIC.

Table C-5. IRQ8# configuration with different scenarios

Internal RTC	External RTC	External APIC	PIIX4's IRQ8# should be selected as*
Used	Not used	Not used	GPI[6] (input)
Used	Not used	Used	IRQ8# (output)
Not used	Used	Not used	IRQ8# (input)
Not used	Used	Used	IRQ8# (input)

* Bit 14 of the PIIX4's GENCFG register will determine the configuration of PIIX4's IRQ8# pin.

C.6 Using Internal RTC versus Using External RTC

Table C-6 presents the differences for some issues between using an internal RTC and an external RTC. The following notations are used to describe how to change the value of a bit.

Set: set a bit to 1

Reset: set a bit to 0

Table C-6. Differences for some issues between using internal and external RTC

Issues	Using Internal RTC	Using External RTC
Control setting	Set bit 0 of the RTCCFG Register to enable the RTC. Bit 29–30 of the GENCFG Register should be set to select GPOs (instead of selecting RTCCS# and RTCALE), and depending on whether an external APIC is used or not, bit 14 of the GENCFG should be chosen to select either IRQ8# or GPI[6] accordingly (refer to Table C-5)	Reset bit 0 of the RTCCFG Register to disable the internal RTC and also reset bit 5 to allow subtractive address decoding. Reset bit 29–30 of the GENCFG Register to select RTCCS# and RTCALE. Set bit 0 of the XBCS Register to enable the RTCCS# and RTCALE signals. Finally, bit 14 of the GENCFG Register should be set to select IRQ8#. RTCCS# is used as chip select of the external RTC; the signal is asserted during a read from or write to I/O location 71h. RTCALE is used to latch memory address into the external RTC; the signal is asserted when writing to I/O port 70h with the appropriate RTC memory address.
RTC RAM accesses	Positively decoded—Fast	Subtractively decoded—Slower
Power plane	RTC power plane, VCC (RTC), is always powered by either the system power when available or an external coin cell battery.	VCC (RTC) can be tied to the suspend power plane, VCC (SUS), which is typically powered by the main power supply. Note that notebooks generally use Suspend-to-disk (STD)/Soft Off state rather than the Mechanical Off state. In STD state, the suspend well and also the RTC are powered by the main battery. Therefore, for notebooks, the only time the RTC well is powered by the coin cell is when the main battery has been removed.
Resume event for suspend modes	RTC alarm (via PIIX4's internal IRQ8#)	External RTC's IRQ8# must be connected to one of the PIIX4's resume signals (GPI[1], LID, EXTSMI#, RI#) because PIIX4's IRQ8# does not generate a resume event.

C.7 RTC Control Register Description

(The Section listed here is for convenience only. The 82371AB PIIX4 Data Sheet is still the standard reference document)

C.7.1 Control Register A

Address Offset: 0Ah

Default Value: NA—This register is not affected by any system reset signal.

Attribute: Read/Write

This register is used for general configuration of the RTC functions.

Bit(s)	Description
7	**UPDATE IN PROGRESS (UIP):** This bit may be monitored as a status flag. 1: signifies that the update of the timing registers is soon to occur or is in progress. 0: signifies that the update cycle will not start for at least 244 µs. The time, calendar, and alarm information in RAM is always available when the UIP bit is 0.
6:4	**Division Chain Select (DVx):** These three bits control the divider chain for the oscillator. DV2 DV1 DV0 Function 0 1 0 Normal Operation 1 1 X Divider Reset 1 0 1 Reserved 1 0 0 Reserved 0 1 1 Reserved 0 1 1 Invalid 0 0 0 Invalid
3:0	**Rate Select Bits (RSx):** Selects one of the 15 taps from the divider chain. The selected tap can generate a periodic interrupt if the PIE bit is set in register B. Otherwise this tap will set the PF flag of register C. If the periodic interrupt is not to be used, these bits should all be set to zero.

RS3	RS2	RS1	RS0	Periodic Rate
0	0	0	0	none
0	0	0	1	3.90625 ms
0	0	1	0	7.8125 ms
0	0	1	1	122.070 µs
0	1	0	0	244.141 µs
0	1	0	1	488.281 µs
0	1	1	0	976.5625 µs
0	1	1	1	1.953125 ms
1	0	0	0	3.90625 ms
1	0	0	1	7.8125 ms
1	0	1	0	15.625 ms
1	0	1	1	31.25 ms
1	1	0	0	62.5 ms
1	1	0	1	125 ms
1	1	1	0	250 ms
1	1	1	1	500 ms

C.7.2 Control Register B

Address Offset: 0Bh

Default Value: X0000XXXb

Attribute: Read/Write

This register is used for general configuration of the RTC functions.

Bit(s)	Description
7	**SET:** Enables the update cycles. 1: a current time update cycle will be aborted, and subsequent update cycles will not occur until SET is returned to 0. When SET is one, the BIOS may initialize time and calendar bytes safely. 0: time update cycle occurs normally once a second. This bit is not affected by RSMRST#.
6	**Periodic Interrupt Enable (PIE):** 1: Enables the generation of the Periodic interrupt. The rate of the Periodic interrupt is determined by bits 3:0 of Control Register A. 0: Disables the generation of the Periodic interrupt. This bit is cleared (set to zero) on active RSMRST#.
5	**Alarm Interrupt Enable (AIE):** 1: enables the generation of the Alarm interrupt. The Alarm interrupt occurs immediately after a time update of the seconds, minutes, hours which match the alarm settings. An alarm can occur once a second, once an hour, once a day, or once a month. 0: Disables the generation of the Alarm interrupt. This bit is cleared on active RSMRST#.
4	**Update-ended Interrupt Enable (UIE):** 1: Enables the generation of the Update-ended Interrupt, which occurs when the update cycle ends. 0: Disables the generation of the Updated-ended interrupt. This bit is cleared on active RSMRST#.
3	**Square Wave Enable (SQWE):** The Square Wave Enable bit serves no function in this device, yet is left in this register bank to provide compatibility with the Motorola 146818B. There is not SQW pin on this device. This bit is cleared on active RSMRST#.
2	**Data Mode (DM):** The Data Mode (DM) bit specifies either binary or BCD data representation. 1: Denotes binary format. 0: Denotes BCD format. This bit is not affected by RSMRST#.
1	**Hour Format (HF):** This bit indicates the hour byte format. 1: Selects twenty-four hour mode. 0: Selects twelve-hour mode. In twelve-hour mode, the seventh bit represents AM as zero and PM as one. This bit is not affected by RSMRST#.
0	**Daylight Savings Enable (DSE):** 1: Enables daylight savings on two special hour updates per year: One is on the first Sunday in April, where time increments from 1:59:59 AM to 3:00:00 AM. The other is the last Sunday in October when the time first reaches 1:59:59 AM, it is changed to 1:00:00 AM. The time must increment normally for at least two update cycles (seconds) previous to these conditions for the time change to occur properly. These special update conditions do not occur when the DSE bit is set to zero. The days for the hour adjustment are those specified in United States federal law as of 1987, which is different than previous years. This bit is not affected by RSMRST#.

C.7.3 Control Register C

Address Offset: 0Ch

Default Value: 00h

Attribute: Read/Write

This register is used for various flags. All flag bits are cleared upon active RSMRST# or a read of Register C.

Bit(s)	Description
7	**INTERRUPT REQUEST FLAG (IRQF):** Interrupt Request Flag = PF * PIE + AF * AIE + UF *UFE. This also causes the CH_IRQ_B signal to be asserted.
6	**Periodic Interrupt Flag (PF):** Periodic interrupt Flag will be one when the tap as specified by the RS bits of register A is one. If no taps are specified, this flag bit will remain at zero.
5	**Alarm Flag (AF):** Alarm Flag will be high after all Alarm values match the current time.
4	**Update-ended Flag (UF):** Updated-ended flag will be high immediately following an update cycle for each second.
3:0	**RESERVED** Read as 0.

C.7.4 Control Register D

Address Offset: 0Dh

Default Value: NA—This register is not affected by any system reset signal.

Attribute: Read/Write

This register is used for various flags.

Bit(s)	Description
7	**VALID RAM AND TIME BIT (VRT):** The Valid Ram and Time bit is set to one when the PWRGD (power good) signal provided is high. This feature is not typically used. This bit should always be set to 0 for write to this register.
6	**RESERVED:** This bit always returns a 0 and should be set to 0 for write cycles.
5:0	**DATE ALARM (DA):** These bits store the date of month alarm value. If set to 000000, then a don't care state is assumed. The host must configure the date alarm for these bits to do anything, yet they can be written at any time. If the date alarm is not enabled, these bits will return zeros to mimic the functionality of the Motorola 146818B. These bits are not affected by RSMRST#.

C.8 Real-Time Clock Configuration Register Description (RTCCFG)

(The Section listed here is for convenience only. The 82371AB PIIX4 Data Sheet is still the standard reference document)

C.8.1 RTCCFG—Real-Time Clock Configuration Register (Function 0)

Address Offset: CBh

Default Value: 21h

Attribute: Read/Write

This register is used to configure the internal Real-Time Clock.

Bits	Description
7:6	**Reserved:**
5	**RTC Positive Decode Enable:** 0 = PIIX4 Subtractively Decodes for RTC I/O registers. 1 = PIIX4 Positively Decodes for RTC I/O registers (default). The PCI cycles with addresses 70–73h are either positively or subtractively decoded based on this bit. The cycles are then routed to the internal RTC controller or forwarded to ISA based on bits 2 (extended bank) and bit 0 (standard bank) below. This bit should be set to 0 if the PIIX4's internal RTC is not used and the external RTC is on the PCI bus, or if subtractive decode is desired for an external RTC on the ISA or XBus.
4	**Lock Upper RAM Bytes:** 0 = Upper RAM data bytes 38h–3Fh in the extended bank are readable and writeable (default). 1 = Upper RAM data bytes 38h–3Fh in the extended bank are neither readable nor writeable. This is used to lock bytes 38h–3Fh in the upper 128-byte bank of RAM. Write cycles will have no effect and read cycles will not return a guaranteed value. **Warning:** This is a write-once register that can only be reset by a hardware reset. No software means is possible to reset this bit.
3	**Lock Lower RAM Bytes:** 0 = Lower RAM data bytes 38h–3Fh in the standard bank are readable and writeable (default). 1 = Lower RAM data bytes 38h–3Fh in the standard bank are neither readable nor writeable. This is used to lock bytes 38h–3Fh in the lower 128-byte bank of RAM. Write cycles will have no effect and read cycles will not return a guaranteed value. **Warning:** This is a write-once register that can only be reset by a hardware reset. No software means is possible to reset this bit.
2	**Upper RAM Enable:** 0 = Accesses to RTC Upper 128-byte extended bank at I/O address 72–73h is disabled. Accesses will be forwarded to ISA bus as determined by bit 5 of this register (default). 1 = Accesses to 72–73h are forwarded to RTC Upper 128-byte extended bank.
1	**Reserved**
0	**RTC Enable:** 0 = Accesses to RTC Lower 128-byte standard bank at I/O address 70–71h is disabled. Accesses will be forwarded to ISA bus as determined by bit 5 of this register. 1 = Accesses to 70-71h are forwarded to RTC Lower 128-byte standard bank. When this bit is reset, the upper bank of RAM may still be accessed (enabled via bit 2 in this register).

D

System Power Control

APPENDIX D
SYSTEM POWER CONTROL

The PIIX4 power management model was designed for use in mobile and desktop systems. Desktop systems are not fully optimized for the PIIX4 power management model. The main concern is circuit control when AC power is lost.

This document will describe a model for desktop power sequencing and an external hardware solution to allow PIIX4 based desktop systems to fit this model.

D.1 Desktop Power Environment

The current desktop power environment can be characterized by the following:

Power is supplied via 110/120V AC line current to a switching power supply. The current standard is the ATX power supply. One of its power outputs consist of a 5V trickle supply at a 10 mA minimum, which is always supplied when AC power is available. A mechanical switch may be optionally used with the power supply to disconnect the power supply from the AC power. Most ATX power supplies do not have this mechanical switch. The main power is a 3.3V supply voltage and other supply voltages controlled by an input signal called “PSON.” If PSON is asserted, these voltages are available from the power supply. If PSON is deasserted, these voltages are not available.

In the case of an ATX power supply with no mechanical switch, all power can be removed from the system in only two ways. The line cord can be removed from the wall or a power outage can occur causing AC power to be lost.

D.2 Desktop Power Sequencing Model

The desktop power sequencing describes how the desktop PC should function as its power is applied and removed from a varying number of scenarios.

The terminology “system context” describes general system context or state. It refers to the state of the operating system, software applications, general hardware registers (processor, chipset and other controllers, peripheral devices, etc.) and other general devices used by the system to perform its intended function. For a system to return to a condition such that the user perceives that the system was never turned off, the system must retain this system state. How this is performed in various power managed modes is described below.

The standard power states of a PC are described here using states potentially available with PIIX4 based systems. These states are:

1. Full On
2. Stop Grant/Sleep
3. Stop Clock/Deep Sleep
4. Suspended—Power on Suspend (POS)
5. Suspended—Suspend to RAM (STR)
6. Suspended—Suspend to Disk (STD)
7. Soft Off (SOFF)
8. Mechanical Off (MOFF)

For purposes of this discussion, the Full On, Stop Grant/Sleep, and Stop Clock/Deep Sleep states will be considered together as On states since typically no power is removed from the system in these states. Only the CPU clock is stopped in varying degrees. System events or user events can cause the system to return to Full On state with system context unchanged. It appears to the user that the system was always turned on. Latency to resume system is less than 1 ms. The Full On state is identified by the processor executing cycles at full speed. The Stop Grant/Sleep states are characterized by the processor stopping clocks in its internal core to a varying degree. In the Stop Clock/Deep Sleep state, the host clocks are stopped going into the processor.

The POS state maintains system context required for recovery in system registers and main memory. This state gets its power savings from stopping the high speed system clocks. DRAM refresh is performed with a low speed suspend clock or with self-refreshing DRAMs. No power is typically removed from system board. This state is primarily used in mobile computers. Desktop systems today seldom take advantage of this power savings mode due to additional cost of implementation. System events or user events can cause the system to return to Full On state with system context unchanged. It appears to the user that the system was always turned on with only the monitor screen off. Latency to resume system is approximately 20 ms.

The STR state maintains system context required for recovery in main memory. This state gets it power savings by removing power from all components except for DRAM, circuitry used to perform DRAM refresh and circuitry for monitoring resume events. An ATX power supply main power would not be switched off in this state. This state is primarily used in mobile computers. Desktop systems today seldom take advantage of this power savings mode due to additional cost of implementation. System events or user events can cause the system to return to Full On state with system context unchanged. It appears to the user that the system was always turned on with only the monitor screen off. Latency to resume system is approximately 1 second.

The STD state stores the system context onto a permanent storage device such as IDE hard disk. All power except trickle power can be removed from the system. The trickle power is used by the circuitry monitoring system resume events. When the system is resumed, the system context is restored from the hard disk. From a hardware viewpoint, the STD state is identical to Soft Off. System events or user events can cause the system to return to Full On state with system context unchanged. It appears to the user that the system was off, but returns to the condition it was in when suspended. Latency to resume system is less than 30 seconds.

The Soft Off state saves no system context. All power except trickle power can be removed from the system. The trickle power is used by the circuitry monitoring system resume events. When the system is resumed, it performs a normal startup (OS boot). From a hardware viewpoint, the Soft Off state is identical to the STD state. System events or user events can cause the system to return to Full On state. It appears to the user that the system was turned completely off and then turned on and booted. Latency to resume system is less than 30 seconds.

The Mechanical Off state may or may not save system context. If the system was in the STD state when it transitions to MOFF state, the system context can be recovered. If in any other state prior to transition to MOFF, all system context will be lost and the system must reboot the OS once power is restored. All power including trickle power is removed from the system. The only power on the system board comes from the RTC battery. This state is reached by the use of a mechanical switch on the power supply, unplugging of the AC wall cord, or from a loss of AC wall power. The system can be resumed only after AC power has been restored to the power supply. What the desired system functionality is when power is reapplied varies depending on the situation (see below).

The normal system transitions occur from the Full On state into one of the other Power States. This transition is all handled via program control, thus the system cannot transition from one power managed state directly to another (such as from POS to STD). It must transition from Full On to a particular power managed state and from that power managed state back to Full On. The only exception to this rule is the transition to Mechanical Off. This cannot be controlled via program control, since it is characterized by an external event (such as loss of AC wall power or unplugging of the power cord).

D.3 Recovery from Mechanical Off Condition

One of the primary concerns for desktop systems occurs when a system transitions from Mechanical Off state (i.e. AC power is reapplied to system). There are various scenarios which are desirable dependent on the state of the system prior to going to Mechanical Off. These are described in the following table:

	System State before transition to MOFF	System Context	System State After Power Returned	Miscellaneous
1	Full On, Stop Grant, Stop Clock	Lost	Full On	System can then transition into Stop Grant or Stop Clock if desired. System Boot required. See Note 1.
2	Full On, Stop Grant, Stop Clock	Lost	Soft Off	System does not power on. User or system event required for transition to Full On. System Boot required. See Note 2.
3	Power On Suspend	Lost	Full On	System can then transition into Power On Suspend if desired. System Boot required. See Note 1.
4	Power On Suspend	Lost	Soft Off	System does not power on. User or system event required for transition to Full On. System Boot required. See Note 2.
5	Suspend to RAM	Lost	Full On	System can then transition into Suspend to RAM if desired. System Boot required. See Note 1.
6	Suspend to RAM	Lost	Soft Off	System does not power on. User or system event required for transition to Full On. System Boot required. See Note 2.
7	Suspend to Disk	Maintained	Full On	System can then transition into Suspend to Disk if desired. System Boot not required. See Note 1.
8	Suspend to Disk	Maintained	STD	System does not power on. User or system event required for transition to Full On. System Boot not required. See Note 2.
9	Soft Off	No System Context	Soft Off	System does not power on. User or system event required for transition to Full On.

NOTES:

1. Used for system which must return to original state after power returns without user intervention. This is required by critical systems at remote sites for which user intervention to return to operation is not available.
2. Used when it is desired to not allow system to restart immediately after power returns. This may be needed at sites with large numbers of computers in order to limit power surge upon restoration of AC power.

A PIIX4 based system without external logic will in all cases above cause the system to restore to a Full On condition.

D.4 PIIX4 External Logic to handle power loss condition

This section presents an external hardware design which will allow a PIIX4 based system to operate similarly to the previously described model. The primary difference is that instead of placing the system into a true “Soft Off” state, the system will be placed into a “pseudo Off” state which requires the assertion of an active low signal to return to On. We will use the PWRBTN# signal attached to external push button, but any active low signal would be sufficient.

A General Purpose Output (GPO[x]) from PIIX4 is programmed to determine whether the user would like to come back to an ON state or whether the user would like to come back to a pseudo OFF state (described below as PWR_ON_OVERRIDE state) after restoration of AC power. The state is termed PWR_ON_OVERRIDE because it externally controls the assertion of the power supply “PSON” signal. This prevents the power supply from supplying the main or core power to the system board and thus holds the PWROK signal inactive.

The GPO value can be changed at any time by the system BIOS. This allows the BIOS to control this functionality for various system states. The truth table for this is shown below.

Note:

Do not use GPO[14] in this external logic because it defaults to a logical ‘0’ while all other GPO’s default to a logical ‘1.’

	GPO=1 (System comes up as on and software may set it back to where it was before power failure)	**GPO=0 (System comes up as off and user has to push the button to turn on the system)**
Full on, Stop Grant, Stop Clock	ON	PWR_ON OVERRIDE
POS	ON	PWR_ON OVERRIDE
STR	ON	PWR_ON OVERRIDE
STD	ON	PWR_ON OVERRIDE
Soft Off	ON	PWR_ON OVERRIDE

The external circuitry is shown below. The PIIX4 GPO signal is connected to the D input of the 74HC74 flip flop. It will be stored into the flip flop when the Power OK signal (PWROK) goes inactive. This may be during a normal system shutdown or during a power failure. The D flip flop is powered by the VBAT power plane, which is supplied by RTC battery when all system power is removed. The CMOS isolation transistor is used to isolate the flip flop from NAND gate when 5V Standby (5VSB) is not available and serves to eliminate any potential leakage current from the flip flop to the NAND gate when 5VSB power is not available.

The Q output of the flip flop is applied to the NAND gate along with the SUSC# signal from the PIIX4 (shown here as PX4_SUSC#). This controls the PSON# signal to the power supply. When Q=1, the PX4_SUSC# signal will flow through the NAND gate and directly control the power supply. When Q=0, the PX4_SUSC# signal will be blocked by the NAND gate (i.e. PSON# held inactive). In order to turn the system on in this case, an external, active low signal needs to be applied to the asynchronous PRESET (PRE#) input of the flip flop. This then allows the PX4_SUSC# signal to again directly control the power supply.

The logic connected to the flip flop asynchronous CLEAR (CLR#) is used during replacement of RTC battery with all system power removed. The RC delay associated with this circuit forces the Q output to 0 upon reinstallation of the RTC battery. This forces the requirement of asserting the PRE# circuit logic to turn the system back on.

Figure D-1 differs from the schematic in Appendix H. The functionality is the same, but the implementation is different. Neither Figure D-1 nor the circuit in the schematics support waking from a suspend state. To support suspend wake up, additional logic is needed.

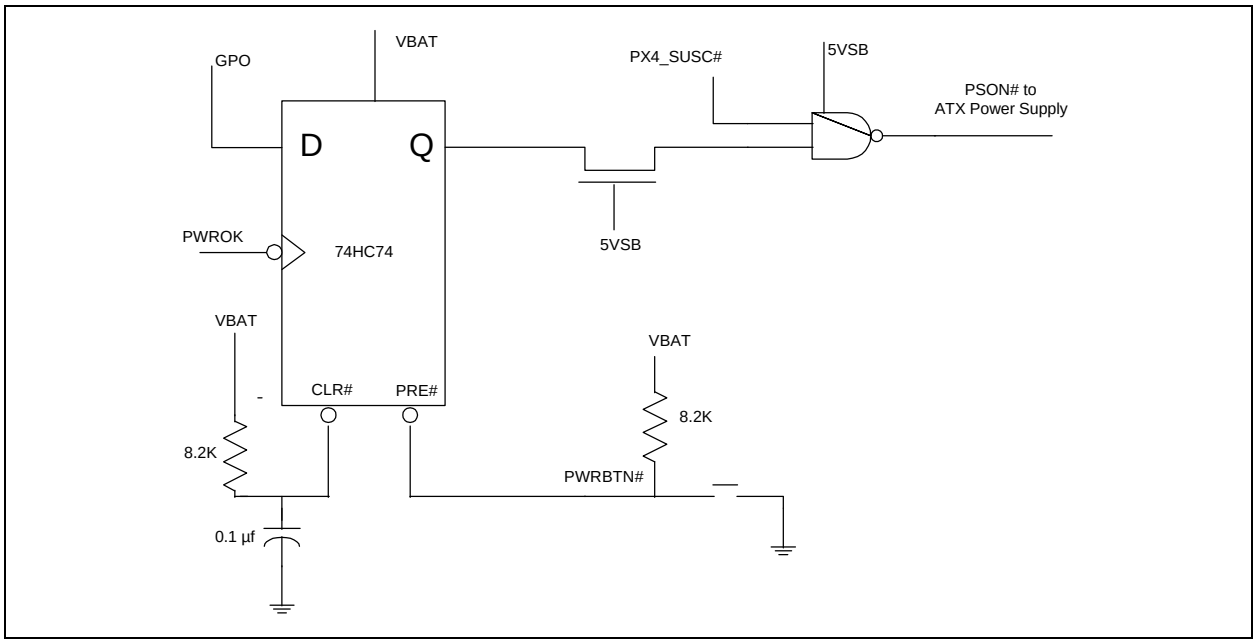


Figure D-1. External Logic to Handle Power Loss

	GPO	PWROK	PRE#	CLR#	Q	PSON#	Comments
	0	Falling	1	1	0	1	OFF
	1	Falling	1	1	1	!PX4_SUSC#	ON
	x	x	0	1	1	!PX4_SUSC#	ON
	x	x	1	0	0	1	OFF
	x	H	1	1	Qo		HOLD

OFF = Main power supply is off, but standby (or trickle) current is on.

ON = Main power supply is on. Software then takes over to place the system into the desired sleep or working state.

Note:

In Appendix H a J-K Flip-Flop is used, while here we use a D Flip-Flop. Neither solution will support wake events other than the power button. To support additional wake events, other logic would be needed.

E

System Management Bus (SMBus) Overview

APPENDIX E
SYSTEM MANAGEMENT BUS (SMBUS) OVERVIEW

Intel introduced the SMBus in 1994. The SMBus is a subset of the I^2C (Inter-IC) bus, which was developed by Philips Semiconductors.

E.1 SMBus Functional Description

The SMBus is a bi-directional, two-wire serial interface which is an inexpensive, simple, but powerful method for controlling and getting information from devices on a motherboard. Specifically, through SMBus, a device can provide manufacturer information, tell the system its model/part number, save its state for a suspend event, report different types of errors, accept control parameters, and return its status.

E.2 SMBus Features

- Only two bus lines are required: a serial data line (SMBDATA) and a serial clock line (SMBCLK). These two lines are open collector and require external pullups.
- Data transfers are serial, 8-bits long, and bi-directional with the Most Significant Bit transferred first.
- Each device has one unique address which is seven bits long with a read/write bit appended in bit position 0.
- A multi-master bus including collision detection and arbitration to prevent data corruption.
- Based on fixed voltage levels.
- Implements device time-outs.

E.3 SMBus Command Protocols

SMBus supports eight possible command protocols which a device can use to communicate with the rest of the system: Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read, and Block Write. For a detailed discussion of the SMBus Command Protocols, refer to the System Management Bus Specification.

E.4 Device Addresses

Each SMBus device has a unique address which is assigned by Intel (for SMBus) and by Philips (for I^2C). These pre-assigned addresses are exclusive, with no overlapping for SMBus and I^2C. See System Management Bus Specification for more details on the address assignments. Every address is seven bits long with a read/write bit appended to bit position 0.

E.5 Start and Stop Conditions

Start and stop are unique conditions defined to start and stop a transfer on the SMBus. A high to low transition on the SMBDATA line while SMBCLK is high is the start condition. A low to high transition on the SMBDATA line while SMBCLK is high is the stop condition. Start and stop conditions are always generated by the Master. Figure E-1 shows the start and stop conditions on SMBus.

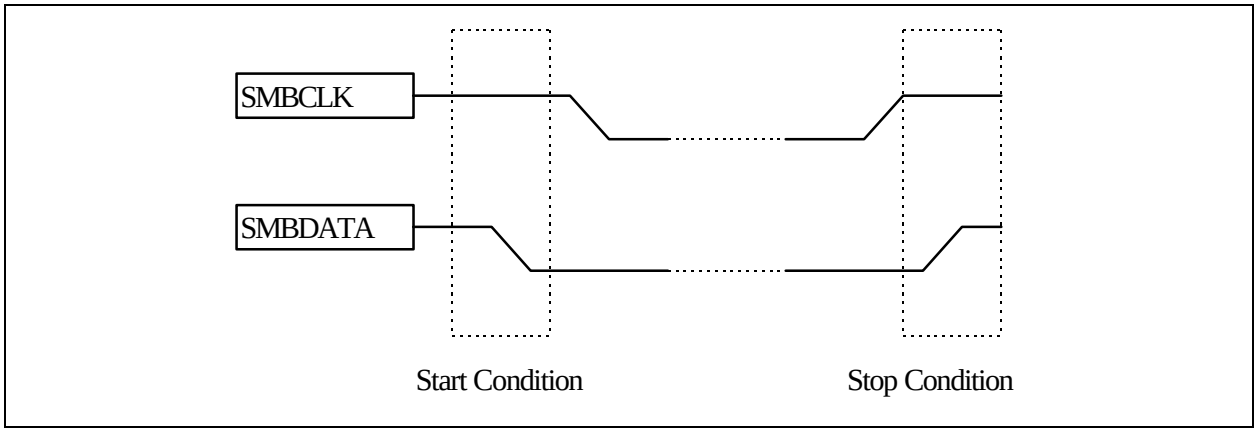


Figure E-1. Start and Stop conditions on SMBus

E.6 Data Validity

The data on the SMBDATA line must be stable while the clock on the SMBCLK line is high. The data can only change while the clock is low. Figure E-2 illustrates when the data is valid and allowed to change on the SMBus.

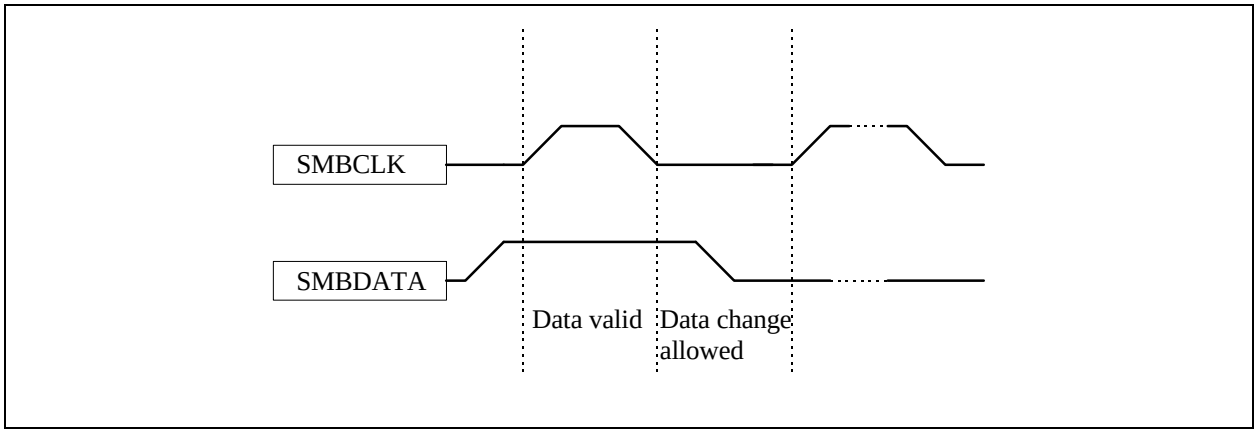


Figure E-2. Data validity on SMBus

E.7 MAIN Differences Between SMBus AND I²C

Table E-1 summarizes the key differences between SMBus and I²C bus.

Table E-1. Key differences between SMBus and I²C

Differences	SMBus	I²C Bus
Voltage logic levels	Fixed voltage levels (see SMBus spec). However, the SMBus logic levels are easily met using standard 5V components.	Voltage levels are scalable to V_{DD}.
Operational clock frequency	Specified as 10 KHz–100 KHz.	100 KHz max for Standard Mode 400 KHz max for Fast Mode No min spec.
Device time-outs	Time-out occurs when clock is held low between 25 ms and 35 ms.	No specification
Maximum bus capacitance	No specification, which means the number of devices connected to the bus is not limited by the bus capacitance.	Specified as 400 pF, which limits the number of devices connected to the bus.
Cumulative clock low extend time (for slave device), $T_{low:sext}$	A slave device is allowed to stretch the cumulative clock low time, for the entire transaction, up to a maximum of 25 ms. (If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.)	No specification
Cumulative clock low extend time (for master device), $T_{low:mext}$	A master device is allowed to stretch the cumulative clock low time, in a single byte, up to a maximum of 10 ms.	No specification
Master/Slave protocol	Specifies the protocol (the modified Write Word protocol) that an SMBus device uses when becoming a master to communicate with the SMBus Host acting as a slave device.	No specification
Block level transfer protocol	SMBus specification requires a command code byte and a byte-count byte to be added after the slave address when performing a block read/write. Block transfer is limited to a maximum of 32 data bytes.	I²C does not require the command code byte or byte-count byte, and treats all bytes after the address as pure data bytes. I²C does not limit the number of bytes transferred in this protocol.

E.8 PIIX4 SMBus Implementation

To interface with the SMBus, the PIIX4 provides a SMBus host controller and a SMBus slave interface which includes a host controller slave port, and two slave shadow ports. Figure E-3 illustrates the PIIX4 SMBus implementation model.

The PIIX4 also supports the SMBus ALERT# protocol which provides a means for a slave-only device to communicate with the host. See the System Bus Management for more details on SMBus ALERT#.

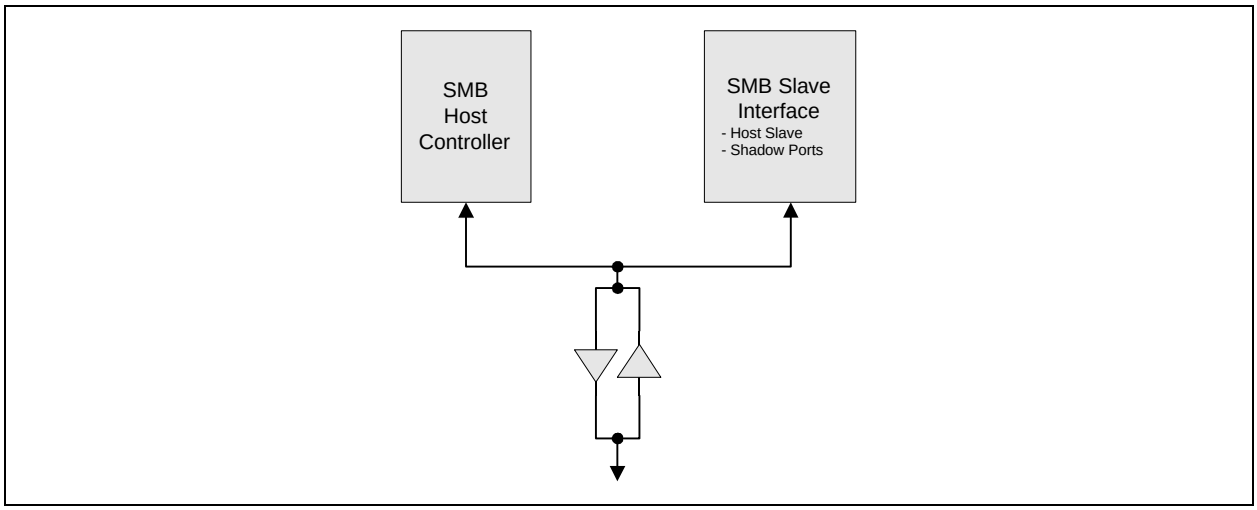


Figure E-3. PIIX4 SMBus implementation model

E.8.1 PIIX4 SMBus Host Controller

The PIIX4 SMBus Host Controller is used to send commands to various SMBus devices. The PIIX4 SMBus controller supports seven command protocols of the SMBus: Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Block Read, and Block Write. PIIX4 does not support Process Call.

The PIIX4 SMBus controller has 3.3V input buffers, which requires the system's SMBus to be designed with a 3.3V termination voltage. For interfacing 5V devices with the PIIX4 SMBus, refer to section E.9.2 for more information.

E.8.2 PIIX4 SMBus Host Transaction

To execute a SMBus host transaction, the following elements of the transaction are first set up:

- The type of transfer protocol (set by bits 4:2 of SMBHSTCNT register)
- The address of SMBus device and read/write bit (bits 7:0 of SMBHSTADD register)
- The command code in the SMBus protocol (bits 7:0 of SMBHSTCMD register)
- The data (for a write) to be transmitted (bits 7:0 of SMBHSTDAT0 and/or SMBHSTDAT1)
- Any control bits (bits 0 and 1 of SMBJSTCNT register for interrupt enable and transaction killing respectively)

The START bit in SMBHSTCNT register is set for the host controller to execute the transaction.

Note that the SMBus controller will not respond to the START bit being set unless all interrupt status bits in the SMBHSTSTS register have been cleared.

Upon completion of the transaction, the PIIX4 will generate an interrupt (either IRQ9 or SMI) if enabled. To recognize the completion of a SMBus host transaction, the system software can detect the interrupt or monitor the HOST_BUSY status bit in the SMBHSTSTS register.

Note:

The SMBHSTCNT, SMBHSTCMD, SMBHSTADD, SMBHSTDAT0, SMBHSTDAT1, and SMBBLKDAT registers should not be accessed after setting the START bit and the HOST_BUSY bit is being set to 1 (until after HOST_BUSY returns to 0)

E.8.3 PIIX4 SMBus Slave Interface—Interrupts and Resume Events

The SMBus slave interface provides three alternative mechanisms for other SMBus masters or slaves to communicate with the PIIX4; these mechanisms can generate interrupts (if the system is not suspended) or resume events (if the system is suspended). One mechanism is supported through the host controller slave port (for SMBus masters), one through slave shadow ports (for SMBus masters), and one through SMBALERT# signal (for SMBus slaves).

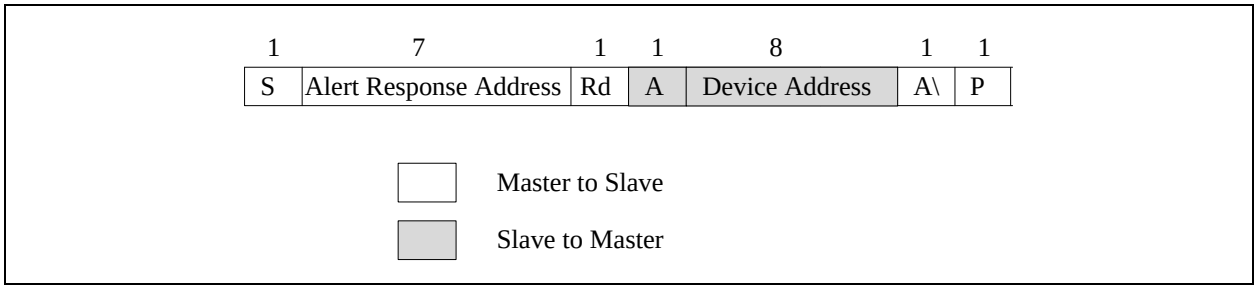
Table E-2 summarizes how the three mechanisms are implemented for external SMBus masters or slaves to generate interrupts or resume events.

Table E-2. Mechanisms for external SMBus masters to generate interrupts or resume events.

Mechanism	Description
Accesses to the SMBus controller host slave port at address 10h[1] (for external SMBus masters)	The host slave port responds to Word Write transactions only with the incoming data being stored in the SMBSLVDAT register and incoming command being stored SMBSHDCMD register. An interrupt or a resume event will be generated (if enabled by setting bit 0 of SMBSLVCNT register) if the incoming command matches the command stored in SMBSLVC register and at least one bit read into the SMBSLVDAT register matches with the corresponding bit in the SMBSLBEVT register.
Accesses to the SMBus slave shadow ports[2] (for external SMBus masters)	The slave shadow ports respond to Word Write transaction only with the incoming data being stored in the SMBSLVDAT register and incoming command being stored in the SMBSHDWCMD register. An interrupt or a resume event will be generated (if enabled by setting bit 1 or 2 of the SMBSLVCNT register) if an incoming address matches the corresponding shadow port's address in SMBSHDW1/SMBSHDW2 register.
Assertion of the SMBALERT# signal (for SMBus slaves)	An interrupt or a resume event will be generated (if enabled by setting bit 3 of the SMBSLVCNT register to 1) when SMBALERT# is asserted. To determine which device asserted the SMBALERT# signal, the PIIX4 host controller should be programmed to execute a read command using the Alert Respond Address[3].

NOTES:

1. This address is actually 0001 000 (7-bit address) appended with a read/write bit of 0, which indicates that the host controller slave interface only receives Write Word commands from external SMBus masters.
2. The addresses of the slave shadow ports are programmable and stored in SMBSHDW1 and SMBSHDW2 registers (function 3 PCI configuration registers).
3. SMBus Alert Response Address is 0001 100. Following is the protocol used for the host to identify the slave that wants to talk (only the device that pulled SMBALERT# low will acknowledge the Alert Response Address):



Note:

The SLV_BSY bit in the SMBSLVSTS register indicates that the PIIX4 slave interface is receiving an incoming message. The SMBSLVCNT, SMBSHDWCMD, SMBSLVEVT, SMBSLVDAT, and SMBSLVC registers should not be accessed while the SLV_BSY bit is active.

E.8.4 PIIX4 SMBus Frequency

The PIIX4 SMBus uses frequencies ranging from 10 KHz to 16 KHz to communicate with slave devices, as specified in the PIIX4 Electrical Timing Specification (PIIX4 ETS). On the other hand, the PIIX4 SMBus interface can sample incoming data from 10 KHz to 100 KHz.

E.8.5 PIIX4 SMBus Registers

The PIIX4 SMBus registers are split between function 3 PCI configuration registers and SMBus I/O space registers. Refer to Table E-3 for a list of PCI configuration registers (function 3) and Table E-4 for a list of SMBus I/O space registers. For a complete description of those registers, refer to the *82371AB (PIIX4) Data Sheet*.

Table E-3. PCI configuration Registers (function 3) for PIIX4 SMBus

Register name	Address offset	Access
SMBBA (SMBus Base Address)	90–93h	Read/Write
SMBHSTCFG (SMBus Host Configuration)	D2h	Read/Write
SMBSLVC (SMBus Slave Command)	D3h	Read/Write
SMBSHDW1 (SMBus Slave Shadow Port 1)	D4h	Read/Write
SMBSHDW2 (SMBus Slave Shadow Port 2)	D5h	Read/Write
SMBREV (SMBus Revision Identification)	D6h	Read only

Table E-4. SMBus I/O Space Registers (PIIX4 Function 3)

Register name	Address offset	Access
SMBHSTSTS (SMBus Host Status)	Base* + 0h	Read/Write
SMBSLVSTS (SMBus Slave Status)	Base + 01h	Read/Write
SMBHSTCNT (SMBus Host Control)	Base + 02h	Read/Write
SMBHSTCMD (SMBus Host Command)	Base + 03h	Read/Write
SMBHSTADD (SMBus Host Address)	Base + 04h	Read/Write
SMBHSTDAT0 (SMBus Host Data 0)	Base + 05h	Read/Write
SMBHSTDAT1 (SMBus Host Data 1)	Base + 06h	Read/Write
SMBBLKDAT (SMBus Block Data)	Base + 07h	Read/Write
SMBSLVCNT (SMBus Slave Control)	Base + 08h	Read/Write
SMBSHDWCMD (SMBus Shadow Command)	Base + 09h	Read only
SMBSLVEVT (SMBus Slave Event)	Base + 0Ah	Read/Write
SMBSLVDAT (SMBus Slave Data)	Base + 0Ch	Read only

* The base address is programmable via the SMBBA Register (PCI function 3)

E.9 Using I²C Devices with SMBus Interface

E.9.1 3V I²C devices communicating on SMBus

- *3V I²C device driving the SMBDATA line low:*
  An I²C output (at 3 mA sink current) has V_{OL} of 0.4V; the PIIX4 has a V_{IL} of 0.6V. This gives enough margin for PIIX4 to recognize the 0 written to it from an I²C device. In fast mode (at 6 mA sink current), an I²C device has V_{OL} of 0.6V, which theoretically may not give enough margin; however, the I_{pullup} current in an SMBus device is limited to 350 µA and therefore an I²C can write a 0 to a SMBus device.
- *3V I²C device driving the SMBDATA line high:*
  The maximum I_{pullup} in the SMBus of 350 µA limits the resistor pullup on the SMBDATA/SMBCLK lines to R=(3.6V- SMBus V_{OL}@350 µA)/(350 µA). If V_{OL} for 350 µA is 0.4V, the R_{pullup} is required to be larger than 9.2 kohm. The slave V_{OH} should be pulled up all the way to the V_{DD} level and should also meet the 1.4V minimum spec of SMB V_{IH}, and the rise time spec as well.
- *SMBus device writing low to a 3V I²C device:*
  Assuming that the I²C devices are specified with the V_{DD}-related inputs, the I²C devices will recognize levels as low if the levels are less than 0.9V (V_{IL}=0.3*3V=0.9V). The PIIX4 SMBus has V_{OL} max of 0.4V so I²C devices will recognize it as low.
- *SMBus device writing high to a 3V I²C device:*
  This is similar to when the I²C slave writes to the SMBus device. Assuming the pull-up resistor is properly sized for AC transitions and allows a full pull-up to the rail, the I²C device will see a high level if the input signal rises above 2.52V (V_{IH}=0.7*3.6V=2.52V).

In summary, 3V I²C devices can communicate with SMBus devices properly in terms of DC characteristics if the following is ensured: All 3V I²C devices input levels are V_{DD}-related (30% and 70% of V_{SS} for V_{IL} and V_{IH} respectively).

- The pull-up resistor is specified to meet the PIIX4 and I²C device V_{OL} levels.
- The pull-up resistor is specified to meet the rise time requirements and pulled to the V_{DD} rail in time to be recognized as a high level by both the PIIX4 and I²C devices.
- All input/output leakages are added to the above V_{OL}/V_{OH} calculations.

E.9.2 5V I²C devices communicating on SMBus

PIIX4 SMBus interface was designed for use with 3.3V devices; therefore 5V I²C devices cannot interface with the PIIX4 SMBus directly due to different voltage levels. When using 5V I²C devices to interface with the PIIX4 SMBus, there must be a circuit to convert voltage levels from 5V to 3.3V and visa versa. Figure E-4 shows an example of a circuit that can be used to translate voltage levels for a 5V I²C slave device and the PIIX4 SMBus to communicate with each other.

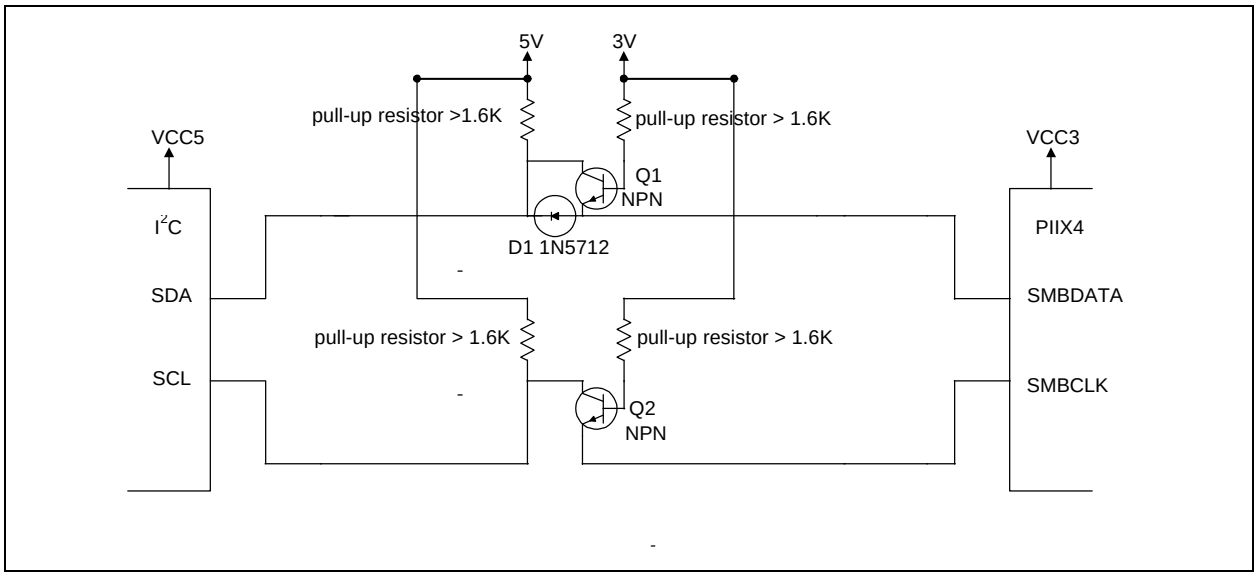


Figure E-4. Circuit used for 5V I²C slave device to interface with PIIX4's SMBus

As shown in Figure E-4, a 5V I²C slave device is connected to the left hand side of the circuit, and 3.3V SMBus device in the right. If the 5V device drives the SDA line low, it will pull the right side SMBDATA line low via D1. If the device on the right drives the SMBDATA line low, Q1 will be on, which pulls the left side SDA line low. Similarly, if the device on the right drives the SMBCLK line low, Q2 will be on, which pulls the left side SCL line low. By this way the voltage levels are translated for both devices to recognize correctly.

Also, as noted from Figure E-4, a diode is not used for the SCL line because the 5V I²C device is a slave (that means bi-directional communication is not required on the clock line). Note that if the 5V I²C device can be a master, the same circuit for SDA line should be used for the SCL line (the diode should be added).

E.9.3 PIIX4 SMBus Interface Connecting to I²C Bus

It is possible to connect the PIIX4 SMBus interface to an I²C bus operating at 100 kbit/s or lower because the PIIX4 SMBus interface was designed to operate at bit rates from 10 kbit/s to 100 kbit/s. The PIIX4 SMBus interface is not designed or tested to operate correctly at bit rates greater than 100 kbit/s; therefore, the PIIX4 interface may not function properly in systems running at bit rates greater than 100 kbit/s.

F

Single End Termination

APPENDIX F
SINGLE END TERMINATION

F.1 Intel 440LX Single Ended Termination Overview

The current design guidelines for the Intel 440LX program shows support for Dual Ended Termination (DET) on the Slot 1 system bus. This requires the placement of a complete set of GTL+ termination resistors on the motherboard for a uni-processor (single Slot 1 connector) design. The second set of termination resistors is located in the processor.

Intel is now also providing support for Single Ended Termination (SET) designs. Intel has performed system simulations which prove the ability of 440LX systems to support a SET design. This design will enable the removal of the GTL+ termination resistors from the motherboard.

This information is being provided to Intel customers in order for them to develop a Single Ended Termination design with the 440LX chip set.

F.2 Intel 440LX Single Ended Termination Design Guidelines

Design Guidelines:

- Total HCLK clock skew between PAC and slot 1 must be less than 200 ps (500 ps for dual-term).
- V_{TT} tolerance must be 1.5V ± 2% (± 10% for dual-term).
- The minimum GTL+ trace to trace spacing must be 15 mils (10 mils for dual-term).
- Motherboard trace impedance must be 70 ohms ± 10% (65 ohms ± 20% for dual-term). The design must maintain a motherboard trace velocity of 1.6 to 2.0 ns/ft (1.6 to 2.2 ns/ft for dual-term).
- Trace length from PAC to slot 1 is 0.75” min & 2.75” max (1.5” to 10” from slot 1 to term-resistor stub for dual-term).
- No change for trace width (5 mils).

G

Wake on LAN in a Pentium II/440LX System

APPENDIX G
WAKE ON LAN IN A PENTIUM II/440LX SYSTEM

G.1 Important Information and Disclaimers

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G.2 Scope

This document provides a reference for implementation of a WOL (Wake-On-LAN) header. This header is used to connect an add-in NIC (Network Interface Card) which has WOL capability to a motherboard. It is provided as a guideline only and is not intended to replace or supplement the user's independent design and validation activity. It includes information about the connector types, manufacturer's part numbers and pertinent signal information.

G.3 Overview

This document proposes the adoption of a standard header on both the motherboard and an add-in NIC card with WOL capability.

The proposed solution is to use identical 3-pin headers on both the motherboard and the NIC.

G.4 System Requirements

G.4.1 Motherboard

- 5-volt standby input routed to WOL header
- A 3-pin header to interconnect the NIC and the motherboard
- Support for the MP_Wakeup pulse to turn on the system
- BIOS support for boot-from-LAN (BIOS Boot Spec) if required

G.4.2 NIC

- WOL capability
- 3-pin header to match motherboard ***OR*** special "dongle" cable for NICs with 2 headers *(see Section G.7).*

G.4.3 Power Supply Unit

- 5VSB rated at least 600 ma

G.5 Wake-on-LAN Definition

Background: Wake-on-LAN is a key manageability feature for corporate systems. WOL is defined as the ability of a management application to remotely power up a computer which is powered off. See the IBM website URL in section G.9 for an excellent description of Wake-On-LAN functionality.

Wake-on-LAN: To support the WOL feature, a computer system must have the ability to detect a Magic Packet* via the LAN and turn on the computer. The most elegant solution is a motherboard which has implemented "LAN down" on the motherboard and includes WOL support. However, many motherboards will not include LAN down and/or WOL support and a method is desired to add that functionality via an add-in NIC which does support WOL. The purpose of this appendix is to define a standard header which can be used to interconnect the NIC and the motherboard in such a system.

G.6 Connectors and Cables

G.6.1 System Block Diagram

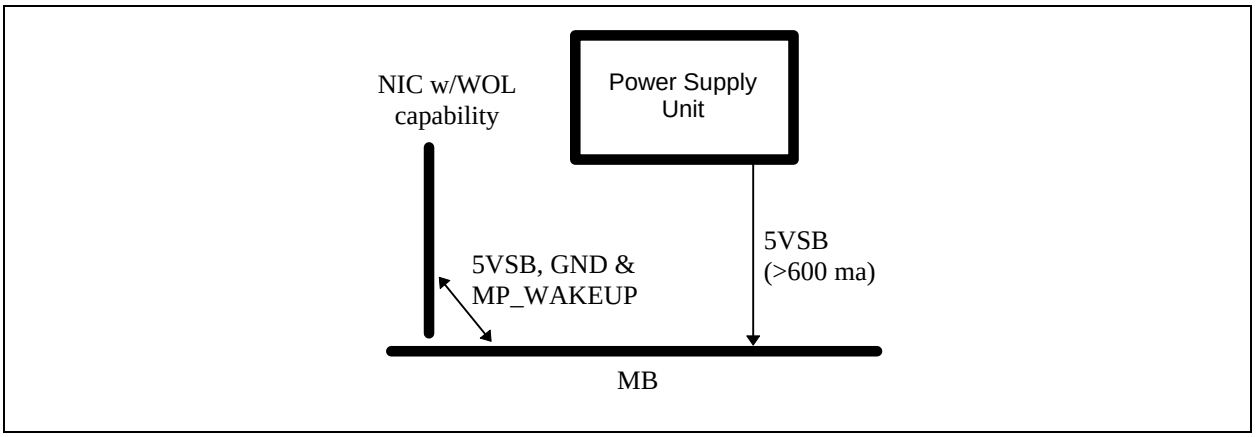


Figure G-1

G.6.2 Interconnect Cable and Components

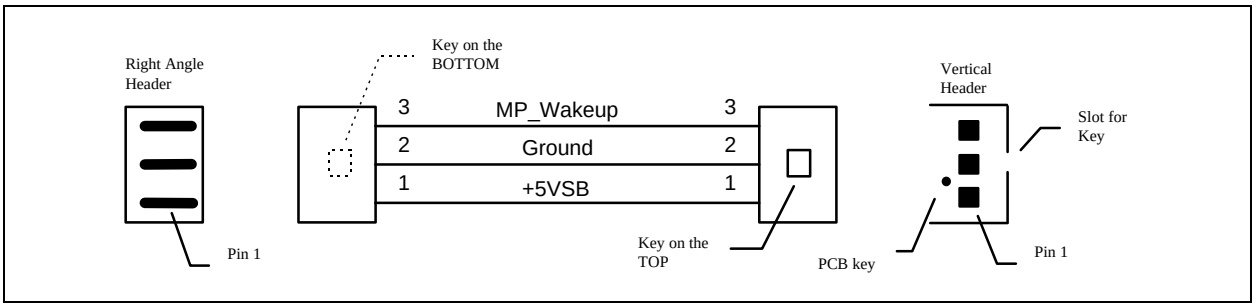


Figure G-2. 3-Pin Header

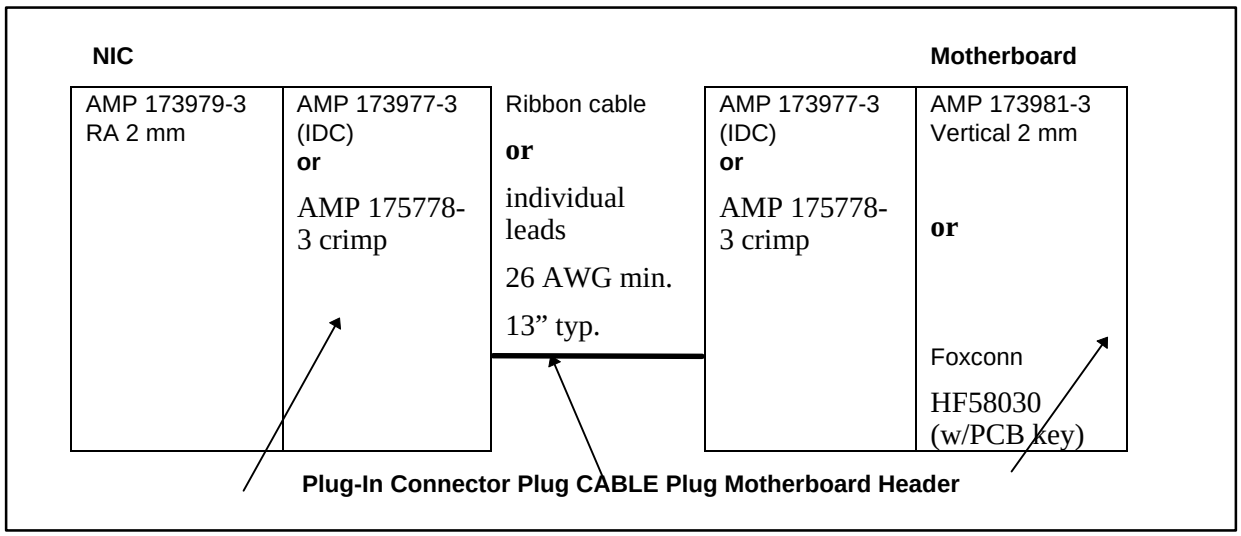


Figure G-3

The motherboard or NIC can use either vertical or right-angle header as desired. Interconnect cable can be oriented in either direction. Headers are friction-locking and shrouded (i.e., keyed).

Note:

Always refer to manufacturer’s WOL cabling documentation for specific cabling requirements.

G.6.3 PIIX4 Based System WOL Implementation

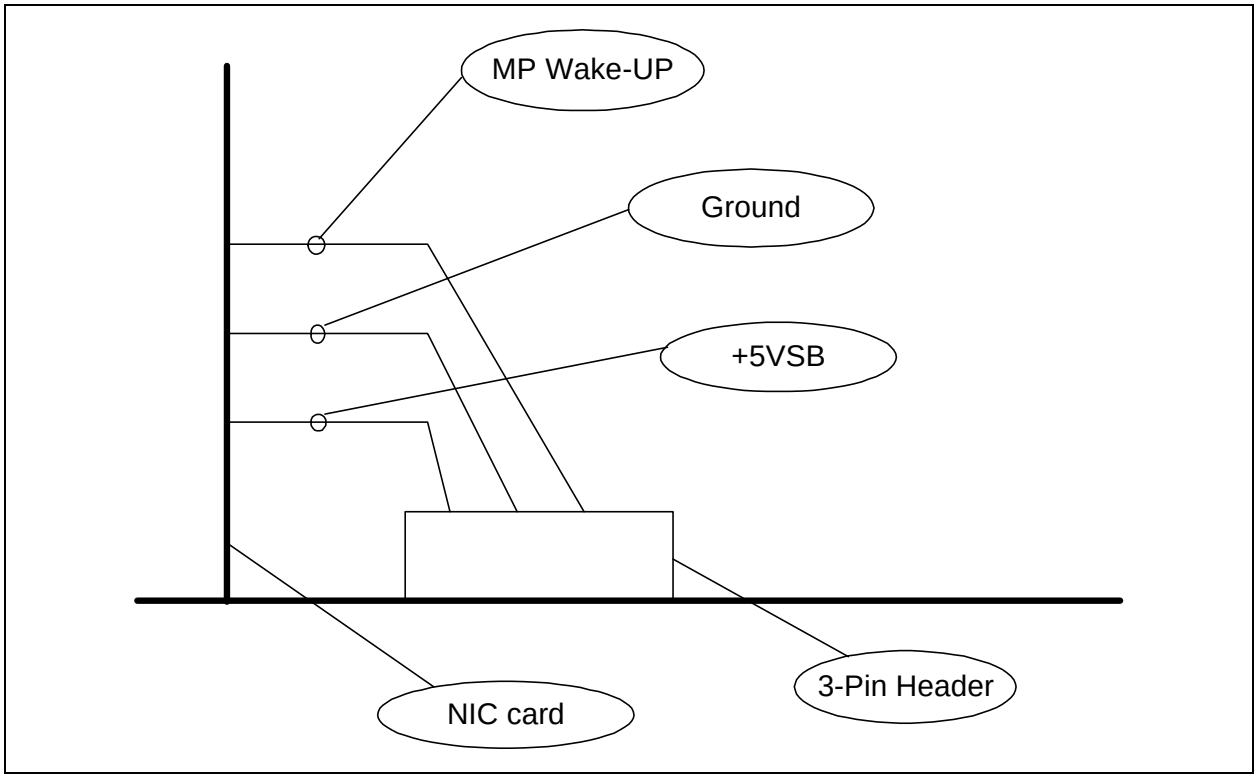


Figure G-4. Card and Board Header Interface

Figure G-4 demonstrates the connection of a 3 pin header to 5 volt standby (+5VSB), ground and MP_WAKEUP to the NIC. If the system is powered down then the PCI and ISA buses are powered down. This means that a LAN card on one of these buses will also be powered down. +5VSB gives the NIC enough power to recognize an incoming Magic Packet*. Once the packet is seen by the NIC then the MP_WAKEUP signal is asserted. This signal then can wake up the system using a GPIx or another signal in the suspend well of the PIIX4. Intel recommends the use of the PIIX4's LID signal. However LID is a 3.3V only signal. This means MP_WAKEUP must be dropped to 3.3 volts. Figure G-5 shows an example of a circuit that shifts signals to the proper voltage (e.g. 5V to 3.3 volts).

Note:

Usage of the LID signal must meet the following requirements:

- The LID/GPI10 bit is '0.' (Function 0 Address Offset B0h–B3h bit 25)
- The LID Enable bit is '1.' (Function 3 I/O Address Offset Base + 0Eh bit 11)
- The LID Polarity bit is '0.' (Function 3 I/O Address Offset Base + 28h bit 25)
- The wake-up signal pulse must be at least 16 ms.

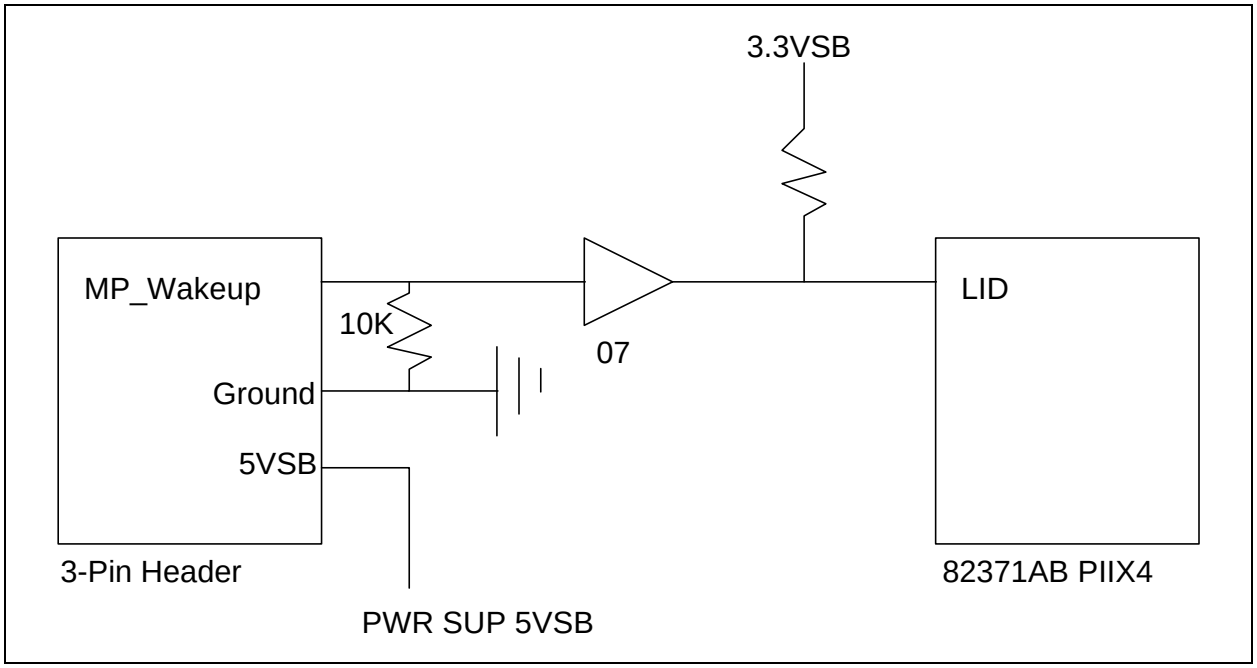


Figure G-5. Example connection of MP_WAKEUP to PIIX4.

G.7 Electrical Characteristics

The WOL input signal from an external or internal source may be from one of several different devices including Ethernet, Token Ring, etc. This signal may be from various logic families or transistor types. This specification delineates the acceptable parameters for this device as well as the input characteristics required (V_{IH}, V_{IL} for the host motherboard) device to fully define what pull-downs, impedances and current load maximums may be.

AC Electrical Characteristics for Devices Driving the WOL Signals			
Parameter	**Symbol**	**Min**	**Max**
Low-Level Output Voltage	V_{OL}		0.8V
High-Level Output Voltage	V_{OH}	2.6V @ 0.5 mA	
Output Transition Time	t_{TLH} & t_{THL}	0 nS	50 nS

G.8 Notes

Adding a WOL NIC is not an end-user activity unless the system has been configured for it by the OEM. This is because of the higher 5VSB current requirements of the PSU, the need for the MB design to support the wake-up signal, and possible BIOS enhancements required to support WOL (alternate boot sequence).

Existing NICs (with 2 connectors) could be used with the header defined in this document but a custom cable ("dongle") would be required between the single MB header and the current NIC headers. See Figure G-1 for example.

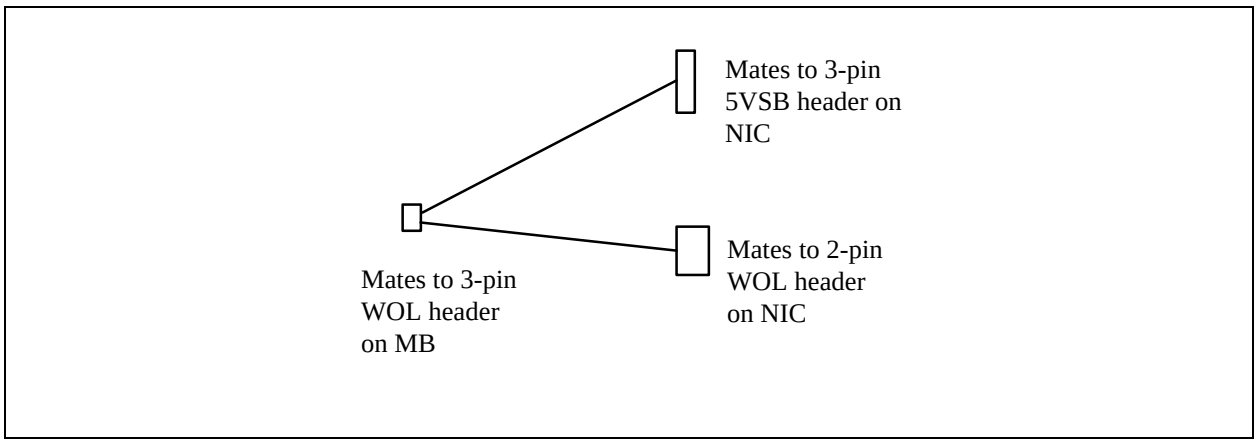


Figure G-6

G.9 Related Documents

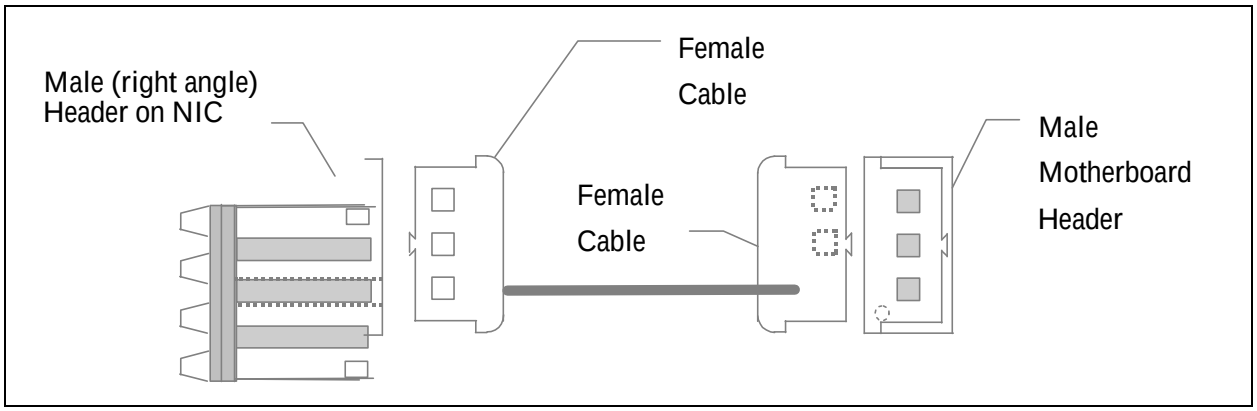
http://www.pc.ibm.com/infobrf/iblan.html (IBM Wake-On-LAN Information Brief)

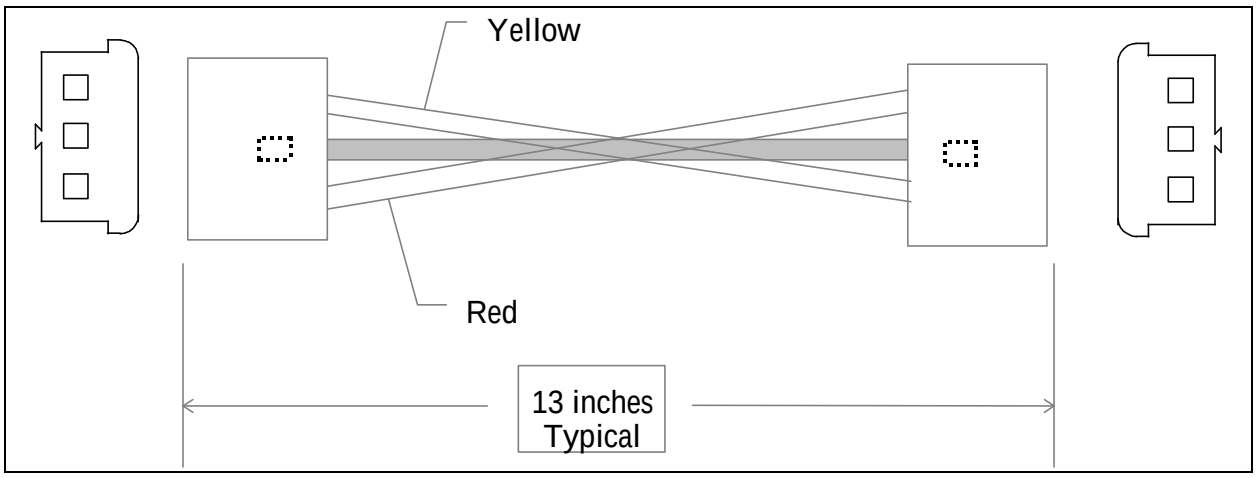
http://www.amd.com/html/products/ind/overview/20212d.html (AMD Magic Packet explanation and proposed AMD implementation of WOL header, to be updated to correlate with this specification)

http://www.intel.com/managedpc/ (Intel Managed PC web site)

http://www.amp.com (search by part number for connector specs)

G.10 Detailed Header and Cabling Harness Illustrations





Pin 1 = 5 Volt Standby (RED)

Pin 2 = Ground (BLACK)

Pin 3 = MP_Wakeup (YELLOW)

H

Thermal Design Considerations

APPENDIX H
THERMAL DESIGN CONSIDERATIONS

H.1 Introduction

In a system environment, the chip set temperature is a function of both the system and component thermal characteristics. The system level thermal constraints consist of the local ambient temperature at the chip set, the airflow over the chip set and surrounding board as well as the physical constraints at, above, and surrounding the chip set. The chip set case temperature depends on the component power dissipation, size, and packaging materials (effective thermal conductivity), the type of interconnection to the substrate and motherboard, the presence of a thermal cooling solution, the thermal conductivity and the power density of the substrate, nearby components, and motherboard.

All of these parameters are pushed by the continued trend of technology to increase performance levels (higher operating speeds, MHz) and packaging density (more transistors). As operating frequencies increase and packaging size decreases, the power density increases and the thermal cooling solution space and airflow become more constrained. The result is an increased emphasis on system design to ensure that thermal design requirements are met for each component in the system.

H.1.1 Document Goals

The 82443LX is the newest addition to Intel's line of Pentium II processor chip sets. Previous generations of chip sets generated insufficient heat to require an enhanced cooling solution in order to meet the case temperature specifications in system designs. As chip sets transition to higher-speeds with enhanced features, the heat generated by the chip set will introduce new thermal challenges for system designers. Depending on the type of system and the chassis characteristics, new designs may be required to provide better cooling solutions for the chip set. The goal of this document is to provide an understanding of the thermal characteristics of the 82443LX and discuss guidelines for meeting the thermal requirements imposed on systems.

H.2 Importance of Thermal Management

The objective of thermal management is to ensure that the temperature of all components in a system are maintained within functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet specified performance requirements. Operation outside the functional limit can degrade system performance, cause logic errors or cause component and/or system damage. Temperatures exceeding the maximum operating limits may result in irreversible changes in the operating characteristics of the component.

H.3 82443LX Packaging Terminology

BGA: Ball Grid Array. A package type defined by a resin-fiber substrate on to which a die is mounted, bonded and encapsulated in molding compound. The primary electrical interface is an array of solder balls attached to the substrate opposite the die and molding compound.

Mold-Cap: The black encapsulating molding compound. The top of this is where maximum case temperatures are taken and where heat sinks are attached.

Thermal Balls: Typically this refers to an array of balls in the center of the larger array of balls which serve to channel heat into the motherboard as well as ground connections.

H.4 Thermal Specifications

The 82443LX power dissipation can be found in the Intel 440LX AGPset: 82443LX PCI AGP Controller (PAC) Data sheet order #290564. Please refer to these documents to verify the actual thermal specifications for the 82443LX. In general, systems should be designed to dissipate the highest possible thermal power.

To ensure proper operation and reliability of the 82443LX, the thermal solution must maintain the case temperature at or below its specified value (Table I-1). Considering the power dissipation levels and typical system ambient environments of 45°C to 55°C, if the 82443LX case temperature exceeds the maximum case temperature listed in Table I-1, system or component level thermal enhancements will be required to dissipate the heat generated.

The thermal characterization data described in later sections illustrates that good system airflow is critical. In typical systems the thermal solution is limited by board layout, spacing and component placement. Airflow is determined by the size and number of fans and vents along with their placement in relation to the components and the airflow channels within the system. In addition, acoustic noise constraints may limit the size and/or types of fans and vents that can be used in a particular design.

To develop a reliable, cost-effective thermal solution, all of the above variables must be considered. Thermal characterization and simulation should be carried out at the entire system level accounting for the thermal requirements of each component.

Table I-1: 82443LX Thermal Absolute Maximum Rating:

Parameter	Maximum
T_{case}	100°C
$T_{case\text{-}hs}$ *	90°C

* $T_{case\text{-}hs}$ is defined as the maximum case temperature with clad-copper thin heat sink (see section I.6.2.2).

H.4.1 Case Temperature

The case temperature is a function of the local ambient temperature and the internal temperature of the 82443LX. As a local ambient temperature is not specified for the 82443LX, the only restriction is that the maximum case temperature (T_{case}) is not exceeded. Section I.7.1 discusses proper guidelines for measuring the case temperature. Note that increasing the heat flow through the case increases the difference in temperature between the junction and case, reducing the maximum allowable case temperature. For clad-copper thin heat sinks the adjusted value is listed in Table I-1.

H.4.2 Power

In previous generations of chip sets where Quad Flat Pack (QFP) packages have been the primary package type, the majority of power dissipation has been through the plastic case of the package into the surrounding air. With the advent of Ball Grid Array (BGA) packaging for chip sets, the majority of the thermal power dissipated by the chip set typically flows into the motherboard to which it is mounted. The remaining thermal power is dissipated by the package itself.

The amount of thermal power dissipated either into board or by the package varies depending on how well the motherboard conducts heat away from the package and whether the package uses thermal enhancements. While package thermal enhancements typically serve to improve heat flow through the case via a heat sink, how well the motherboard conducts heat away from the package is strictly a function of motherboard design:

- How well the thermal balls are connected to the inner planes of the motherboard (do not use thermal reliefs).
- How well the inner planes conduct heat away from the package.
- The size of the motherboard and number of layers.

All should be taken into account by system designers when developing new systems.

H.5 Designing for Thermal Performance

In designing for thermal performance, the goal is to keep the component within the operational thermal specifications. The heat generated by the components within the chassis must be removed to provide an adequate operating environment for all of the system components. To do so requires moving air through the chassis to transport the heat generated out of the chassis.

H.5.1 Airflow Management

It is important to manage the airflow path and amount of air that flows through the system to maximize the amount of air that will flow over the 82443LX area. System airflow can be increased by adding one or more fans to the system, by vents and fans in combination, by increasing the output (faster speed) or size of an existing system's fan(s). Local airflow can also be increased by managing the local flow direction using baffles or ducts. An important consideration in airflow management is the temperature of the air flowing over the chip set area. Heating effects from add-in boards, memory, other processors and disk drives greatly reduce the cooling efficiency of this air, as does re-circulation of warm interior air. Care must be taken to minimize the heating effects of other system components and to eliminate excessive warm air re-circulation.

For example, a clear air path from the external system vents to the system fan(s) will enable the warm air from the 82443LX to be efficiently removed from the system. If no air path exists across the 82443LX, the warm air ambient to the 82443LX will not be removed from the system, resulting in localized heating ("hot spots") at and around the chip set requiring the addition of a thermal cooling device. Figure I-1 shows two examples of air exchange through a PC style chassis. The system on the left is an example of good air exchange incorporating both the power supply fan, an additional system fan and good venting. The system on the right shows a system with only a power supply fan (blowing into the box) and minimal venting resulting in poor airflow.

Re-circulation of internal warm air is most common between the system fan and chassis and between the system fan intake and the drive bays behind the front bezel. These paths may be eliminated by mounting the fan flush to the chassis, thereby obstructing the flow between the drive bays and fan inlet, and by providing generous intake vents in both the chassis and the front bezel.

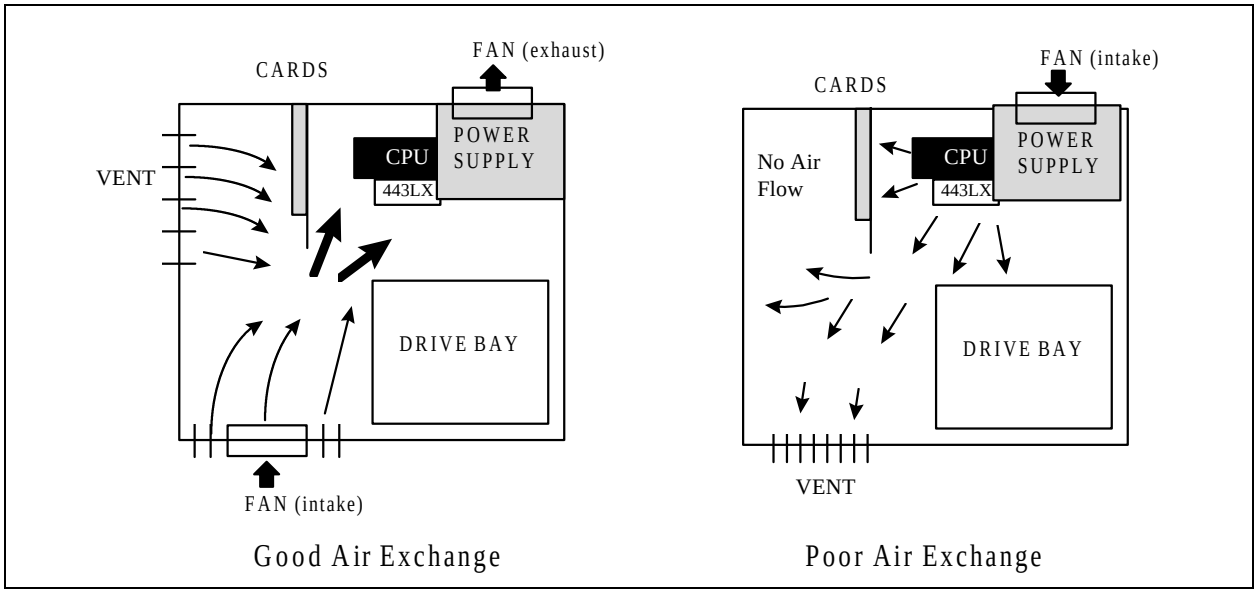


Figure I-1. Example of air exchange through a PC chassis

H.6 Cooling Solutions

Numerous alternatives for cooling solutions exist for the 82443LX. This section will explore system cooling solutions as well as package heat sinks. Due to their varying attributes, each of these solutions may be appropriate for a particular system implementation.

H.6.1 System Fans

Fans are needed to move the air through the chassis. The airflow rate of a fan is a function of the system's impedance to airflow and the capability of the fan itself. Maximum acceptable noise levels may limit the fan output or the number of fans selected for a system. It is appropriate at this time to reiterate section I.4.2. The majority of the thermal power dissipated by the 82443LX typically flows into the motherboard to which it is mounted. Cooling the motherboard will cool the component by increasing the efficiency of heat transfer from the device to the motherboard.

H.6.1.1 Fan Placement

Proper placement of the fans can ensure that the 82443LX is properly cooled. Because of the difficulty in building, measuring and modifying a mechanical assembly, models are typically developed and used to simulate a proposed prototype for thermal effectiveness to determine the optimum location for fans and vents within a chassis. Prototype assemblies can also be built and tested to verify if thermal specifications for the system components are met.

An air fan is typically in the power supply exhausting air through the power supply vents. A second system fan is added to improve airflow to the chip set and other system components. Figure I-2 and Figure I-3 show recommended fan placements for an ATX form factor layout and a NLX form factor, respectively.

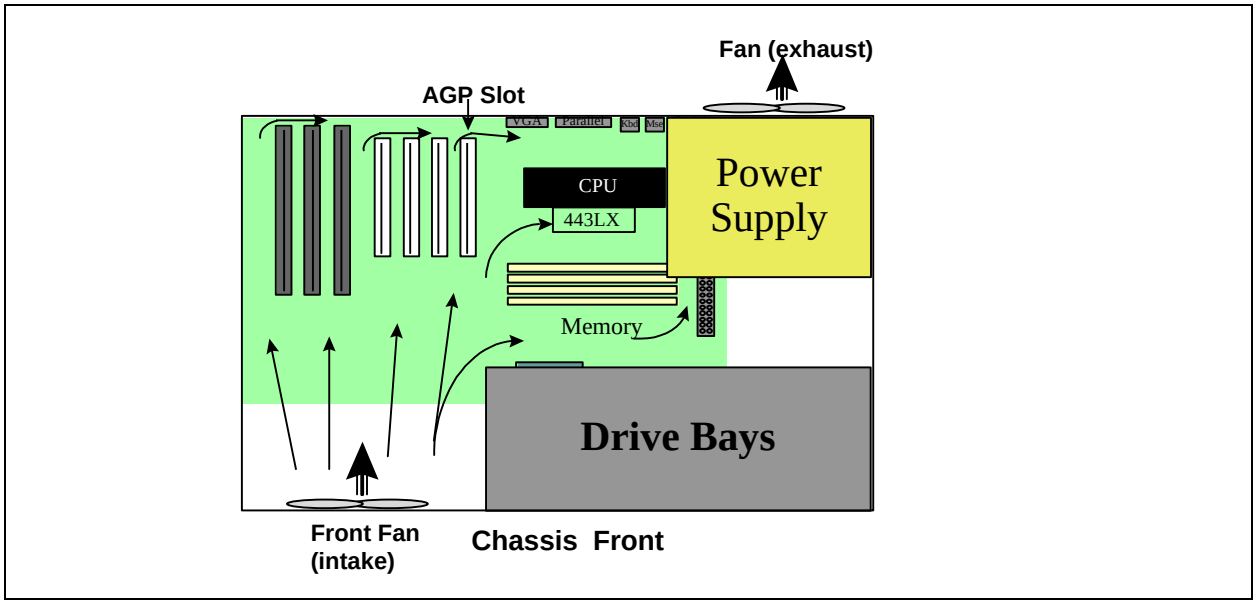


Figure I-2. Fan Placement and Layout of an ATX Form Factor Chassis—Top View

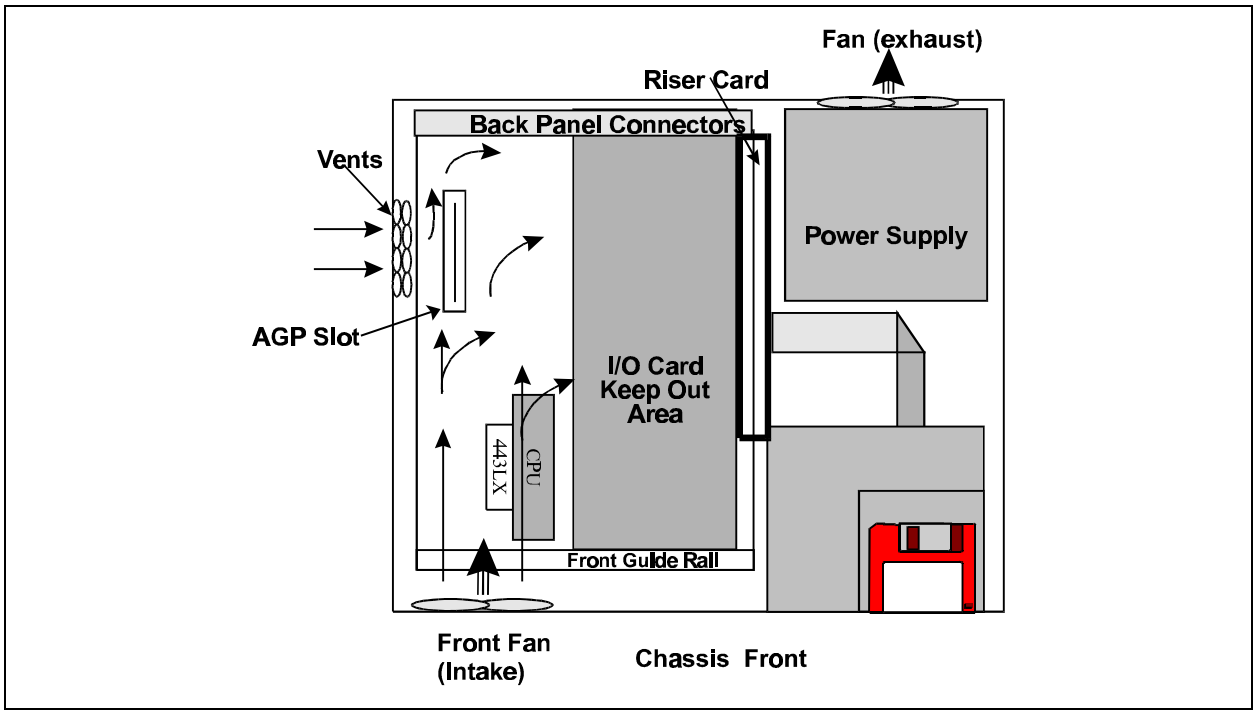


Figure I-3. Fan Placement and Layout of an NLX Form Factor Chassis—Top View

H.6.1.2 Fan Direction

If the fan(s) are not moving air across the 82443LX then little cooling can occur. Hence the 82443LX may exceed its absolute maximum thermal ratings. Note the recommended fan airflow directions in figures I-2 and I-3.

The direction of the airflow can also be modified with baffles or ducts to direct the airflow over the 82443LX. This will increase the local flow over the device and may eliminate the need for a larger or higher speed fan.

H.6.1.3 Size and Quantity

A larger fan does not always increase cooling efficiency: A small blower using ducting might direct more air over the 82443LX than a larger fan blowing non-directed air. The following provides some guidelines for size and quantity of the fans.

The fan should be a minimum of 80 mm (3.150”) square, with a minimum airflow of approximately 40 CFM (cubic feet per minute), or approximately 400 LFM (linear feet per minute). As shown in figures I-2 and I-3, two (2) fans should be used. The intake air fan blows cooler external air into the chassis, while a second fan (most likely in the power supply) would exhaust the air out of the system.

H.6.1.4 Fan Venting

As shown in figures I-2 and I-3, intake venting should be placed at the front (user side) of the system. Location should take into consideration cooling of the microprocessor and peripherals as well as the 82443LX. A good starting point would be the lower 50% of the Front Panel (Bezel). Intake venting directly in front of the intake fan is the most optimal location.

H.6.1.4.1 Vent Placement

In most cases, exhaust venting in conjunction with an exhaust fan in the power supply is sufficient. However, depending on the number, location and types of add-in cards, exhaust venting may be necessary near the cards as well. This should be modeled or prototyped for the optimum thermal potential. Hence a system should be modeled for the worst case, i.e., all expansion slots should be occupied with typical add-in options.

H.6.1.4.2 Vent Area/Size

The area and/or size of the intake vents should consider the size and shape of the fan(s). Adequate air volume must be obtained and this will require appropriately sized vents. Intake vents should be located in front of the intake fan(s) and adjacent to the drive bays. Venting should be approximately 50% to 60% open in the EMI containment area due to EMI constraints. Outside the EMI containment area, the open percentage can be greater if needed for aesthetic appeal (i.e. bezel/cosmetics). For more information concerning EMI constraints and Pentium II processor based system design, see the *Pentium II Processor EMI Design Guidelines Application Note*.

H.6.1.4.3 Vent Shape

Round, staggered pattern openings are best for EMI containment, acoustics and airflow balance. For material related to EMI considerations please see *Pentium II Processor EMI Design Guidelines Application Note*.

H.6.1.5 Ducting

Ducts can be designed to isolate components from the effects of system heating and to maximize the thermal budget. Air provided by a fan or blower could be channeled directly over the 82443LX or split into multiple paths to cool multiple components.

H.6.1.5.1 Ducting Placement

When ducting is to be used, it should direct the airflow evenly from the fan across the entire component and surrounding motherboard. The ducting should be accomplished, if possible, with smooth, gradual turns as this will enhance the airflow characteristics. Sharp turns in ducting should be avoided. Sharp turns increase friction and drag and will greatly reduce the volume of air reaching the 82443LX.

H.6.2 Thermal Enhancements

One method used to improve thermal performance is to increase the surface area of the device by attaching a metallic heat sink to the mold cap. To maximize the heat transfer, the thermal resistance from the heat sink to the air can be reduced by maximizing the surface area of the heat sink itself.

Note:

Increasing the heat flow through the case increases the difference in temperature between the junction and case, reducing the maximum allowable case temperature. For clad-copper thin heat sinks the adjusted value is listed in Table I-1.

H.6.2.1 Clearance

Though each design may have unique mechanical volume and height restrictions or implementation requirements, the constraints typically placed on the 82443LX by the Single Edge Card Connector (SECC) heat sink allows 0.375” clearance between the 82443LX mold cap and the bottom of the SECC heat sink.

H.6.2.2 Clad-Copper Thin Heat Sink

A simple and economical thermal enhancement is the clad-copper thin heat sink. It is typically insulated copper, roughly 0.010” total thickness covered with an electrically non-conductive coating and varying in area from 1 in^2 to 6 in^2. It is mounted using an integral pressure sensitive adhesive (PSA) and shown in Figure I-4.

Clad-copper heat sinks are available from multiple suppliers and depending on size, cost in 50K quantities are typically in the $0.20–$0.50 range.

Suppliers, Part Numbers and Sales Office Locations are listed in section I-9.

H.6.2.3 Clad-Copper Thin Heat Sink Attach

To properly attach the Clad-Copper Thin Heat Sink, the general guidelines below should be followed. For more specific information, contact your heat sink supplier.

The required materials are:

Clean Cotton Cloth

Isopropyl Alcohol

Rubber Gloves

The following steps are recommended:

Step 1: Clean the top surface of the mold cap with the cotton cloth.

Step 2: Wipe the surface of the mold cap with isopropyl alcohol and allow to dry.

Note: Do not touch the mold cap after cleaning! If this occurs, repeat steps 1 and 2.

Step 3: Remove the clear, PSA protective cover, exposing the PSA. Avoid touching the adhesive surface with your fingers.

Step 4: Center the exposed PSA on the mold cap. Press and smooth the entire bonding area with firm finger pressure (about 5 psi for 5 seconds).

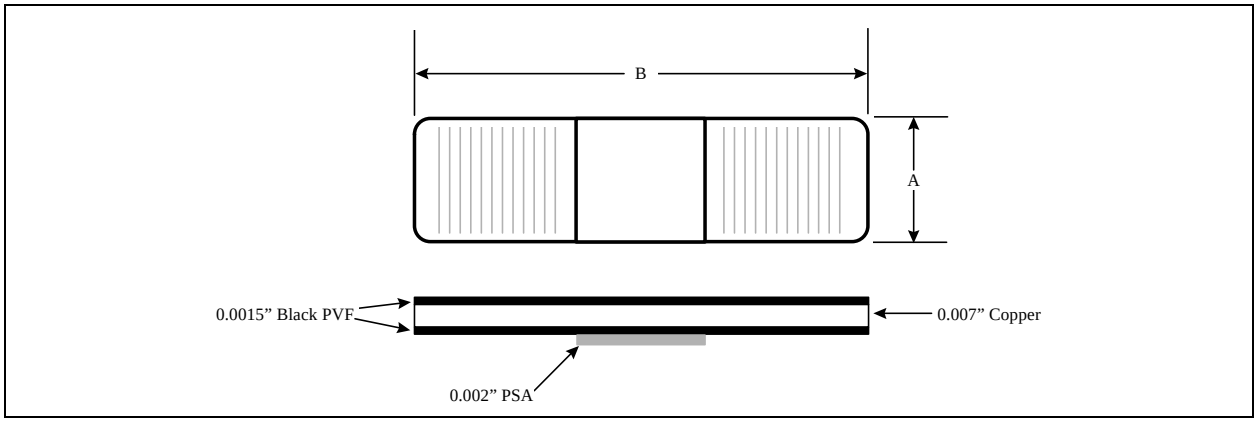


Figure I-4. Clad-Copper Thin Heat Sink

H.6.2.4 Other Thermal Enhancements

While other thermal enhancements may be implemented by the customer given the clearance constraints of the device, some general recommendations are:

If a clip must be used, DO NOT clip a heat sink to the 82443LX substrate as damage to the component is very likely (this applies to any PBGA). If a clip must be used, the recommended attachment method is to clip the heat sink to the motherboard.

Exercise caution when epoxying or otherwise permanently attaching a heat sink exceeding 10 gms in weight and 5 mm in height to the mold cap. The additional weight and change in center of gravity may negatively effect the long-term reliability of the solder joint during mechanical stress.

H.6.3 Thermal Interface Management for Heat Sink Solutions

For solutions where a heat sink is preferred, to optimize the heat sink design for 82443LX, it is important to understand the impact of factors related to the interface between the mold-cap and the heat sink base. Specifically, the bond line thickness, interface material area and interface material thermal conductivity should be managed to realize the most effective heat sink solution.

H.6.3.1 Bond Line Management

The gap between the mold-cap and the heat sink base will impact heat sink solution performance. The larger the gap between the two surfaces, the greater the thermal resistance. The thickness of the gap is determined by the flatness of both the heat sink base and the mold-cap, plus the thickness of the thermal interface material (e.g., PSA, thermal grease) used between these two surfaces.

H.6.3.2 Interface Material Performance

Two factors impact the performance of the interface material between the thermal plate and the heat sink base:

- Thermal resistance of the material
- Wetting/filling characteristics of the material

Thermal resistance is a description of the ability of the thermal interface material to transfer heat from one surface to another. The higher the thermal resistance, the less efficient an interface is at transferring heat. The thermal resistance of the interface material has a significant impact on the thermal performance of the overall thermal solution. The higher the thermal resistance, the higher the temperature drop across the interface and the more efficient the thermal solution must be.

The wetting/filling of the thermal interface material is its ability to fill the gap between the case and the heat sink. Since air is an extremely poor thermal conductor, the more completely the interface material fills the gaps, the lower the temperature drop across the interface.

H.7 Measurements for Thermal Specifications

To appropriately determine the thermal properties of the system, measurements must be made. Guidelines have been established for the proper techniques to be used when measuring the 82443LX case temperatures. Section I.7.1 provides guidelines on how to accurately measure the case temperature of the 82443LX. Section I.7.2 contains information on running an application program LXPOWER.EXE which will emulate anticipated maximum thermal design power. The flowchart in Figure I-7 and heat sink selection guide (Table I-2) describe the guidelines for measurement and implementation.

H.7.1 Case Temperature Measurements

To ensure functionality and reliability, the 82443LX is specified for proper operation when T_{case} (case temperature) is maintained at or below the maximum case temperatures listed in Table I-1. The surface temperature of the case directly above the center of the package is measured. Special care is required when measuring the T_{case} temperature to ensure an accurate temperature measurement.

Thermocouples are often used to measure T_{case}. Before any temperature measurements are made, the thermocouples must be calibrated.

When measuring the temperature of a surface which is at a different temperature from the surrounding local ambient air, errors could be introduced in the measurements. The measurement errors could be due to having a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation, convection, by conduction through thermocouple leads, or by contact between the thermocouple cement and the heat sink base for those solutions which implement a heat sink. To minimize these measurement errors, the following approach is recommended:

Attaching the Thermocouple

- Use 36 gauge or smaller diameter K type thermocouples.
- Ensure that the thermocouple has been properly calibrated.
- Attach the thermocouple bead or junction to the top surface of the package (case) in the center of the mold-cap using high thermal conductivity cements.
- The thermocouple should be attached at a 0° angle if there is no interference with the thermocouple attach location or leads (refer to Figure I-5). This is the preferred method and is recommended for use with both unenhanced packages as well as packages employing Clad-Copper Thin Heat Sinks.

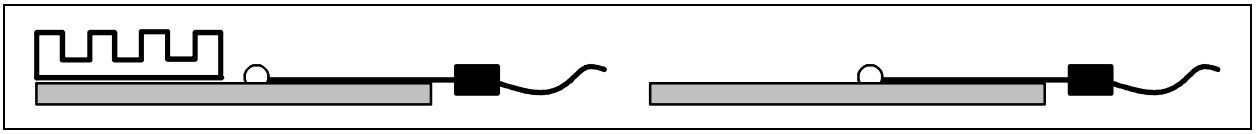


Figure I-5. Technique for Measuring T_{case} with 0° Angle Attachment

- For solutions where a heat sink is preferred, the thermocouple should be attached at a 90° angle if a heat sink is attached to the case and the heat sink covers the location specified for T_{case} measurement (refer to Figure I-6).
- The hole size through the heat sink base to route the thermocouple wires out should be smaller than 0.150” in diameter.
- Make sure there is no contact between the thermocouple cement and heat sink base. This contact will affect the thermocouple reading.

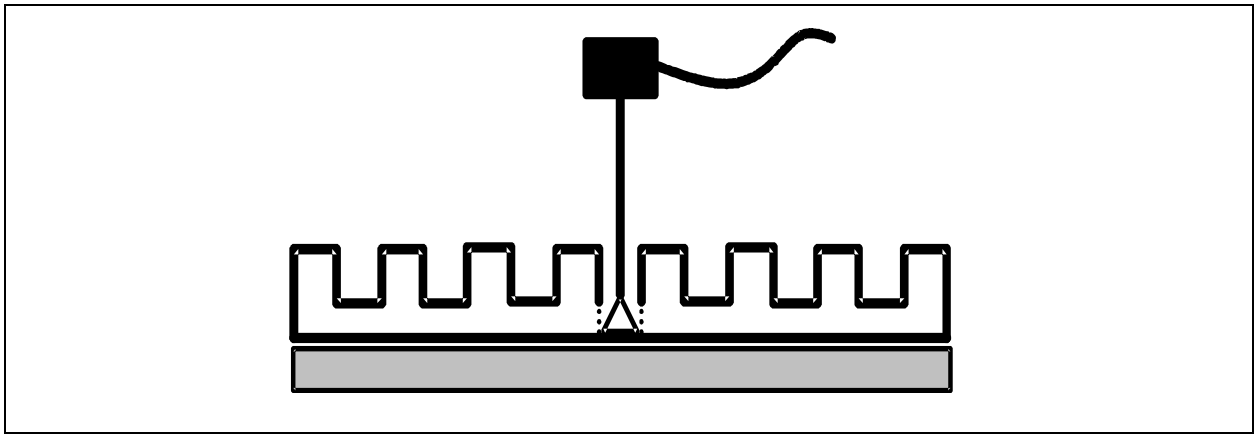


Figure I-6. Technique for Measuring T_{case} with 90° Angle Attachment

H.7.2 LXPOWER Simulation Program

H.7.2.1 Overview

LXPOWER is a utility designed to stress the thermal design power for an Intel 82443LX PCI A.G.P. Controller (PAC) when used in conjunction with a Pentium II processor. The combination of the Pentium II processor along with the high bandwidth capability of the 82443LX PAC enables new levels of system performance which are not utilized in most current software applications. However, it is conceivable that new applications will be written which take advantage of this increased bandwidth. To ensure the thermal performance of the 82443LX PAC while running this type of high bandwidth application, Intel has developed a software utility which emulates this anticipated power dissipation. See your Intel Field Representative for information on LXPOWER.

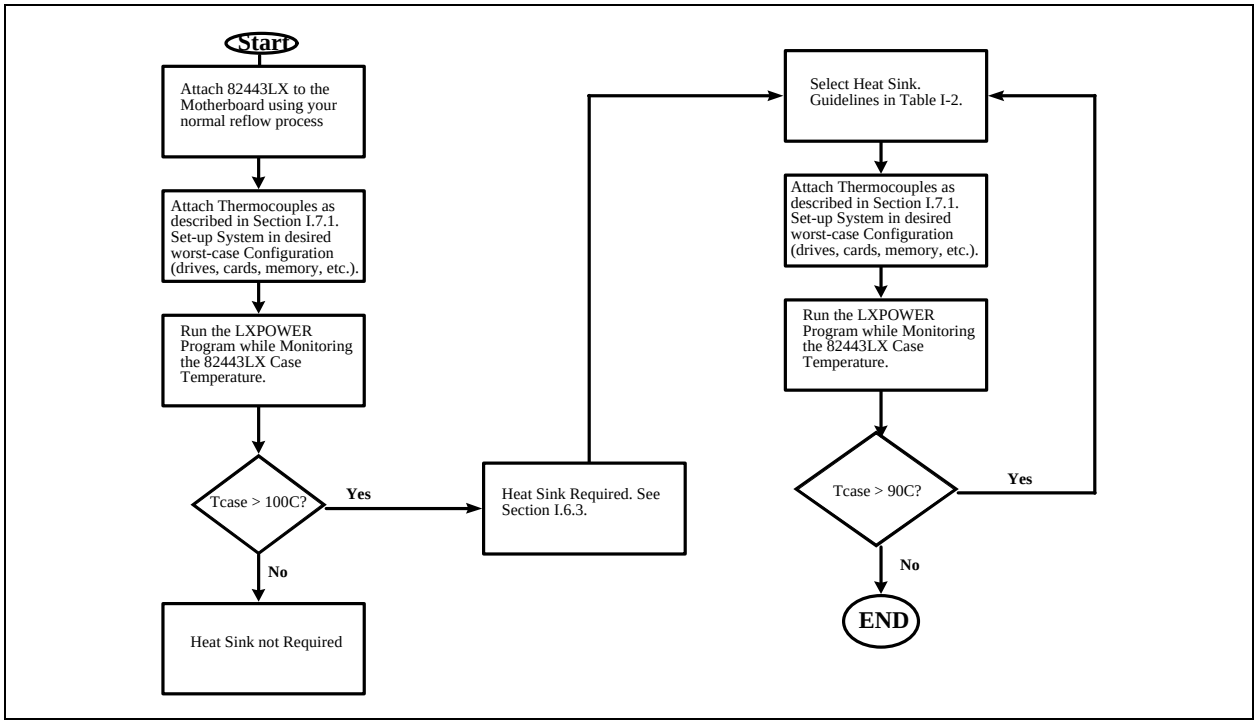


Figure I-7. Thermal Enhancement Decision Flowchart

Table I-2. Clad-Copper Thin Heat Sink Selection Guide

Clad-Copper Heat Sink Size			
T_{case} No Heat Sink	1 in x 1 in	1 in x 2 in	1 in x 3 in
100–110C	OK	OK	OK
111–115C		OK	OK
116–120C			OK

H.8 Conclusion

As the complexity of today's chip sets continues to increase, so do the power dissipation requirements. Care must be taken to ensure that the additional power is properly dissipated. Heat can be dissipated using improved system cooling, selective use of ducting and/or passive heat sinks.

The simplest and most cost-effective method is to improve the inherent system cooling characteristics through careful design and placement of fans and ducts. When additional cooling is required, use a clad-copper heat sink in conjunction with enhanced system cooling. The size of the heat sink can be varied to balance size and space constraints with acoustic noise. This document has presented the conditions and requirements for properly designing a cooling solution, a system implementing the 82443LX. Properly designed solutions provide adequate cooling to maintain the 82443LX case temperature at or below those listed in Table I-1. This is accomplished by providing a low local ambient temperature and creating a minimal thermal resistance to that local ambient temperature. By maintaining the 82443LX case temperature at or below those recommended in this document, a system will function properly and reliably.

H.9 Heat Sink Vendors

Sales Locations

For Chomerics, please go to: http://www.chomerics.com.

For AAVID, please go to: http://www.aavid.com.

Part Numbers

Chomerics: 1 in. x 1 in. with Full PSA: 69-12-21326-TW10

1 in. x 2 in. with Full PSA: 69-12-21325-TW10

1 in. x 3 in. with 1 in. PSA: 69-12-21323-TW10

1 in. x 3 in. with full PSA: 69-12-21324-TW10

AAVID: 0.5 in. x 2 in. with 0.5 in. PSA: 341600B00000

0.5 in. x 3 in. with 0.5 in. PSA: 341700B00000

0.75 in. x 3 in. with 0.75 in. PSA: 341800B00000

1 in. x 3 in. with 1 in. PSA: 341900F00000

H.10 Reference Documents And Information Sources

Document Name or Information Source	Available From
Intel 440LX AGPset: 82443LX PCI AGP Controller (PAC) Data sheet	Intel—order number 290564
Pentium® II Processor Thermal Design Guidelines. Application Note (order number 243331-001)	Intel—order number 243331
Pentium® II Processor EMI Design Guidelines Application Note	Intel—order number 243334
EIA/JESD51-1 Integrated Circuit Thermal Measurement Method-Electrical Test Method	
EIAJESD51-2 Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)	

I

Intel Pentium II/ 440LX Schematics

APPENDIX I
INTEL PENTIUM II/440LX SCHEMATICS

I.1 Uni-Processor Systems

I.2 Dual-Processor System