

# Intel<sup>®</sup> 440EX AGPset

**Design Guide** 

August 1998

Order Number: 290637-002



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# **Revision History**

Date of Revision	Revision	Description
April 1998	001	Initial Release
August 1998	002	Reclassified registers from "Reserved/Default" to allow easier migration from Intel® 440LX AGPset to Intel® 440EX AGPset. Added strapping requirement for Memory Configuration #2.



# Introduction

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This information is being provided to Intel customers designing with the Intel<sup>®</sup> 440EX AGPset. The Intel<sup>®</sup> 440EX AGPset is a Basic PC solution for the Pentium<sup>®</sup> II processor platform.

The guidelines in this document are provided in conjunction with the *Intel*<sup>®</sup> 440LX AGPset Design Guide and Design Guide Update. The documents should be followed in all areas except those listed in this document.

The 82443EX is a full featured 82443LX with the following exceptions:

- 1.0.1 Maximum of 2 DIMM sockets
- 1.0.2 Maximum of 3 PCI slots (4-PCI masters including PIIX4)
- 1.0.3 NO ECC
- 1.0.4 Single processor with no support for IOAPIC
- 1.0.5 Nand Tree Test Mode not supported

## 1.1 Reference Documents

- Intel® 440EX AGPset datasheet (www: order number 290616)
- Intel® 440LX AGPset Design Guide and Design Guide Update (http://developer.intel.com/design/pcisets/designex)
- Intel® 440LX AGPset Application Notes and Specification Updates (www.intel.com)



#### 82443EX/82443LX Pin Differences **1.2**

Pin differences between the 82443LX and 82443EX are as follows:

Ball Number	82443LX Name	82443LX Type of Pin	82443EX Name	Relationship to Reduced Feature
AF13	SRAS2#	0	NC	1.0.1
AF10	SCAS2#	0	NC	1.0.1
AC19	RCSA4#	0	NC	1.0.1
AB17	RCSA5#	0	NC	1.0.1
AF9	WE2#		NC	1.0.1
AC12	WE3#		NC	1.0.1
AD14	MAB0	0	NC	1.0.1
AF14	MAB1	0	NC	1.0.1
AE14	RCSA6#/MAB2	0	NC	1.0.1
AB14	RCSA7#/MAB3	0	NC	1.0.1
AE15	SCAS3#/MAB4	0	NC	1.0.1
AF15	SRAS3#/MAB5	0	NC	1.0.1
AA19	RCSB0#/MAB6	0	NC	1.0.1
AF16	RCSB1#/MAB7	0	NC	1.0.1
AB19	RCSB2#/MAB8	0	NC	1.0.1
AE16	RCSB3#/MAB9	0	NC	1.0.1
AF18	RCSB4#/MAB10	0	NC	1.0.1
AD18	RCSB5#/MAB11	0	NC	1.0.1
AB18	RCSB6#/MAB12	0	NC	1.0.1
AD17	RCSB7#/MAB13	0	NC	1.0.1
AF12	CDQB1#	0	NC	1.0.1
AE12	CDQB5#	0	NC	1.0.1
B12	GNT3#	0	NC	1.0.2
D12	GNT4#	0	NC	1.0.2
B13	REQ3#	I	TM1 (PU)	1.0.2
D13	REQ4#	I	TM2 (PU)	1.0.2, 1.0.5
U23	ECCERR#	0	NC	1.0.3
AD8	MECC0		NC	1.0.3
AE8	MECC1	_	NC	1.0.3
AF22	MECC2		NC	1.0.3
AB21	MECC3		NC	1.0.3
AC8	MECC4		NC	1.0.3
AB9	MECC5		NC	1.0.3
AE22	MECC6		NC	1.0.3
AD22	MECC7		NC	1.0.3
V24	WSC#	0	NC	1.0.4

- All pins labeled NC are NO CONNECTS and should not be connected on the motherboard
  All pins labeled (PU) should be connected to a 4.7K to 10K ohm pull-up resistor to 3.3V on the motherboard.



# 1.3 Memory Configuration Strapping

The Intel® 440EX AGPset based system must be configured for "Memory Configuration #2" by ensuring that there are no external pull-up resistors on the CKE pin of the 82443EX device. This will configure the PAC for the "Small DRAM array".

# 1.4 82443EX/82443LX Register Differences

Register setting differences between the 82443LX and 82443EX are shown below. These specific register/bit combinations should be set as indicated to support the Intel 440EX AGPset. Refer to the Intel® 440EX AGPset datasheet for more detail.

Register Name	Address Offset	Change To
PACCFG - PAC Configuration Register (Device 0)	50-51h	Bit 15 - Note 1
		Bit 11 - Note 2
		Bit 8:7 - Note 3
		Bit 6 - Note 3
MBSC - Memory Buffer Strength Control Register (Device 0)	6C-6Fh	Bit 23:22 - N/A
		Bit 13:12 - N/A
		Bit 11:10 - N/A
		Bit 5:4 - N/A
		Bit 3:2 - N/A
		Bit 1:0 - N/A
ERRCMD - Error Command Register (Device 0)	90h	Bit 1 - Note 4
		Bit 0 - Note 4
ERRSTS0 - Error Status Register 0 (Device 0)	91h	Bit 7:0 - N/A

N/A (not applicable)

**Note 1**: This bit will be set to "1" as a result of the system configuration being single processor/no IOAPIC.

**Note 2**: This bit will be set to "0" as a result of the system configuration for Memory Configuration #2.

Note 3: This bit will be set to "0" as a result of the system configuration using non-ECC DRAM.

**Note 4**: This bit should be set to "0" since ECC error reporting via SERR# is not needed.

# 1.5 Additional Information

All Intel<sup>®</sup> 440LX AGPset Applications Notes and Specification Updates apply to the Intel<sup>®</sup> 440EX AGPset. These documents are available on the WEB or through Intel Field Representatives.

http://developer.intel.com/pcisets

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