Intel® 430TX PCIset

Design Guide Update

October 1998

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Contents

Revision History

Date of Revision	Document Name	Description
October 1997	001	Initial Release
April 1998	002	Added General Design Consideration 2, WHQL Testing Requirement Effective 7/01/98 - RI# Event Added General Design Consideration 3, PIIX4 THRM# Configuration if a Thermal Protection Circuit Is Not Used. Added General Design Consideration 4, SMBus Data and Clock Isolation from RTCCLK. Added General Design Consideration 5, Implementing a RESET BUTTON for Desktop Based Systems. Added General Design Consideration 6, Clock Skews.
August 1998	003	Added Schematic Layout and Routing Update 1- 2 and Documentation Change 2.
October 1998	004	Added General Design Consideration 7,PCIRST# Load Sensitivity.

Preface

This document is an update to the following document:

Intel 430TX PCIset Desktop Design Guide Rev 1.0, June 1997, order number 297739.

References may also be made to the following documents: Intel 430TX PCIset: 82439TX (MTXC) data sheet order number 290559 and 82371AB (PIIX4) data sheet order number 290562.

It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. This design guide is primarily targeted at the PC market segment and was first published in 1996, revised in 1997. Those using this design guide should check for device availability before designing in any of the components included in this document.

Nomenclature

General Design Considerations include system level considerations that the system designer should account for when developing hardware or software products using the 82430TX.

Schematic, Layout and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Codes Used in Summary Table

Doc: Document change or update that will be or has been implemented

Shaded: This information is either new or modified from the previous version of this document.

NO.	430TX General Design Considerations
1	Implication of MUXed CKEx/MAAx Pins: SDRAM Self-Refresh and ACPI PC97 Testing
2	WHQL Testing Requirement Effective 7/01/98 - RI# Event
3	PIIX4 THRM# Configuration if a Thermal Protection Circuit Is Not Used
4	SMBus Data and Clock Isolation from RTCCLK
5	Implementing a RESET BUTTON for Desktop Based Systems
6	Clock Skews
7	PCIRST# Load Sensitivity on PIIX4/PIIX4E

NO.	Plans	430TX Schematic, Layout, and Routing Updates
1	Doc	Guidelines to minimize ESD events that may cause loss of CMOS contents is added.
2	Doc	Added Correct Strapping for SMC FDC37C932FR Ultra IO Device VBAT Pin

NO.	Plans	430TX Documentation Changes
1	Doc	Flexible Motherboard Design Layout Review Checklist, section 2.2.8, IDE Interface, bullet 11 about the recommendation for 10K Ohm pull-down resistors on PDD7 & SDD7 is modified.
2	Doc	Flexible Motherboard Design Layout Review Checklist, section 2.3.1, Addition of New Item Regarding SMC Ultra IO VBAT Connection.

430TX General Design Considerations

1. Implication of MUXed CKEx/MAAx Pins: SDRAM Self-Refresh and ACPI PC97 Testing

The 82430TX desktop design implementation in the Intel 430TX PCIset Desktop Design Guide and the 430TX Customer Reference Board schematics are such that CKEx/MAAx are multiplexed. This provides a second copy of memory address MAx (MAAx). This implementation does not provide the capability of allowing SDRAM to enter into the self refresh mode in an S1 power down state. As a result:

1. The SDRAM will not self refresh during the S1 power down state and the system may hang upon power-up.
2. 430TX desktop designs copying the Customer Reference Board schematics will not pass the S1 power down ACPI tests used in PC97 testing effective 1 July 1997.

There are two design techniques which eliminate the problem with the SDRAM not entering self refresh during S1 power down and allow the platform to pass the S1 power down ACPI tests used in PC97 testing. These design techniques are:

1. Cut the SUSSTAT1# connection between the 82371AB PIIX4 and the 82439TX MTXC. As a result, the MTXC will continue to generate normal refresh cycles to the SDRAM while the system is in the S1 power down state.
2. Use a BIOS which has an SMI Handler which traps the PM_CNTR Register used by the OS to place the system into S1. The SMI Handler will then use the PIIX4 clock control logic to 'simulate' S1, thereby preventing the SUS/RES logic from ever asserting SUSSTAT1# to the MTXC. The MTXC will again continue to generate normal refresh cycles to the SDRAM while the system is in the S1 power down state. Psuedocode for this SMI handler is shown below.

For new designs the following memory options are available

1. Two Rows: These designs do not need CKE/CKEB to be used as MAA0/MAA1 muxed signals. Connect SUSSTAT1# from the PIIX4 to the MTXC and connect CKE/CKEB from the MTXC to the DIMM sockets. Buffering issues on CKE/CKEB to DIMM connections need to be analyzed and characterized for specific layouts.
2. Three or four Rows: These designs need CKE/CKEB used as MAA0/MAA1 muxed signals to support multiple DIMMs. Do not connect SUSSTAT!# from the PIIX4 to the MTXC.

Psuedocode for the SMI handler is shown below. This BIOS fix should only be used in those implementations already in use and only as a last resort. Future implementations should always use the hardware fixes.

BIOS SMI HANDLER FIX SYSTEM METRICS

For clarity, this discussion will assume the following

1. PIIX4 PM IO Space Register Block is 64bytes in length. PM_Base setting specifies SA[15:6] @ Func3 Reg 20h. The 32bit GPOREG @ PMBase+34 is last used register in this block. PMBase+38 thru PMBase+3F are UNUSED I/O in this block.
   a. PIIX4 responds to PMBase+38 thru PMBase+3F
   b. Using PMBase+40h will cause PIIX4 to Master-Abort the trapped Bus Cycle
2. At init time BIOS sets PM_BASE to 8000h, this places the PM1_CNTRL register reported to the OS in the ACPI FACP table at 8004h.

BIOS SMI HANDLER FIX

1. Remap PM1_CNTRL register reported to OS in ACPI FACP Table as 8040h

   Even if an IO Address is Trapped by the PIIX4, writes to that IO Address will pass. Remapping the PM1_CTRL address prevents OS writes to the PM1_CTRL register from triggering the SUS/RES state machine.
2. Setup PIIX4 Device Trap logic to trap any r/w to IO Address 8040h.
3. SMI Handler Processing
   a. Determine if IO Access was a read or a write

      Look at SMM_Saved_State.EAX

IF (AX=FFFF) Then READ Cycle	(PIIX4 Master Aborts always return FF's)
IF (AX != FFFF) Then Write Cycle	(FF for Byte, FFFF for Word, FFFFFFFF for DWORD)

   b. Read Cycle Processing

      SMI Handler reads the real PM1_CNTRL register and reports its contents back to the OS:

      Read 8004, and write it to SMM_Saved_State.EAX, exit SMI Handler without Restarting the IO cycle.
   c. IO Write Cycle Processing

      Assumes wake from PWRBTN only. See below for wake from RI, THRM, & USB

IF (SLP_TYP=S1 AND SUS_EN=1)

{ Save Context of Clock Control Logic (DEVACTB@Func3 Reg58h, PCNTRL@PMBase+10h)

PCNTRL.10 (BST_EN) = 0	Enabled System Events will restore System to full-speed clocking)
PCNTRL.4(THT_EN) = 0	Disable System Throttling
DEVACTB.25 = 1	Enable SMI on access of APM Command Reg
DEVACTB.24 = 0	Disable PCI Activity Event Monitor
DEVACTB.23:16 =	Don't Care
DEVACTB.15:8=	Don't Care
DEVACTB.6 = 0	Disable IRQ Global Reload Enable
DEVACTB.5 = 0	Disable IRQ8# Stop Break Event
DEVACTB.4 = 1	Enable ExtSMI#, **GPI1#**, **PWRBTN#**, and **LID** Stop Break Events
DEVACTB.3 = 0	
DEVACTB.2 = 0	Disable KYB/Mouse Global Standby Timer Reload
DEVACTB.1 = 0	Disable IRQ Clock Events
DEVACTB.0 = 0	Disable IRQ Stop Break Event

Read LVL2 Reg to put CPU into Stop Grant State

System Enters 'Simulated S1', upon detecting an Enabled Stop Break Event:

Clock Logic to Deasserts STPCLK, Break Event causes RSM_RST (ACPI WAK_STS) to be SET,

CPU Resumes execution in SMI Handler at ?instruction following Read LVL2?

DO NOT CLEAR THE RSM_STS BIT, OS IS SPINNING ON THIS BIT IN POS

DO NOT CLEAR ANY PM STATUS BITS....OS is expecting to see these set upon Waking

Restore Clock Control Logic (PCNTRL & DEVACTB Registers)
Exit SMI Handler **}**

ELSE { Forward contents of write to the real PM1_CNTRL Register @ 8004h)
Exit SMI Handler **}**

Wake from RI, Thrm#, and USB:

For S1 using POS (i.e., no power removed anywhere)
Unmask SCI and COM/RI IRQ @ 8259 in the SMI Handler
OS masks all IRQ's before putting the system to sleep
Enable IRQ Stop Break Events
This will cause Clock Control Logic to deassert STPCLK anytime SCI or COM IRQ occurs
Mask SCI and COM/RI IRQs before existing SMI handler
Leave the PIC masks the way the OS had them prior to entry into the SMI handler
Do not clear any ACPI GPE Status bits
RI_STS, USB_STS, THRM_STS

When SMI handler returns to control to OS, OS will check these flags (along with PWRBTN_STS) to determine what caused the wake up and process accordingly.

2. WHQL Testing Requirement Effective 7/01/98 - RI# Event

TX desktop systems that are submitted to WHQL after July 1, 1998 will not pass ACPI testing unless the RI# event is connected to a pin other than RI#. This insures that an SCI is generated in compliance with PC98 requirements .

If power management of an on-board modem is needed, the RI# of the modem should be connected to GPI1 of the PiiX4. This will allow the PiiX4 to generate an SCI. The RI# input of the PiiX4 will not allow generation of an SCI.

3. PIIX4 THRM# Configuration if a Thermal Protection Circuit Is Not Used

When not used in a thermal protection mode, THRM# must be pulled-up to the Core Power Plane with an 8.2K Ohm resistor.

4. SMBus Data and Clock Isolation from RTCCLK

SMBus SMBDATA and SMBCLK signals should be isolated from RTCCLK signals to prevent signal integrity problems.

5. Implementing a RESET BUTTON for Desktop Based Systems

The following should be considered when implementing a RESET BUTTON for desktop based systems:

The system reset button has typically been connected indirectly to the PWROK input of the pIIX4. This technique will not reset the suspend well logic, which includes the SM Bus Host and SLave controllers. T reset the hardware in the suspend will, the reset button should be connected to the RSMRST# input of the PIIX4. Assertion of RSMRST#, via a reset button, will result in a complete system reset. RXMRST# assertion will cause SUS[A-C]# to assert which results in the deassertion of PWROK if SUS[A-C]# controls the power supply PS-ON control signal. The deassertion of PWROK will cause the PIIX4 to assert PCIRST#, RSTDRV, and CPURST.

For mobile based systems, the Power Button is typically connected to the RSMRST# input of the PIIX4. Consult the appropriate design related collaterals regarding this implementation when designing mobile based platforms.

6. Clock Skews

The clock skew between any two HCLK loads must be less than 250 ps (follow layout recommendations or simulate). The skew between PCLKs must be less than 300 ps. The difference between rising edges of HCLK and PCLK must be between 1 and 4 ns.

7. PCIRST# Load Sensitivity on PIIX4/PIIX4E

A specific board sensitivity has been identified by PCD that may result in a low going glitch on a deasserted PCIRST# signal when it is lightly loaded. This glitch may occur as a result of VCC droop caused by simultaneous switching of most/all AD[31:0] signals from 0 to 1. This glitch can in some designs be low enough (below 1.7V) to interfere with proper operation of the Host PCI Bridge Controller component.

This sensitivity manifests itself on designs where PCIRST# is lightly loaded with less than approximately 50pF, or is not driving the entire PCI bus. Design features that could aggravate the problem are; an in-line active component on the PCIRST# signal, such as an AND gate or, lack of a series termination resistor on the PCIRST# signal at the PIIX4 or PIIX4E.

There are several improvements that can be implemented individually or in any combination. First, a series termination resistor between 22 and 33ohms placed close to the PIIX4/PIIX4E will help reduce the glitch. Second, an external capacitor of approximately 47pF will help reduce the glitch. Third, if the design currently uses an in-line active gate/buffer on PCIRST# to drive the PCI bus, consider removal of this gate/buffer entirely. The PIIX4/PIIX4E is designed to drive the entire PCI bus.

430TX Schematic, Layout and Routing Updates

1. Guidelines to Minimize ESD Events that may Cause Loss of CMOS Contents

Recommendations for New Board Designs:

1. Provide a luF X5R dielectric, monolithic, ceramic capacitor between the VCCRTC pin of the PIIX4/PIIX4E and the ground plane. This capacitor's positive connection should not be stubbed off the trace run and must be as close as possible to the PIIX4/PIIX4E. The cap must be no further than 0.5 inch from the PIIX4/PIIX4E. If a stub is required, it should be kept to a few mm maximum length. The ground connection should be made through a via to the ground plane, with no or minimal trace between the capacitor pad and the via.
2. Place the battery, 1K ohm series current limit resistor, and the common-cathode isolation diode very close to the PIIX4/PIIX4E. If this is not possible, place the common-cathode diode and the 1K Ohm resistor as close to the 1uF capacitor as possible. Do not place these components between the capacitor and the PIIX4. The battery can be placed remotely from the PIIX4/ PIIX4E.
3. On boards that have chassis-intrusion utilizing external logic powered by the VCCRTC pin, place the inverters as close to the common-cathode diode as possible. If this is not possible, keep the trace run near the center of the board.
4. Keep the PIIX4/PIIX4E VCCRTC trace away from the board edge. If this trace must run from opposite ends of the board, keep the trace run towards the board center, away from the board edge where contact could be made by people and equipment that handle the board.

Recommendations for Existing Board Designs;

1. The effectiveness of adding a 1uF capacitor, as identified above, needs to be determined by examining the routing and placement. For example, placing the cap far from the PIIX4 reduces its effectiveness.

2. Correct Strapping for SMC FDC37C932FR Ultra IO Device VBAT Pin

When the PIIX4/PIIX4E internal RTC is used, the SMC Ultra IO device, FDC37C932FR, VBAT pin must be connected to ground through between a 1K and 0 ohm pulldown resisitor.

430TX Documentation Changes

1. Flexible Motherboard Design Layout Review Checklist, Section 2.2.8, IDE Interface, bullet 11, concerning the recommendation for 10K Ohm pull-down resistors on PDD7 and SDD7 is modified.

This bullet indicated above is changed to read:

"There is no internal pull-up or down on PDD7 or SDD7 of the PIIX4. The ATA3 specification recommends a 10K Ohm pull-down on DD7 in section 4.3.1. Devices shall not have a pull-up resistor on DD7. It is recommended that a host have a 10K Ohm pull-down resistor on PDD7 and SDD7 to allow the host to recognize the absence of a device at power-up. This pull-down resistor allows the BIOS to recognize the absence of an IDE slave device. Without this pull-down, some BIOSes may take up to 30 seconds to recognize that there is no slave device, or some BIOSes may hang the system."

2. Flexible Motherboard Design Layout Review Checklist, Section 2.3.1, Addition of New Item Regarding SMC Ultra IO VBAT Connection.

A new bullet will be added to section 2.3.1 to read:

"When the PIIX4/PIIX4E internal RTC is used, ensure that the VBAT pin of the SMC Ultra IO device FDC37932FR, is connected to ground through a pulldown resistor between 1K and 0 ohms. Consult your IO device vendor for implementation guidelines for this or other IO devices."

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