Using SDRAM in Intel® 430TX PCIset Embedded Designs

Application Note

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Application Note

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1.0 Introduction

This application note discusses the benefits of using Synchronous Dynamic Random Access Memory (SDRAM), explains the differences between SDRAM and Fast Page Mode (FPM)/ Extended Data Out (EDO) DRAM, and describes design layout considerations when using SDRAM instead of FPM/EDO DRAMs in 430TX PCIset designs.

2.0 The Benefits of Using SDRAM

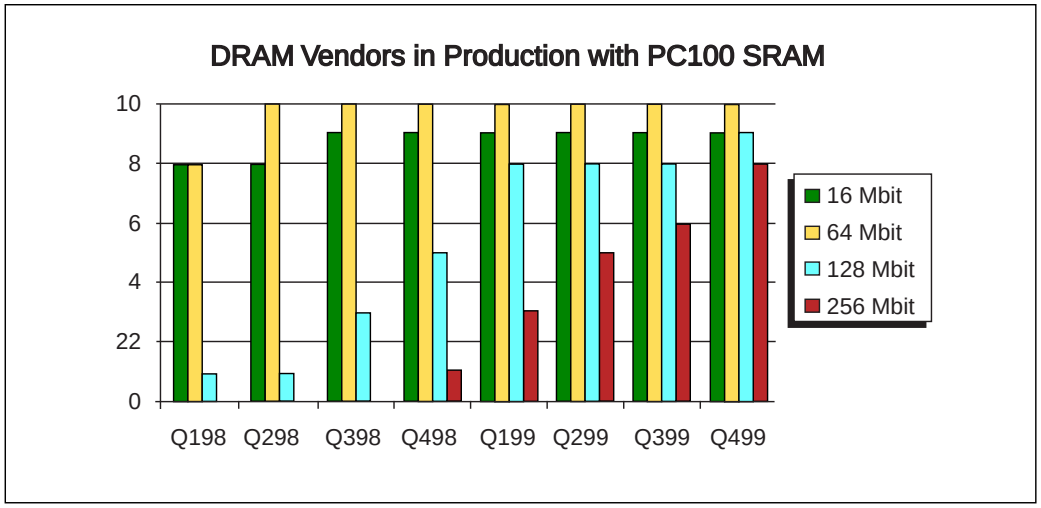
Dynamic random access memory (DRAM), with cycle times of approximately 60 ns, once provided acceptable performance in most embedded designs. Today, with processors running at speeds of 166 MHz, 200 MHz, and faster, DRAM accesses require the insertion of wait states, which degrades system performance. With programs running simultaneously in the Windows* environment, the external (L2) cache receives fewer hits, creating a bottleneck in system performance. Because the processor must more frequently access memory—rather than cache—designers must use increasingly larger caches. If the DRAM is accessed ‘randomly’, as its name implies, the performance would be quite low in systems that have processor speeds greater than 100 MHz. High-performance systems demand fast memory access times to keep up with the heavy workload imposed upon them.

SDRAM technology uses existing device technology and conforms to a JEDEC standard. The architecture features two independent memory banks that can be accessed individually or in an interleaved, or seamless, fashion. The independent banks allow each SDRAM to have two different rows active at the same time. This means that the data can be read from or written to one bank while the other bank is being precharged. The SDRAM interface uses a clock or synchronous interface, which eases system setup/hold requirements on the address and control pins. Therefore, using SDRAMs simplifies the design of the chipset/memory interface, enabling it to be based on a simple state machine operation.

One industry objective is to ensure that memory subsystems continue to support evolving platform requirements and that memory does not become a bottleneck to system performance. It is especially important that the PC memory roadmap evolves together with the performance roadmaps for the processors, I/O, and graphics. To meet this goal, Intel has worked with leading DRAM vendors to develop the PC100* SDRAM component and DIMM specifications that are now available on Intel's developer web site.

In addition, Intel participates in an ongoing industry dialog to ensure that memory suppliers get their technical questions answered. Figure 1 summarizes PC100 SDRAM availability data collected from 10 DRAM vendors (Fujitsu*, Hitachi*, Hyundai*, LG Semicon*, Micron Technology*, Mitsubishi*, NEC*, Samsung*, Texas Instruments*, and Toshiba*). This shows that the industry is on-track for the 66-MHz to 100-MHz SDRAM transition in the second half of 1998.

Figure 1. DRAM Vendors in Production with PC100 SDRAM



Source: DRAM vendors—information not verified by Intel

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3.0 Functional Differences between SDRAM and FPM/ EDO DRAMs

The following sections list the performance characteristics of FPM DRAM, EDO DRAM, and SDRAM.

3.1 FPM DRAM Characteristics

- Up to 33 MHz operation
- Level RAS# control
- Falling edge of CAS# latches column address
- Rising edge of RAS# turns data output buffer off
- Refresh modes: RAS-only, CAS-before-RAS, and Hidden

3.2 EDO DRAM Characteristics

- Up to 50 MHz operation
- FPM with a different output buffer stage
- Falling edge of CAS# latches column address
- OE# controls data output buffer
- Refresh modes: RAS-only, CAS-before-RAS, Hidden, and Self

3.3 SDRAM Characteristics

- Up to 100 MHz operation
- Inputs and outputs synchronous to clock
- All operations initiated using commands
- Pulsed RAS# control
- Two banks for on-chip interleaving (better hit rate)
- Refresh modes: Auto and self

4.0 Memory Design Considerations for Intel® 430TX PCIset

The Intel 82439TX System Controller (MTXC) integrates a DRAM controller that supports a 64-bit memory array from 4 Mbytes to 256 Mbytes of main memory. The MTXC supports Standard FPM, EDO, and SDRAM memories using 32-bit wide single in-line memory modules (SIMMs), 64-bit wide unbuffered dual in-line memory modules (DIMMs), and 64-bit wide unbuffered small-outline DIMMs (SO-DIMMs). DRAM parity is not supported, and for loading reasons, parity modules should not be used. All three memory types can be mixed and matched. The MTXC generates all DRAM control signals and multiplexed addresses for the DRAM array. The DRAM controller interface is fully configurable using a set of control registers.

When DRAM types (EDO, FPM, and SDRAM) are mixed, each row is optimized for that particular type of DRAM. The MTXC supports six rows of memory (six RAS#/CS# lines). For maximum memory flexibility and performance, it is recommended that a DRAM configuration of four rows be used. This configuration allows 64-Mbit DRAM devices to be used and permits mixing SDRAM and EDO/FPM DRAM. Figure 2 shows an EDO/FPM configuration using x32 SIMM modules and Figure 3 shows a four-row EDO/FPM/SDRAM configuration using x64 DIMM modules (or x64 SO-DIMMs).

Note: For reliability reasons, it is not recommended to mix SDRAM (which are 3-V devices) with 5-V EDO/FPM SIMMs, unless the SDRAM and EDO/FPM are properly isolated (e.g., the memory data lines are isolated using Qswitches). Not all SDRAMs are 5-V tolerant.

Figure 2. FPM/EDO Four-Row SIMM Configuration

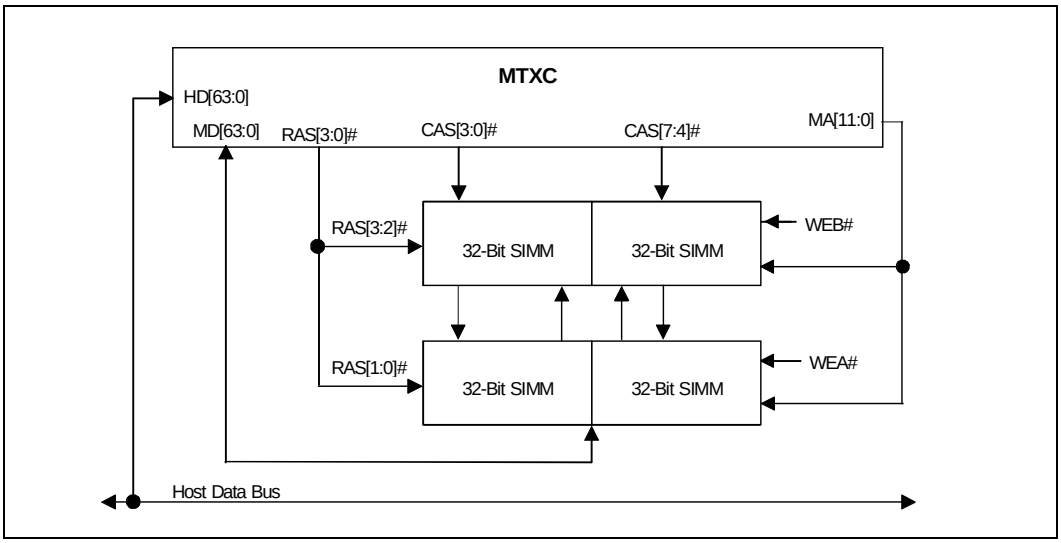
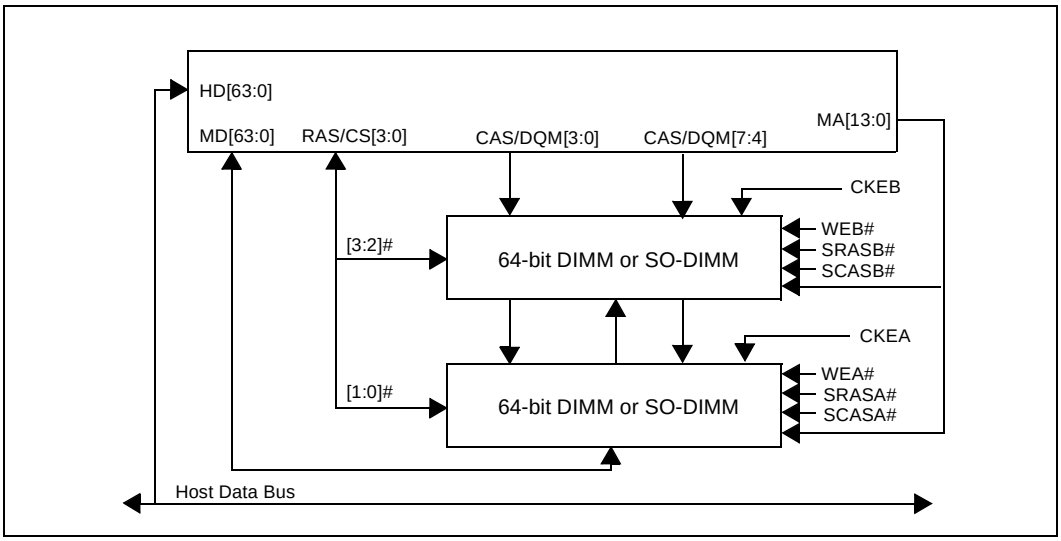


Figure 3. FPM/EDO/SDRAM Four-Row DIMM or SO-DIMM Configuration



NOTE:

1. In a configuration that supports suspend to RAM, only CKE is used. This is because CKEB is not part of the suspend well that the MTXC maintains during a suspend to RAM state.
2. In a desktop system that supports EDO/FPM, CKE and CKEB should be used as the second pair of MA0 and MA1 lines. CKE is used as MAA0 and CKEB is used as MAA1. In this case, they should be evenly distributed throughout the system along with the first pair of MA0 and MA1 lines.

5.0 SDRAM Configuration Requirements

5.1 General Configuration Requirements

In a system that uses 64-Mbit SDRAM, the RAS4#/CS4#/BA1 and RAS5#/CS5#/MA13 signals are used to provide two additional address lines, BA1 and MA13. KRQAK/CS4_64# is used to provide the fifth CS# line, if required.

To enable 64-Mbit support for four rows of SDRAM, SDRAMC [bit 1] must be set to 1 (offset 54h). To enable 64-Mbit support for five rows of SDRAM, SDRAMC [bit 1] must be set to 1, and DRAM cache must *not* be present in the system (indicated by CEC [bit 5]=0, offset 53h). In a five-row SDRAM system that supports 64-Mbit SDRAM devices, the KRQAK/CS4_64# signal provides the fifth CS# (or CS4_64#) function. This means that a system that supports DRAM cache cannot support five rows of 64-Mbit SDRAM. However, four rows of 64-Mbit SDRAM with DRAM cache are supported.

In an FPM/EDO-only configuration, there are no restrictions on using 64-Mbit devices (i.e., all six rows can support 64-Mbit DRAM devices). However, SDRAMC [bit 1] must be set to 1 when more than four rows of EDO/FPM are used. Setting this bit allows the RAS4# and RAS5# functions to be used.

	Driven on RAS5#/CS5#/ MA13	**Driven on RAS4#/ CS4#/ MA13**	**Driven on KRQAK/ CS4_64#**	**64-Mbit (SDRAM)**	**64-Mbit (EDO/ FPM)**
Bit 1, reg 54h=0	RAS5#/CS5#	RAS4#/CS4#	KRQAK	no	yes (6 rows)
Bit 1, reg 54h=1 and DRAM Cache is present†	MA13	BA1 (Bank Select)	KRQAK	Yes (4 rows)	Yes (4 rows)
Bit 1, reg 54h=1 and DRAM Cache is not present1	MA13	BA1 (Bank Select)	RAS4#/ CS4_64#	Yes (5 rows)	Yes (5 rows)

†The presence of DRAM cache is indicated by the value in bit 5, register 53h.

Other general configuration requirements include the following.

- Due to loading, using SDRAM x4 devices is not recommended.
- The buffering of SDRAM rows is not supported.
- In a five-row system, the fifth row is intended to be implemented with DRAM devices that are soldered to the motherboard. If a DIMM or a SIMM is used in the fifth row, it should *not* be used as an upgrade path by the end user; the size and type of DRAM that can be implemented in the fifth row is restricted.
- The total memory supported is 256 Mbyte, even though it is possible to populate the six rows with more than 256 Mbyte. This limit must be specified by the system BIOS.

5.2 EDO/FPM-only Configuration Requirements

- When more than four rows of x4 DRAM devices plus one row of x8 DRAM devices of memory are supported, it is recommended that all six rows be buffered. MA and MWE# signals should be buffered. In a system that supports only x8 or x16 devices (i.e., x4 devices are not supported), six rows of memory can be supported without buffering.
- The maximum load supported without buffers is four rows of x4 DRAM devices plus one row of x8 DRAM devices.
- A second pair of MA0 and MA1 signals are provided by muxing CKE with MAA0 and CKEB with MAA1. In a desktop system, the second pair of MA lines must be used to support 5-2-2-2 EDO performance in more than two rows of memory. The second pair of MA lines are not required in a mobile system, assuming x4 devices are not used. The MA functionality is selected via DRAMC [bit 2] (67h).

5.3 SDRAM-only Configuration Requirements

- The maximum number of rows supported is five rows of x8 devices.

5.4 Mixed SDRAM/EDO/FPM Configuration Requirements

- When SDRAM and EDO/FPM are mixed in a system, the configuration is limited to a maximum of four rows (two rows of x4 EDO/FPM and two rows of x8 or x16 SDRAM). If only x8 or x16 EDO/FPM and SDRAM devices are used (i.e., x4 devices are not used), five rows can be supported.
- SDRAMs can be mixed with EDO/FPM on a row-by-row basis (e.g., row 0 can be populated with SDRAMs while row 3 is populated with EDO/FPM devices).
- A second pair or MA0 and MA1 signals are provided by muxing CKE with MAA0 and CKEB with MAA1. In desktop systems, the second pair of MA lines must be used to support 5-2-2-2 EDO performance in more than two rows of memory. The second pair of MA lines are not required in a mobile system, assuming x4 devices are not used. The MA functionality is selected via DRAMC[bit 2] (67h).

5.5 Host and PCI Clock Layout for an EDO/FPM/SDRAM Design

The following is the host clock layout for a two-DIMM SDRAM/EDO/FPM design. Note that the clock synthesizer component has eleven host clock outputs. When an SDRAM design must implement more than four rows, a clock synthesizer component with 15 host clock outputs is required (four separate clocks are connected to a double-sided SDRAM DIMM).

Host clock layout requirement:

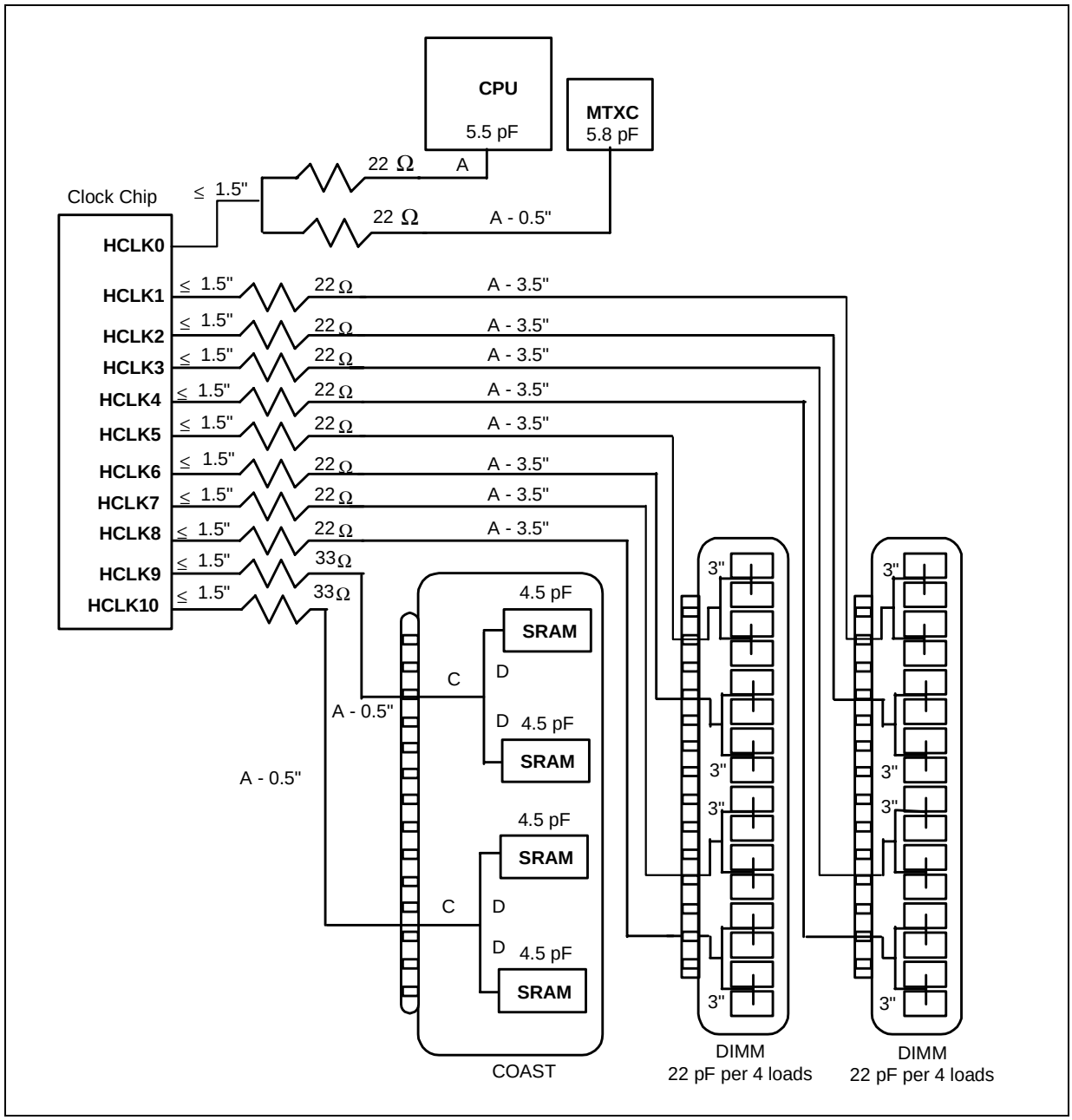
Where:

$D < 1.0''$

$C + D = 3.0''$

Note that trace length ‘A’ is primarily dictated by the host clock-to-CPU trace.

Figure 4. Host Clock Layout Recommendation for a Two-DIMM Design (SDRAM/EDO/FPM)



6.0 DRAM and System Options

Because SDRAM module design is in its infancy, manufacturers and users have not yet consistently defined its speed nomenclature. However, there are similarities among the various nomenclatures.

FPM/EDO DRAM performance is specified by the DRAM timing parameters (e.g., tRAC, tCAC), whereas SDRAM performance has two measures: clocking capabilities (tCK) and the DRAM timing parameters. The de facto industry standard for SDRAM speed designations is to use clocking capabilities alone—specifying *66 MHz* and *100 MHz* (15 ns and 10 ns, respectively) to describe a device sounds more impressive than *-6* and *-7* (60 ns and 70 ns, respectively). The DRAM performance is often buried within the specifications. Unfortunately, each manufacturer's DRAM timing parameters vary to some degree within the SDRAM. Care must be used in deferring the required number of clocks to be used for the DRAM parameters. If the simplest common denominator timings are not used, some SDRAM modules may cause conflicts.

Table 1 shows the possible DRAM and system options supported by the 430TX PCIset.

Table 1. Memory Types Supported by the Intel®430TX PCIset

DRAM Type	FPM, EDO, SDRAM
DRAM/SDRAM Module Type	72-pin SIMM: 32 bit; 168-pin DIMM: 64 bit
DRAM/SDRAM Voltage	3.3 V, 5.0 V
Number of rows of memory	1 to 6
DRAM Speed	50, 60, 70 ns
DRAM Component Width	x4, x8, x16
SDRAM Speed	66/60 MHz, RAS-to-CAS latency=2 or 3 clocks
SDRAM Component Width	x8, x16
CPU Bus Frequency	60, 66 MHz

7.0 Conclusion

Today's high-performance systems continue to demand data at faster rates. Transfer rates provided by the main memory may not keep pace with system requirements. Using SDRAM provides system designers with a roadmap for using future high-bandwidth processors.

To avoid unexpected behavior in systems that use the 430TX PCIset and SDRAM, platform designers should use only SDRAMs that meet the PC SDRAM Specification and should follow all motherboard layout guidelines found in the *Intel® 430TX PCIset Desktop Design Guide* (order number 297739).

8.0 Related Information

Intel offers a variety of information through the World Wide Web at http://www.intel.com.

Table 2. Related Documents

Document Name	Intel Order Number
Intel® 430TX PCIset: 82439TX System Controller (MTXC) datasheet	290559
Intel® 430TX PCIset System Controller (MTXC) Timing Specification	273134
430TX Specification Update	290615
82371AB PCI-to-ISA/IDE Xcelerator (PIIX4) datasheet	290562
Intel® 82371AB PCI ISA IDE Xcelerator (PIIX4) Timing Specification	273135
Intel® 82371AB (PIIX4) Specification Update	297738
Intel® 430TX PCIset Desktop Design Guide	297739
Intel® 430TX PCIset Design Guide Update	290613