AP-589

APPLICATION NOTE

Slot 1 Processor EMI Overview

April 1997

Order Number: 243334-001

CONTENTS

1.0. INTRODUCTION

Experiments indicate that EMI radiation from Pentium® Pro processors can meet regulatory requirements. Worst case radiation levels are approximately 20 dB below regulatory specifications (assuming a typical desktop or server chassis which is capable of 20 dB of shielding effectiveness) to processor radiation frequencies up to 2 GHz.

The Pentium Pro processor implemented the connection between the Level 2 (L2) cache, the cache controller, and the processor on a bus structure, known as the cache bus. Starting with the Pentium II processor, cache bus radiation levels increased due to higher frequency operation and an increase in the effective cache bus current loop area. The latter increases primarily due to moving the L2 cache out of the processor package onto the processor substrate, increasing the interconnect lengths.

Scaling the cache bus radiation levels from the Pentium Pro processor data indicates that emissions may become significant when cache bus frequencies exceed 150 MHz. This document details the validation and mitigation strategies that Intel has pursued to ensure low cost solutions are in place so that systems using our future processors will pass regulatory requirements for radiated emissions.

1.1. Terminology

Electromagnetic Interference (EMI). Radiation from an electrical source interrupting the normal operation of an electronic device.

Electromagnetic Compatibility (EMC). The successful operation of electronic equipment in its intended electromagnetic environment. Encompasses energy generated within or external to the system.

Emissions. Energy emanating from an external source that may pose a threat to other equipment. This energy may be conducted or radiated.

1.2. References

ABC's of EMI and RFI, Daryl Gerke and Bill Kimmel, Kimmel Gerke Associates, Ltd., St. Paul, June 1994.

EDN's *Designer's Guide to Electromagnetic Compatibility*, Daryl Gerke and Bill Kimmel, Cahners Publishing Co., January 1994.

An Introduction to Electromagnetic Compatibility, Clayton R Paul, John Wiley and Sons, New York, 1992.

2.0. EMI BACKGROUND

This document focuses on the efforts made by Intel and additionally, the efforts required of Personal Computer Original Equipment Manufacturers (PC OEMs) to prevent Intel processors (based on the Single Edge Contact (S.E.C.) cartridge form factor) from interfering with other electronic products.

There are generally two methods by which interference can occur: (1) below 30 MHz EMI RF noise is *conducted*, and (2) above 30 MHz RF noise is *radiated*. As all of the frequencies generated for and by the Pentium II processor exceed 66 MHz, this document concerns itself only with emissions above 66 MHz.

2.1. EMI Regulations and Certifications

PC OEMs ensure Electromagnetic Compatibility (EMC) by meeting EMI regulatory requirements. PC OEMs must ensure that their computer systems do not exceed the emission limit standards set by applicable regulatory agencies. The two standards that this document references are: (1) the United States' Federal Communication Commission's (FCC) Part 15B, and (2) the International Electrotechnical Commission's International Special Committee on Radio Interference (CISPR) 22B. Table 1 and Table 2 list the frequency and associated radiation limits.

Table 1. FCC Part 15B Limits

Frequency (MHz)	Radiation (dB uV/m)
30 – 88	40.0
88 – 216	43.5
216 – 960	46.0
Above 960	54.0

NOTES:
Quasi-peak measured at 3 meters.

Table 2. CISPR 22B Limits

Frequency (MHz)	Radiation (dB uV/m)
30 – 230 MHz	30.0
230 – 1000 MHz	37.0

NOTES:
Quasi-peak measured at 10 meters.

3.0. PENTIUM® II PROCESSOR EMI FEATURES

Intel routed traces away from areas likely to exacerbate EMI. Intel is investigating additional ways to further reduce EMI for future products.

3.1. Current EMI Reducing Features

The Pentium II processor design routes all clock traces on layers of the processor substrate adjacent to reference planes. All processor substrate clock traces avoid substrate and power plane edges. No processor substrate clock traces cross power plane boundaries. Clock traces also avoid possible antennas such as the thermal plate retention posts and clips. Series resistors on the processor substrate slow down edge rates where practical.

3.2. Possible Future EMI Reduction Features

3.2.1. CLOCK GENERATOR

Intel is presently working with vendors to develop a system clock generator with an EMI mode. This EMI mode should reduce peak radiation by a minimum of 8 dB. The clock generator will have a compatible footprint and pinout with existing clock generators, and Intel expects it to be available at a later date to support future generations of Slot 1 processors.

The clock generator reduces radiated emissions by spreading the emissions over a wider frequency band. Radiated emissions are typically confined in a narrow band centered about clock frequency harmonics. This band can be broadened, with subsequent reductions in the measured radiation levels, by slowly frequency modulating the processor clock over a few MHz. By uniformly distributing the radiation over a band of a few MHz, regulatory measurement levels (in a 120 kHz band) will be reduced. Figure 1 shows the effects of a prototype spread spectrum clock generator on cache bus radiation.

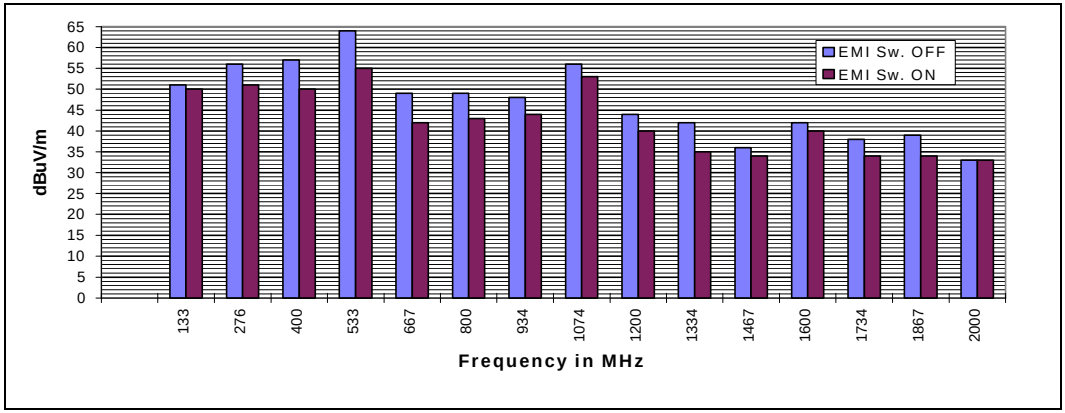

Figure 1. Impact of a Spread Spectrum Clock on Cache Bus Emitted Radiation

3.2.2. SHIELDING

For future generation Slot 1 processors, Intel is investigating an integrated metallic shield that fits within the cover of the S.E.C. cartridge. The S.E.C. cartridge encloses the processor substrate and attaches to pads on the substrate located just above the substrate edge fingers.

This shield will not be implemented on the Pentium II processor, but may be required for future processors that operate at significantly higher frequencies.

4.0. SYSTEM EMI DESIGN RECOMMENDATIONS

This section suggests techniques that system designers may use to ensure EMC.

4.1. Clock Trace Routing

Clocks and their associated circuitry may have the greatest impact on EMC. The following pointers help reduce the clock circuit radiation.

- Route clock traces on any layer that has an adjacent reference plane layer (voltage or ground). Emission levels of a signal are directly proportional to the distance of the signal from a reference plane.
- Minimize the use of added trace length to increase delay time of clock signals. Where possible, use series resistance to accomplish needed delays.
- Keep clock traces at least 100 mils from the edge of an adjacent reference plane layer. This increases the amount of radiation emanating from the clock trace that the reference plane captures.
- Keep clock vias to a minimum.

4.2. High Speed Signal Routing

High speed signals also contribute to EMI radiation. Keep the following points in mind when routing high speed signals.

- Route high speed, high duty cycle signal traces (strobes, least significant address lines) over a continuous reference plane. For example, when routing on layers adjacent to the power plane, do not route these traces over breaks in this plane. Routing traces over power plane voids increases both common and differential mode radiation.
- Minimize the number of high speed data traces and least significant address traces that cross breaks in the reference plane. Least significant address lines tend to switch more often than more significant address lines.
- Follow sound interconnect principles (like parallel, series or dual-ended termination) to minimize high speed signal ringing.

4.3. Other Motherboard Design Considerations

- Keep the power plane shorter than the ground plane by at least 3X the spacing between the power and ground planes. This allows any AC difference in potential to be absorbed by the ground plane.
- Position the Slot 1 connector on the motherboard so that the S.E.C. cartridge is at least two inches from I/O connector pins. This should reduce coupling to manageable levels.
- Keep leads on through hole components short. Mount the components as close to the PCB as possible and trim leads if necessary.
- Position system clocks as far as possible from signals that go to cables.
- Connect the Slot 1 connector's EMI pins to ground via 0(resistors. Future Slot 1 processors may use these pins for EMI suppression.

4.4. Case Construction

The system case reduces EMI by containing EMI radiation. The two main factors that impact the effectiveness of the case in reducing EMI are the case material and discontinuities in the case. The following points help mitigate case discrepancies.

- Keep chassis seams as far away from the processor as practical. The example below shows that seams become leaky at 1/20 wavelength. Therefore, even seams 2 inches long leak 300 MHz frequency EMI.

$$f = c/\lambda$$

Where:

f = frequency passed through the seam

c = speed of light = 3×10^8 m/s

$\lambda/20$ = length of the seam = 2” = 0.05m

λ = 40” = 1m

f = $3 \times 108/1m = 300$ MHz

- Wherever possible use round holes instead of slotted holes. Round holes provide the greatest airflow volume for the least amount of EMI leakage.
- Thin material works fine for most high frequency I/O shielding. However, I/O shielding should be grounded at as many points as possible. I/O shielding may need to be stiffened to prevent system to system EMI variation.

4.5. Cabling

Cables make excellent antennas. The following suggestions reduce the impact of cables on EMI radiation.

- Provide adequate grounding for all cables.
- Ground both ends of cables to chassis ground.
- To prevent coupling, keep all cables away from chassis seams.
- Use ferrite beads to attenuate common mode noise on I/O cables.

5.0. POSSIBLE EMITTED PROCESSOR FREQUENCIES

Table 3 shows the harmonic frequencies of Pentium II processor clocks. The Pentium II processor may be the source of emissions at one or more of these frequencies. Often, the source of emission is the motherboard, a peripheral or add-in card. Use an EMI sensing probe (or pick-up coil) to determine the source of EMI emissions.

Table 3. Possible Emitted Processor Frequencies

Harmonic	Cache Bus (MHz) for 233 MHz Core	Cache Bus (MHz) for 266 MHz Core	Cache Bus (MHz) for 300 MHz Core
First	116.5	133	150
Second	233.0	266	300
Third	349.5	399	450
Fourth	466.0	532	600
Fifth	582.5	665	750
Sixth	699.0	798	900
Seventh	815.5	931	1050
Eighth	932.0	1064	1200
Ninth	1048.5	1197	1350
Tenth	1165.0	1330	1500
Eleventh	1281.5	1463	1650
Twelfth	1398.0	1596	1800
Thirteenth	1514.5	1729	1950
Fourteenth	1631.0	1862	2100
Fifteenth	1747.5	1995	2250
Sixteenth	1864.0	2128	2400
Seventeenth	1980.5	2261	2550

6.0. PENTIUM® II PROCESSOR EMI TEST RESULTS

This section discusses the experimentation conducted to verify that the Slot 1 form factor could meet regulatory requirements.

6.1. System Validation

6.1.1. PURPOSE

To determine the impact of a chassis design on EMI emissions.

6.1.2. SCOPE

Measure EMI radiation levels emanating from three different production chassis (all three used ATX motherboards). Configure chassis with cables connected and covers on. Determine the source of any frequencies that exceed the CISPR 22B limits. Conduct tests at Open Air Test Site (OATS) with chassis in both horizontal and vertical configuration. See Figure 2 for an example of the OATS site layout.

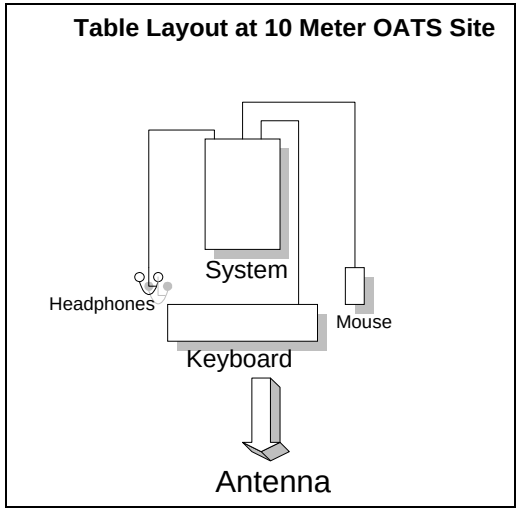

Figure 2. Setup for System Validation

6.1.3. RESULTS

The testing showed that it is possible to meet CISPR 22B requirements with a Pentium II processor-based ATX motherboard installed.

Chassis A, a desktop chassis, exceeded CISPR 22B limits (see Table 4 and Table 5) at 199 MHz and 207 MHz. This was due to a known motherboard frequency coupling to the headphone I/O cable. A motherboard redesign was required to bring the failing frequencies back below CISPR 22B limits.

Chassis B, a different desk top chassis, (see Table 6 and Table 7) passed at all frequencies.

Chassis C, a tower chassis, exceeded CISPR 22B limits (see Table 8 and Table 9) at 199 MHz and 465 MHz with a 233 MHz processor. The same chassis failed only at 199 MHz with a 266 MHz processor installed. Since the same motherboard was used for all three chassis tests, the 199 MHz was determined to be generated by the motherboard. The absence of the 465 MHz failing frequency with the 266 MHz processor indicated that the source of the 465 MHz was the Pentium II processor. 465 MHz is the fourth harmonic of the cache bus. The excessive radiation was snooped to the peripheral cables. Manual movement of the I/O shield brought emissions down below specified limits. Improving the stiffness and grounding of the I/O EMI shield reduced the EMI radiation to passing levels.

Table 4. Chassis 'A' EMI Marginal Frequencies with Core Clock at 233 MHz

Frequency (MHz)	QP Level (dBu V/m)	Limit (dBu V/m)	Delta (dBu V/m)	Orientation
207	30.5	30.0	+0.5	Vertical
199	27.9	30.0	–2.1	Vertical
207	29.4	30.0	–0.6	Horizontal
199	28.1	30.0	–1.9	Horizontal

Table 5. Chassis 'A' EMI Marginal Frequencies with Core Clock at 266 MHz

Frequency (MHz)	QP Level (dBu V/m)	Limit (dBu V/m)	Delta (dBu V/m)	Orientation
199	33.0	30.0	+3.0	Vertical
207	28.5	30.0	–1.5	Vertical
199	30.5	30.0	+0.5	Horizontal
207	27.7	30.0	–2.3	Horizontal

Table 6. Chassis 'B' EMI Marginal Frequencies with Core Clock at 233 MHz

Frequency (MHz)	QP Level (dBu V/m)	Limit (dBu V/m)	Delta (dBu V/m)	Orientation
125	28.5	30.0	–1.5	Vertical
504	31.5	37.0	–5.5	Vertical
200	26.4	30.0	–3.6	Horizontal
465	32.5	37.0	–4.5	Horizontal
124	24.1	30.0	–5.9	Horizontal

Table 7. Chassis 'B' EMI Marginal Frequencies with Core Clock at 266 MHz

Frequency (MHz)	QP Level (dBu V/m)	Limit (dBu V/m)	Delta (dBu V/m)	Orientation
125	26.6	30.0	–3.4	Vertical
504	33.5	37.0	–3.5	Vertical
75	24.9	30.0	–5.1	Vertical
116	24.2	30.0	–5.8	Vertical
360	31.0	37.0	–6.0	Vertical
229	24.7	30.0	–5.3	Horizontal
200	24.7	30.0	–5.3	Horizontal

Table 8. Chassis 'C' EMI Marginal Frequencies with Core Clock at 233 MHz

Frequency (MHz)	QP Level (dBu V/m)	Limit (dBu V/m)	Delta (dBu V/m)	Orientation
199	39.0	30.0	+9.0	Vertical
133	28.5	30.0	–1.5	Vertical
465	34.2	37.0	–2.8	Vertical
698	31.6	37.0	–5.4	Vertical
199	40.7	30.0	+10.7	Horizontal
465	37.4	37.0	+0.4	Horizontal
698	34.4	37.0	–2.6	Horizontal
86	24.4	30.0	–5.6	Horizontal
731	31.1	37.0	–5.9	Horizontal

Table 9. Chassis 'C' EMI Marginal Frequencies with Core Clock at 266 MHz

Frequency (MHz)	QP Level (dBu V/m)	Limit (dBu V/m)	Delta (dBu V/m)	Orientation
199	33.5	30.0	+3.5	Vertical
66	25.1	30.0	–4.9	Vertical
199	37.9	30.0	+7.9	Horizontal
458	32.7	37.0	–4.3	Horizontal
598	32.1	37.0	–4.9	Horizontal
432	31.8	37.0	–5.2	Horizontal
465	31.7	37.0	–5.3	Horizontal

7.0. TYPICAL EMI MEASUREMENTS

Figure 3 shows radiated emissions from a production version of the 233 MHz Pentium II processor on a production motherboard in a production chassis. The chassis does not exceed the FCC three meter limits.

Figure 4 and Table 10 show worst case EMI measurements taken using a production Pentium II processor on a production Intel motherboard in a production Intel chassis. Measurements are referenced to CISPR 22B limits.

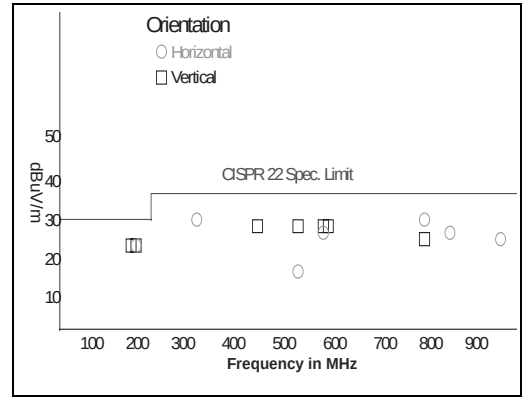

Figure 3. EMI Measurements from an Intel Production Motherboard and Chassis

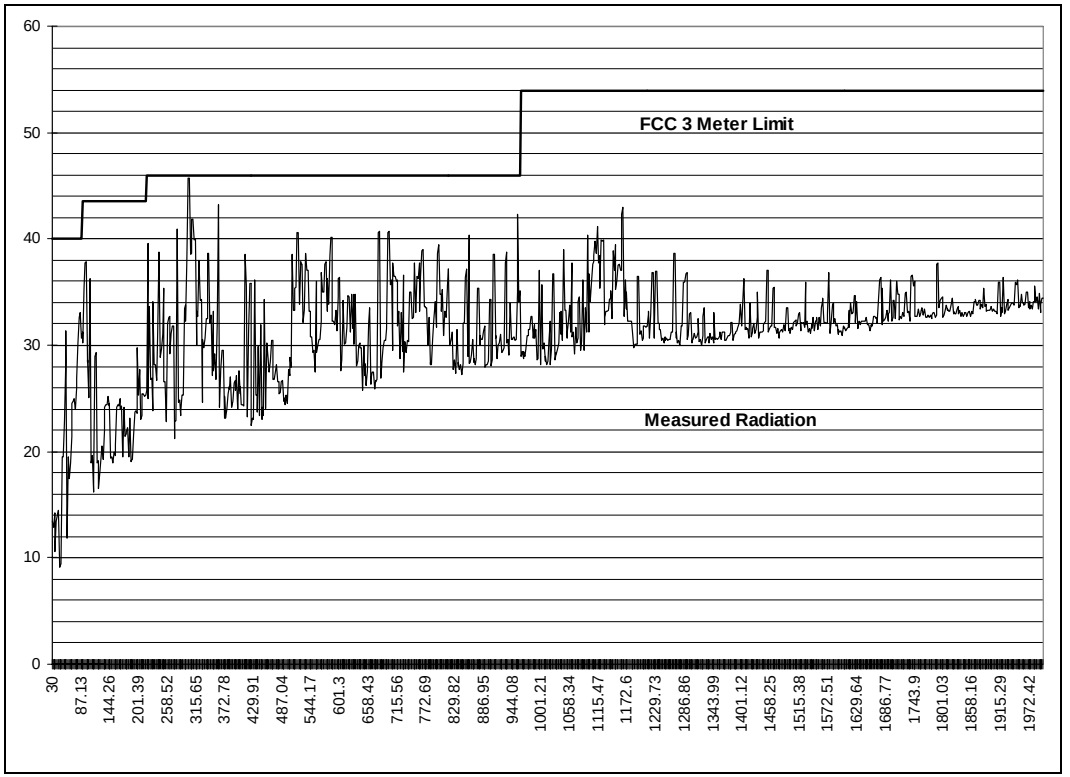

Figure 4. Scan of Production Pentium® II Processor

Table 10. EMI Measurements from an Intel Production Motherboard and Chassis

Frequency (MHz)	QP Level (dBu V/m)	Limit (dBu V/m)	Delta (dBu V/m)	Orientation
199.760	21.7	30.0	–8.3	Vertical
200.460	21.6	30.0	–8.4	Vertical
200.460	21.3	30.0	–8.7	Horizontal
332.910	31.5	37.0	–5.5	Horizontal
798.975	31.4	37.0	–5.6	Horizontal
798.975	26.9	37.0	–10.1	Vertical