Slot 1 Bus Termination Card Design Guidelines

August 1997

Order Number: 243409-002

1.0. INTRODUCTION

The Pentium® II processor includes termination circuitry for the microprocessor's GTL+ bus. In a 2-way multiprocessor system each end of the bus must be properly terminated, whether or not both processor locations (Slot 1 connectors) have processors installed. This document describes design considerations for a termination card to occupy the second Slot 1 connector location which terminates the bus when there is only one processor installed in a 2-way multiprocessor system.

Note that there are other ways to implement a bus termination card than as specified in this document. The resistor and decoupling network schematics in this document are recommendations only. The design guidelines within this document should be adhered to in order to ensure that the designed card will operate correctly in a 2-way multiprocessor system. However, other resistor and decoupling designs are feasible. This document does not provide detail on variations to the specific design solution presented.

Figure 1 shows the outside of the S.E.C. cartridge and the corresponding terminology.

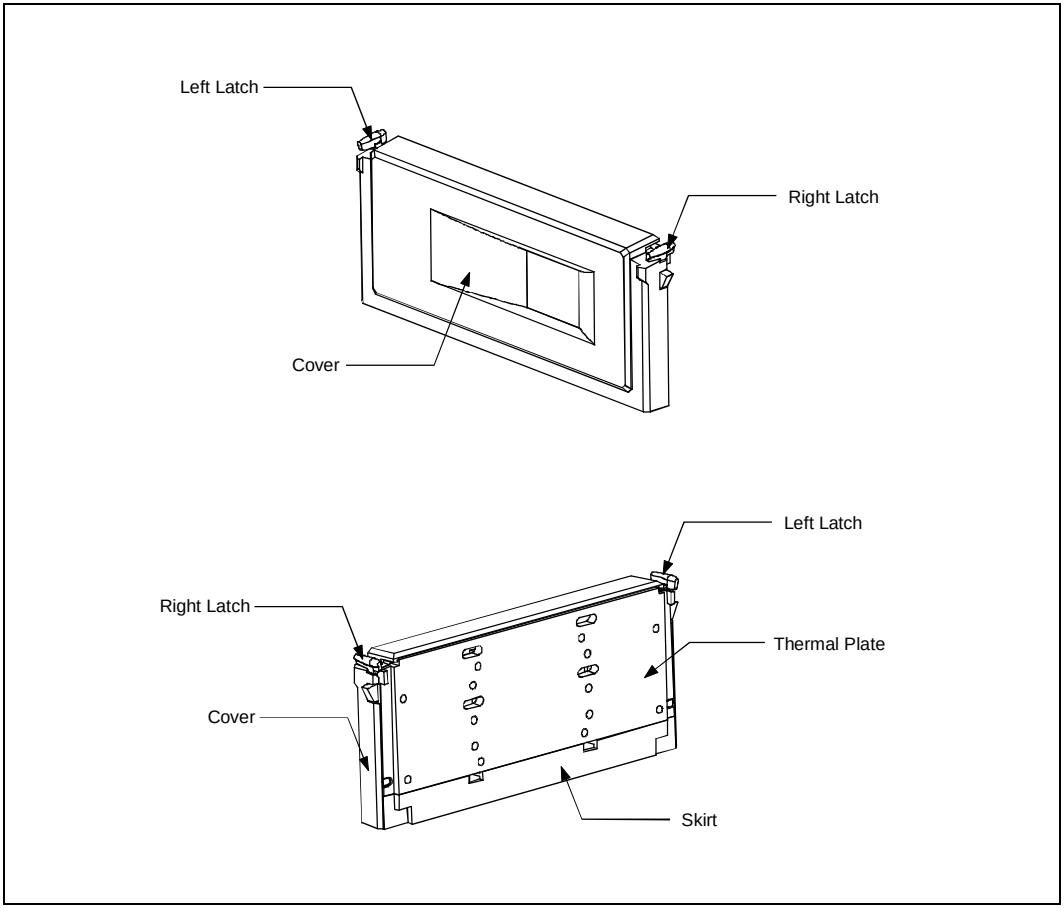

Figure 1. S.E.C. Cartridge - Thermal Plate and Cover Side Views

2. TERMINATION CARD REFERENCE SCHEMATICS

Figures 2 and 3 provide the names of the corresponding signals that are interfaced with the Slot 1 connector. Figure 2 represents the signals that are found on the thermal plate side of the processor substrate, and Figure 3 represents the signals that are found on the cover side of the processor substrate. A jumper to ground should be placed on the 100/66# signal. This will ensure compatibility with Slot 1 processors using either a 100 or 66 MHz system bus frequency in flexible system bus frequency platforms. This jumper should be closed for 66 MHz operation and open for 100 MHz operation.

Figures 4 and 5 are examples of termination resistor networks implemented with four resistor packages that have separate power and ground connections per resistor. Figure 4 shows the network for the thermal plate side signals which include the data signals. Figure 5 shows the network for the cover side signals which include the address and bus control signals. Note that the maximum power for each resistor is 0.05 W (i.e. 0.20 W/four pack of resistors) and that this is the maximum power per resistor that will need to be dissipated.

Figure 6 is a capacitor decoupling network from V_{TT} to ground that functions to prevent V_{TT} noise interference (voltage drop) on the bus signals. This interference is caused by the potential large current draw through the V_{TT} power distribution plane (or trace) to the termination resistors.

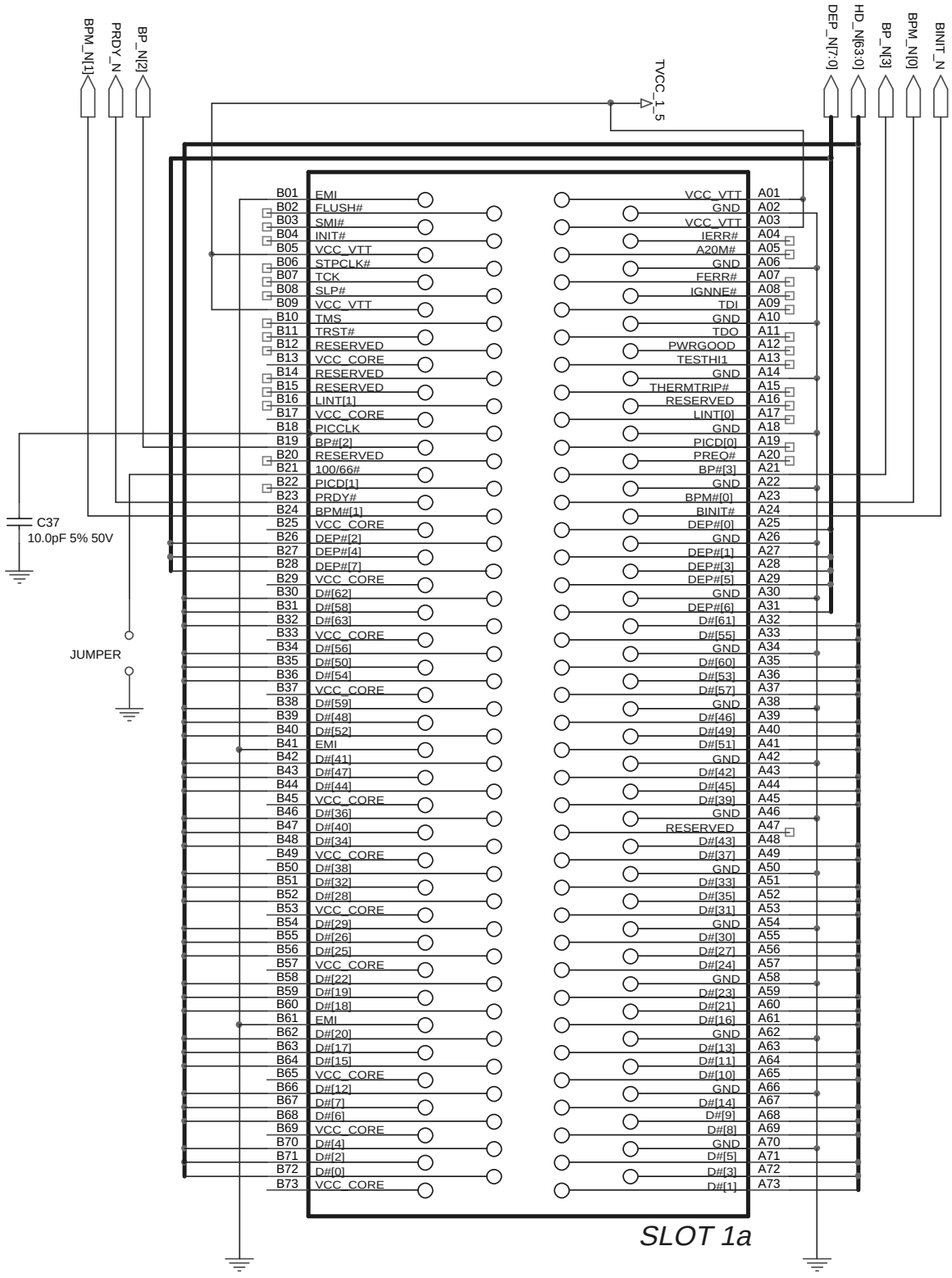

Figure 2, Slot 1, Thermal Plate Side

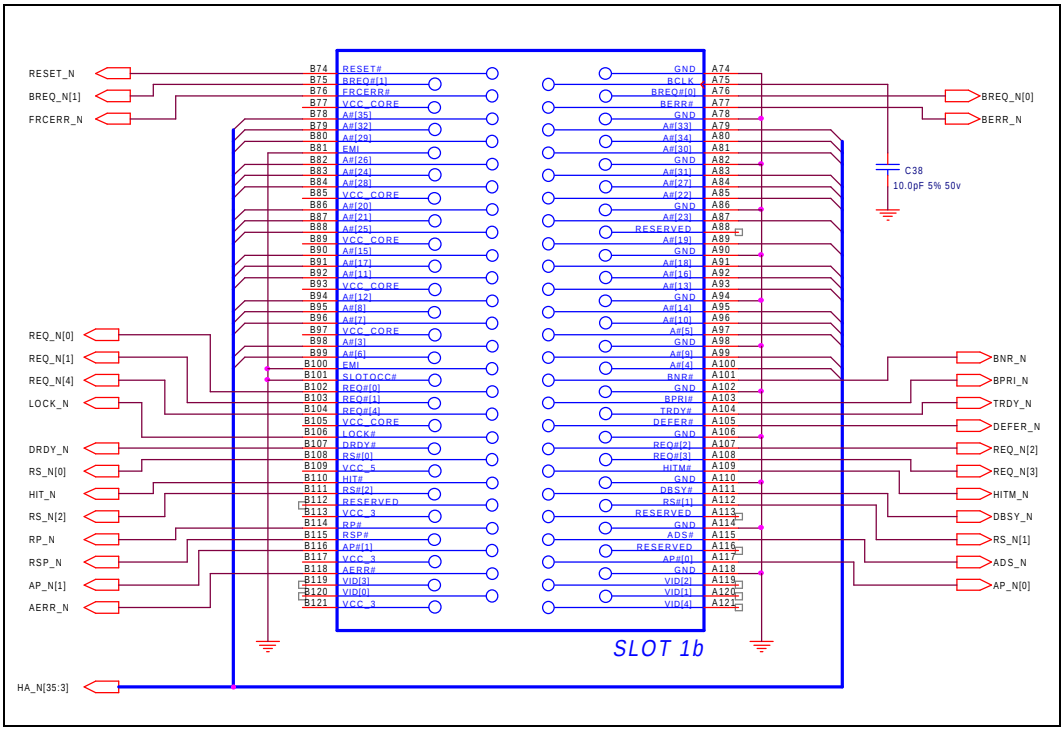

Figure 3. Slot 1, Cover Side

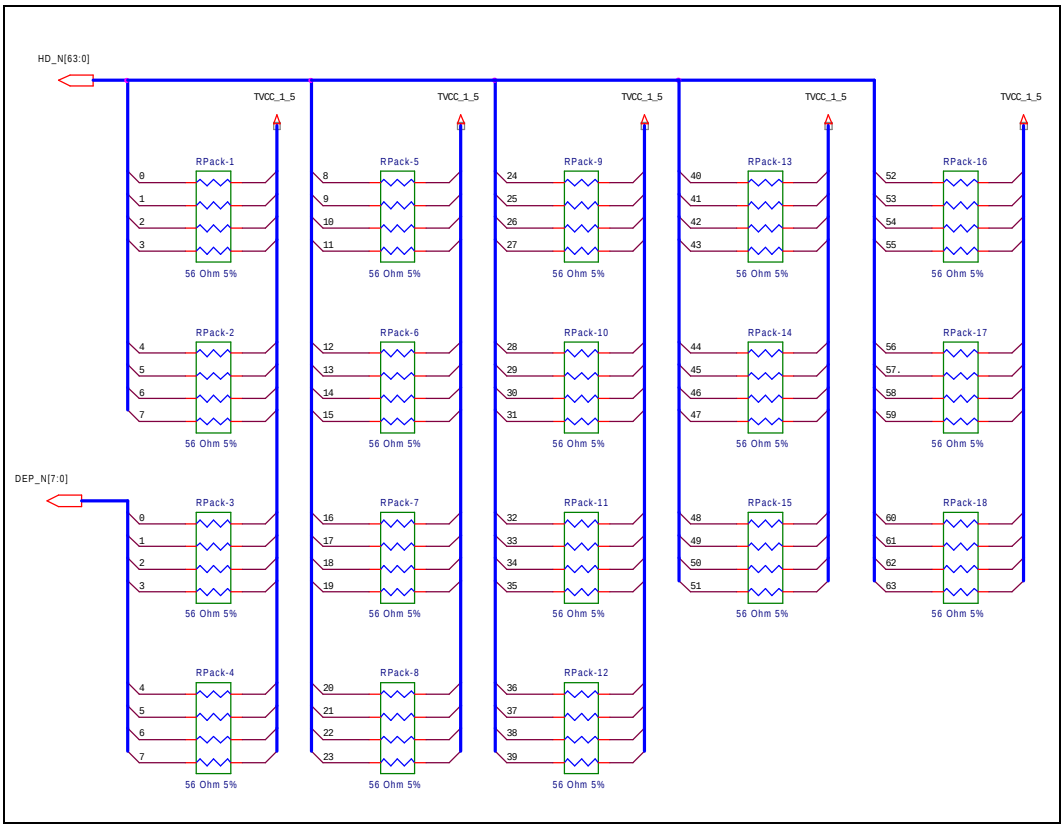

Figure 4. Termination Resistors, Thermal Plate Side

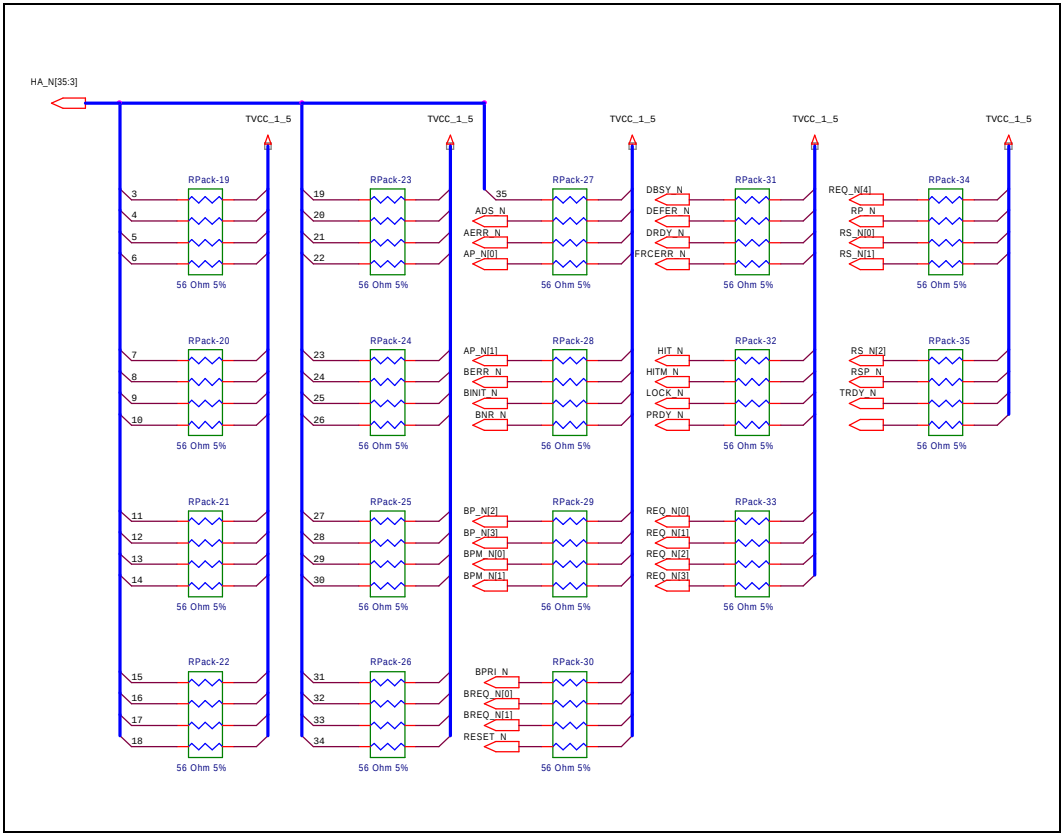

Figure 5. Termination Resistors, Cover Side

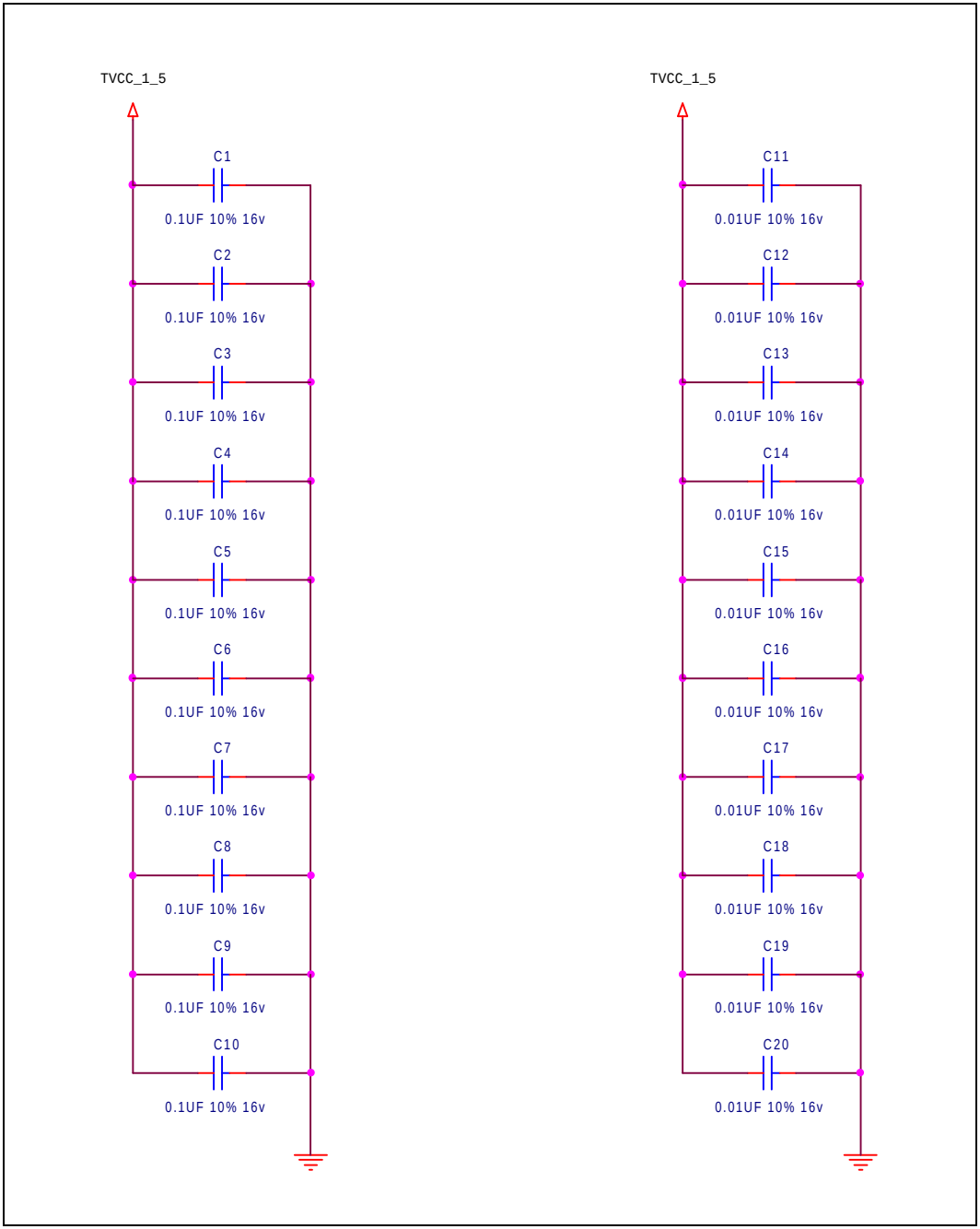

Figure 6. Termination Decoupling

3.0. GTL+ BUS GUIDELINES

The design should follow the guidelines in the application note: Pentium II processor GTL+ Guidelines. Below are some of these guidelines.

- Limit the trace routing length on the card to 1.5 inches.
- Distribute VTT with a wide trace or plane. A plane is recommended; however, a 50 mil minimum width trace may also be used.
- Closely control the characteristic line impedance, Z_0 (50Ω to 80Ω). A ground plane will be needed to maintain the proper characteristic line impedance.
- Make sure power routings are decoupled correctly. Please refer to the Pentium II processor GTL+ Guidelines, Section 5.2 for more information.
- A PCB signal velocity of 1.6 to 2.2 ns/ft should be used.
- Plan to minimize crosstalk by:
    1. Maximize the line-to-line spacing (at least 10 mils between traces).
    2. Keep the dielectric constant used on the termination card between 4.2 and 4.8.
    3. Minimize the cross sectional area of the traces, (5 mil lines with 1/2 ounce/ft^2 copper - but beware of higher resistively traces).
    4. Eliminate parallel traces between layers if not separated by a power or ground plane.
    5. Isolate GTL+ signals in groups. That is, route the data signals in one group, the control signals in one group, and the address signals in another group. If the groups are routed together on a plane, provide at least 25 mils separation between the groups.

Note that the use of standard "pull-up" resistor networks for termination may not be suitable. These networks have a common power or ground pin at the extreme end of the package, shared by 13 to 19 resistors (for 14- and 20-pin components). These packages generally have too much inductance to maintain the voltage/current needed at each resistive load. Intel recommends using discrete resistors, resistor networks that have separate power and ground pins for each resistor, or working with a resistor network vendor to obtain resistor networks that have acceptable characteristics. Figures 4 and 5 show resistor networks that utilize packages with four resistors and in which each resistor has a power and ground connection.

4.0. TERMINATION CARD PHYSICAL DESCRIPTION

Figure 7 illustrates a recommended physical format for the termination card. The card edge must mate properly with the Slot 1 connector (see Slot 1 Connector Design Guidelines). For details on S.E.C. cartridge dimensions please refer to the Pentium II processor at 233 MHz, 266 MHz and 300 MHz datasheet.

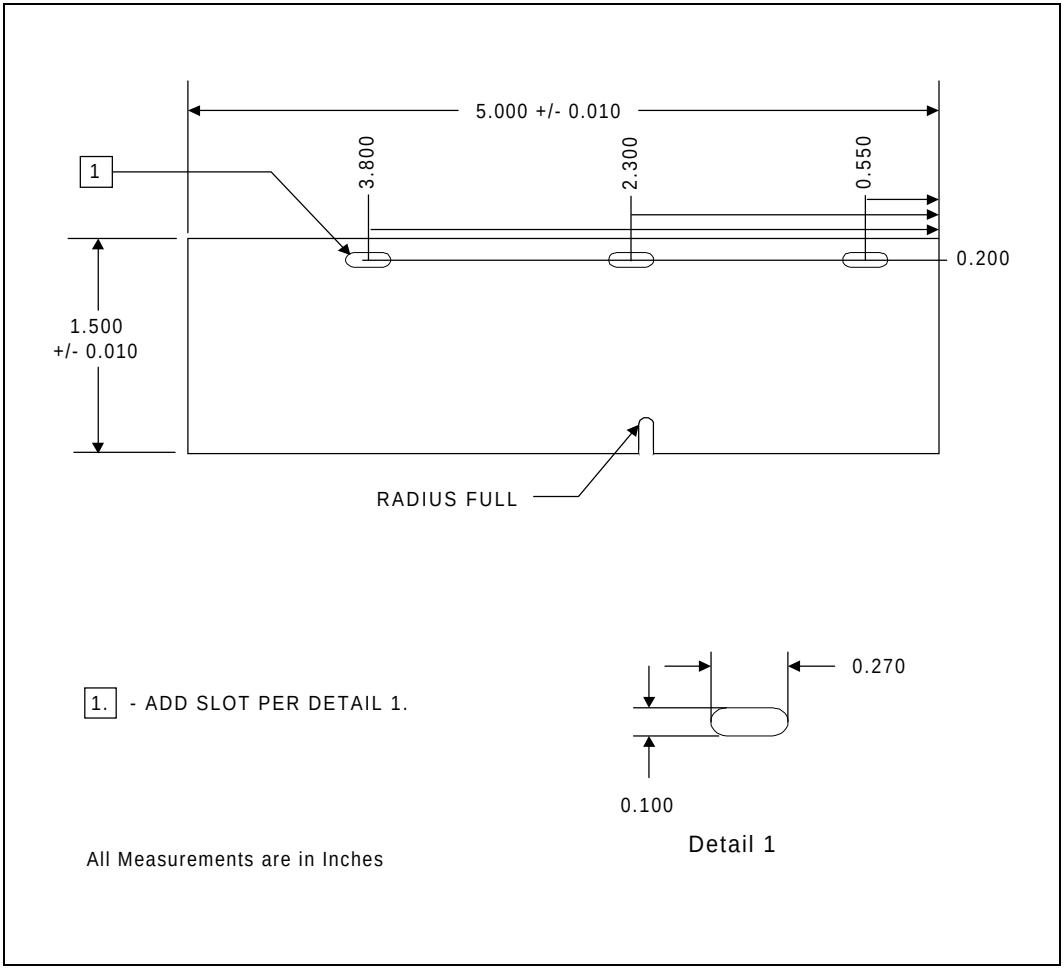

Figure 7. Termination Card Dimensions

5.0. TERMINATION CARD RETENTION

Intel has enabled a retention mechanism, shown in Figure 8. Computer board and system manufacturers install retention mechanisms on motherboards to ensure the mechanical integrity of systems with S.E.C. cartridges. Depending on the shock and vibration specifications, a latching adapter might be necessary to ensure the bus termination card remains secure. For a drawing of the latching adapter please refer to Figure 9. The latching adapter in Figure 9 is compatible

with the single processor retention mechanism in Figure 8 and the dual processor retention mechanism in Figure 10. Note that mechanical shock and vibration specifications are OEM dependent.

The bus termination card should be physically compatible with the same retention mechanism used for the S.E.C. cartridge. For supplier and mechanical information on the retention mechanisms please refer to the following URL:

http://www.intel.com/design/PentiumII/components/

Note that Figure 10 provides a drawing of the dual processor retention mechanism. The drawing represents one viable solution of a dual processor retention mechanism.

For detailed dimensions of the retention mechanisms please refer to the *Mechanical Support Pieces for S.E.C. Cartridge Processors*.

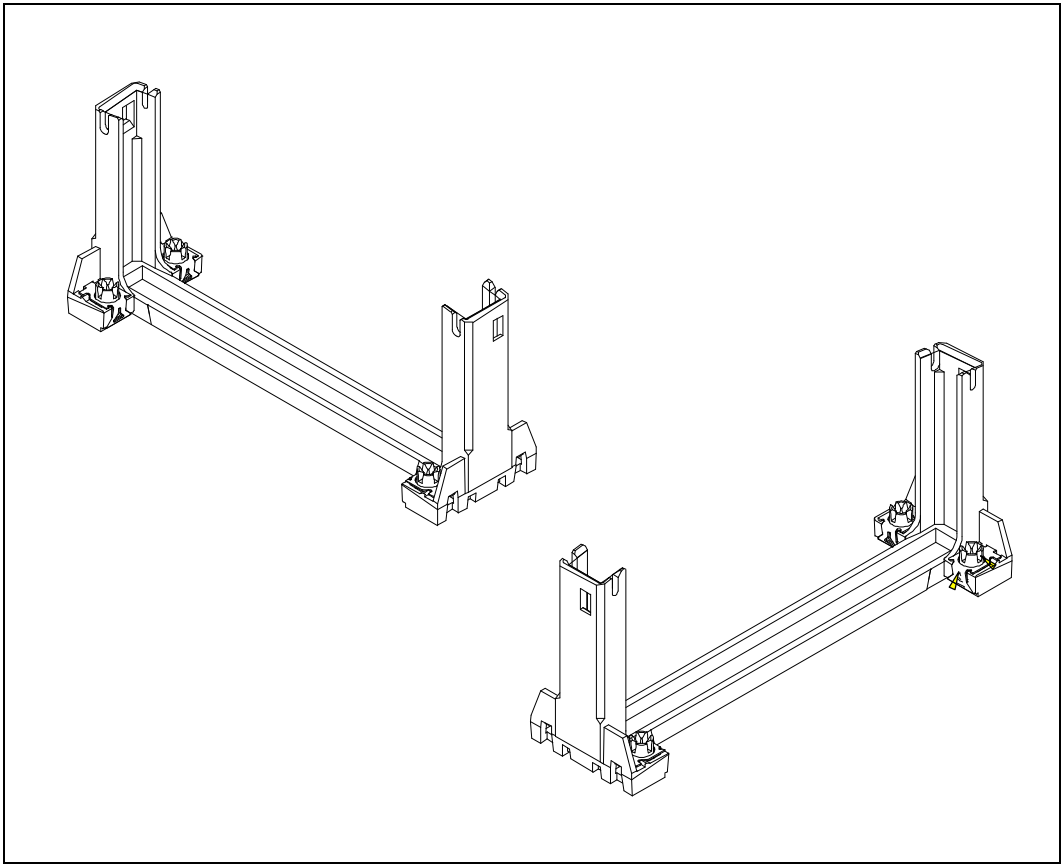

Figure 8. S.E.C. Cartridge Retention Mechanism

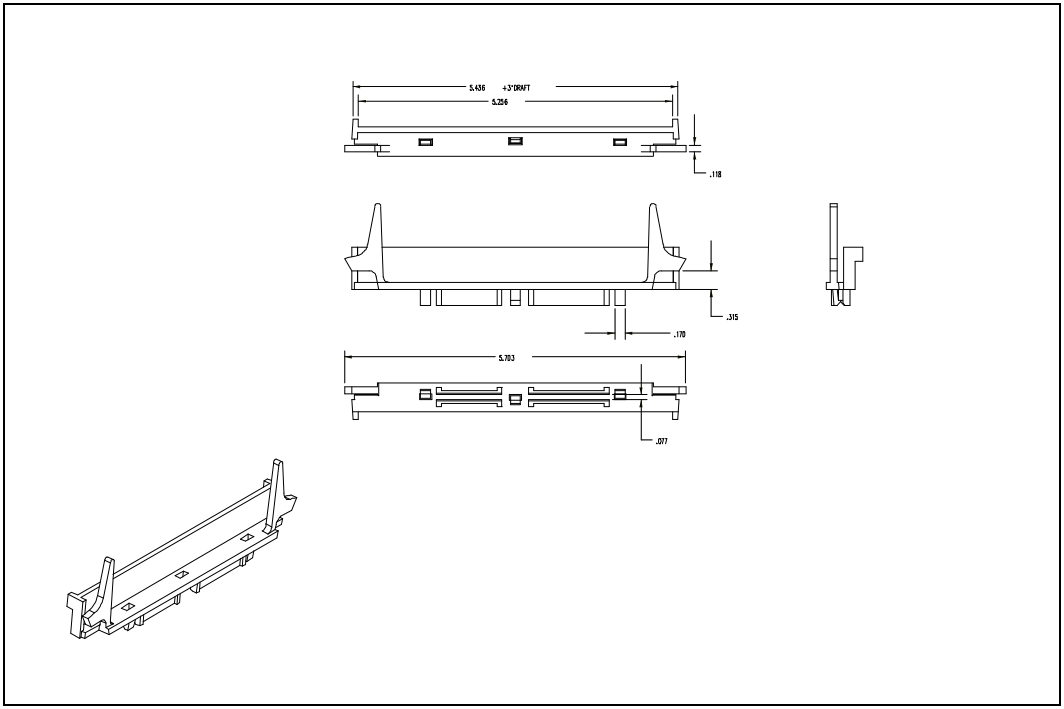

Figure 9. Latching Adapter Concept Drawings

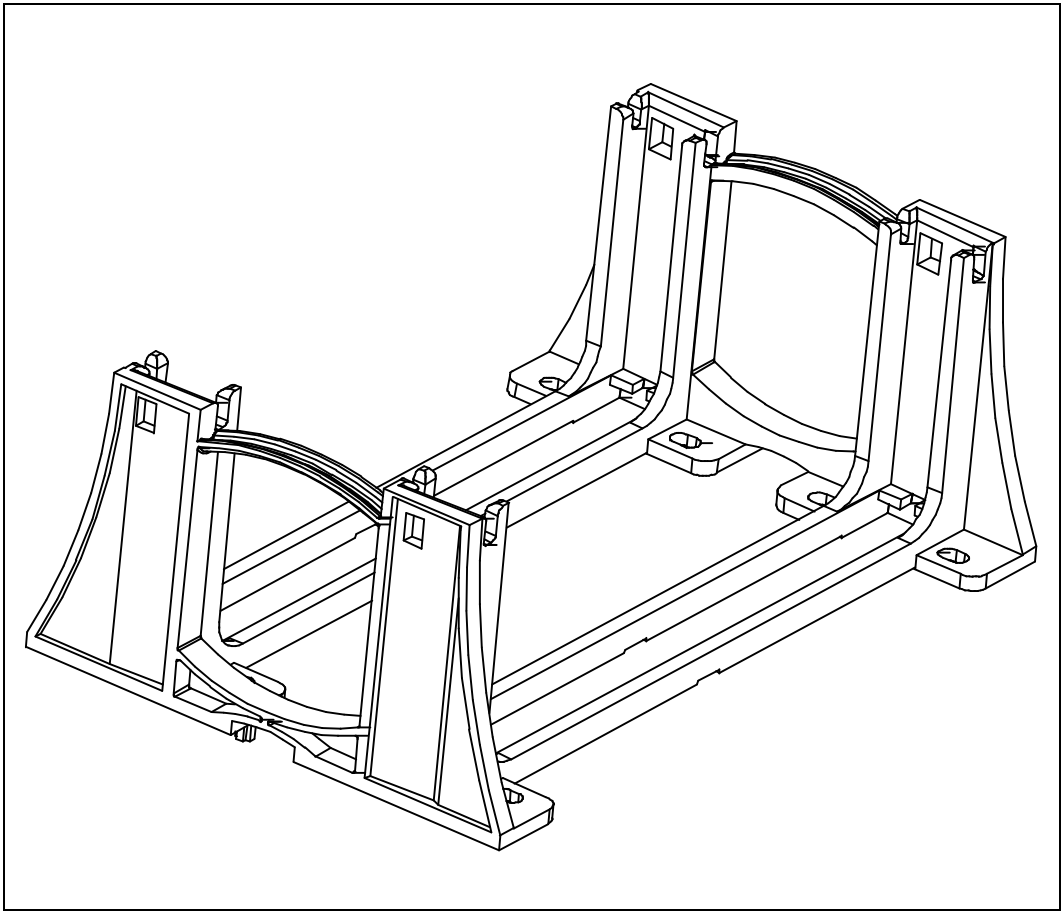

Figure 10. S.E.C. Cartridge Dual Processor Retention Mechanism

6.0. REFERENCE DOCUMENTS

Pentium® II Processor at 233 MHz, 266 MHz, and 300 MHz, Order Number 243335-001

Pentium® II Processor GTL+ Guidelines, Order Number 243330-001

**Slot 1 Connector Design Guidelines* - Revision 1.4

**Mechanical Support Pieces for S.E.C. Cartridge Processors*

*To be published. For a listing of current documentation available for the Pentium II processor please see:

http://developer.intel.com/design/PentiumII/