Application Note 89
High-Speed Micro Memory Interface Timing

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INTRODUCTION

The DS80C320 microcontroller was the first member of the new High-Speed Micro Family from Dallas Semiconductor. Since its introduction in 1993, there have been a number of new micros introduced which include new features and peripherals. The family now includes the DS80C310, DS87C520, and DS87C530, among others. The DS80C320 is unique in the family because it has slightly different external memory interface timing from the other members. When the DS80C320 was introduced, an application note (#57) was published to describe the speed requirements for the memories that interfaced to it. This application note serves the same purpose for the more recent family introductions.

One major difference in the timing of the new members of the family and the DS80C320 is that the original DS80C320 had a maximum clock rate of 25 MHz. All of the more recent 5-volt micros were introduced at a maximum clock rate of 33 MHz. Obviously, this affects the timing of the external memory interfaces significantly. The analysis that follows is based on a “worst case” timing using a 33 MHz clock, but will also identify memory speeds required for other frequencies as well.

A common configuration for a High-Speed Micro-based system is shown in Figure 1. In this example, both program (EPROM) and data (SRAM) memory devices are included in the system. Of course, with an EPROM-based part such as the DS87C520, it is likely that no other program storage will be required outside the processor. However, for the purposes of this discussion, it will be assumed that external program storage will be used. If the application dictates the use of both on-board and external program memories, some additional decoding logic (not shown) may be required so that the two memory spaces do not overlap.

As with all 8051 external memory interfaces, port 0 lines (P0.7-P0.0) of the processor carry both address and data, and a latch is used to demultiplex the information. The specific part number for the latch will be determined by the speed requirements of the system as discussed below. However, in general, the latch will be a ’373 or ’573 type. The main difference between these two part types is the pinout. On the ’573, all inputs are on one side of the package and all outputs are on the other. This allows a more convenient board layout.

The number of lines connected from the processor’s Port 2 address bus (P2.7-P2.0) to the memories’ address bus is shown in the figure as ‘N’. The exact value of ‘N’ is determined by the storage size of the memory devices used.

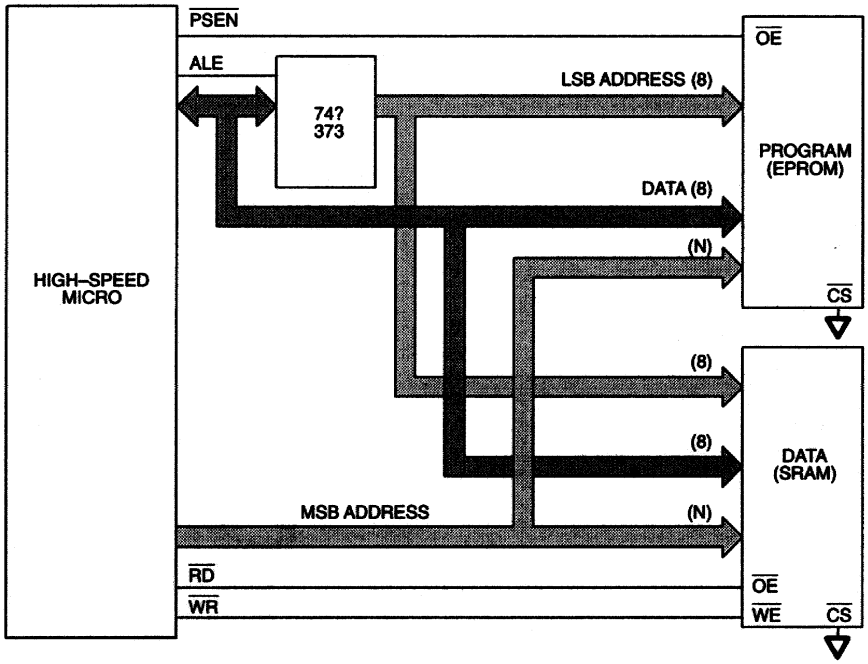
LATCH REQUIREMENTS

Due to the high speed of the Port 0 (AD7-AD0) bus, some consideration must be given to the choice of latches used for address demultiplexing. By examining the High-Speed Micro data sheet, it can be seen that some timing constraints are placed on the latch. For instance, the CPU parameter t_{AVLL} (Port 0 Address Valid to ALE Low) determines the minimum setup time (t_{SU}) the latch will actually have. The parameters t_{LHLL} and t_{LLAX} also affect the timing requirements of the latch. Table 1 shows the CPU parameters for 33 MHz operation, and the requirements placed on various latch families. For the parameters in the table, the CPU parameters must be greater than the latch parameters. It can be seen that

the minimum required setup and hold time are violated for the HC latch family (highlighted). For this reason, this family cannot be used for 33 MHz operation.

The other relevant property of the latch is its propagation delay from input to output. Since the latch is in the address path, this parameter has a direct and significant impact on the memory timing requirements. This parameter will be discussed in the following section.

TYPICAL HIGH-SPEED MICRO SYSTEM Figure 1



LATCH PARAMETERS Table 1

CPU PARAMETER	@33 MHz	LATCH PARAMETER	AC FAMILY	F FAMILY	HC FAMILY
t_{LLHL} min	40 ns	t_W	4.5 ns	6.0 ns	20.0 ns
t_{AVLL} min	10 ns	t_{SU}	6.0 ns	2.0 ns	15.0 ns
t_{LLAX} min	10 ns	t_H	1.0 ns	3.0 ns	13.0 ns
		t_{PROP}	11.5 ns	8.0 ns	38.0 ns

PROGRAM MEMORY

As shown in Figure 1, the program memory (typically EPROM) interfaces to the processor's LSB address through the address demultiplexing latch. The EPROM also interfaces directly with the processor via the MSB address bus and the Program Store ENable ($\overline{\text{PSEN}}$) signal. The processor always outputs the MSB address before the LSB address, so this interface can be ignored. However, each of the two remaining interfaces must be examined for the most critical timing. The relevant timing parameters for EPROM devices may be found by evaluating their data sheets. Table 2 summarizes the main parameters for several speed grades of EPROMs from two different manufacturers[1].

[1] EPROM devices from AMD and Amtel were considered.

EPROM PARAMETERS Table 2

PARAMETER	-55	-70	-90	-120	-150	-200	-250
t_{ACC} min	55 ns	70 ns	90 ns	120 ns	150 ns	200 ns	250 ns
t_{CE} min	55 ns	70 ns	90 ns	120 ns	150 ns	200 ns	250 ns
t_{OE} min	25/35 ns	30/40 ns	30/40 ns	35/50 ns	65 ns	75 ns	100 ns
t_{DF} min	25 ns	30/25 ns	30/25 ns	35/30 ns	30 ns	30 ns	30 ns

Note: X/Y indicates difference between the Atmel/AMD devices.

Upon evaluation of the timing specifications for the processor, the latch and the EPROM, it can be seen that the most critical timing path is through the LSB address bus. The address must appear on this bus, pass through the latch, address the EPROM, and the EPROM must output valid data in less time than the CPU parameter t_{AVIV}. Since the latch is in the path, the timing of this bus can be expressed by the following equation: $t_{PROP} + t_{ACC} < t_{AVIV}$. The DS87C520 data sheet shows that t_{AVIV} is a function of clock speed (denoted t_{CLCL}), and is given by: $t_{AVIV} = 3t_{CLCL}$ - 20 ns. Solving these equations for 33 MHz operation using an F type latch, it can be seen that an EPROM access time of less than 63 ns is required. Therefore for full speed operation, an EPROM with 55 ns address access time must be used because this is the slowest speed grade that meets the requirement of 63 ns.

The equation above shows that the latch speed directly impacts the required speed of the EPROM. Since a fast latch is less expensive than a fast EPROM, an F type latch is recommended at clock speeds that would necessitate the use of an EPROM of 120 ns or faster.

Solving for the clock speed in the equation, an F type latch is recommended for clock speeds greater than 19.8 MHz. Based on the same argument, an AC type latch is recommended for clock speeds greater than 16.8 MHz.

Table 3 shows the EPROM speeds and latch types recommended for various CPU clock speeds. The suggested speed grade is based on the above equation and the EPROM and latch timing parameters. Further evaluation shows that the EPROM parameter t_{DF} may also be a critical parameter at some high CPU clock speeds. This parameter must always be less than the CPU parameter t_{PXIZ}. As indicated in Table 2, t_{DF} varies for the same speed grade device from different manufacturers. Therefore in Table 3, AMD is the recommended manufacturer where a CPU frequency of 29.4912 MHz is used. If the Atmel device were used, the t_{PXIZ} parameter would be violated. This exception applies to any clock frequency between 30.61 MHz, where the switch of a 70 ns EPROM is made, and 28.47 MHz, where processor requirement for t_{PXIZ} becomes 30 ns.

RECOMMENDED EPROM SPEEDS Table 3

CLOCK FREQUENCY (MHz)	SPEED WITH 'F373 LATCH	SPEED WITH 'AC373 LATCH	SPEED WITH 'HC373 LATCH
33.0	**55**	55	N/A
29.4912	**70***	70	N/A
25.0	**90**	70	55
22.1184	**90**	90	70
20.0	**120**	90	90
19.8	120	**120**	90
18.432	120	**120**	90
16.8	150	120	**120**
16.0	150	150	**120**
14.746	150	150	**120**
14.318	150	150	**150**
12	200	200	**150**
11.059	200	200	**200**
7.37	250	250	**250**
1.8432 and below	250	250	**250**

* Should be AMD 70 ns device because of t_{DF}.

DATA MEMORY

There are a number of factors that make interfacing data memories (SRAMs) to the High-Speed Microcontroller family extremely easy. First, SRAM devices are generally faster, and more readily available in higher speed grades. In fact, it is sometimes difficult to find a slow SRAM. A more significant factor is that all High-Speed Micro Family members have the ability to insert stretch cycles into the MOVX instructions. This provides a convenient means of supporting both high- and low-speed devices on the same data bus without requiring external support hardware. All High-Speed Micro Family members default to the use of one stretch cycle for MOVX instructions. To obtain maximum throughput, application software can write to certain Special Function Register (SFR) bits and cause the MOVX instructions to operate with zero stretch cycles. This default condition is a convenience to existing designs that may not have fast RAM in place. Even in high-speed systems, it may not be necessary or desirable to perform data accesses at full speed. Additionally, there are a variety of memory mapped peripherals such as LCD displays or UARTs that are not fast enough to keep up with the full speed high-speed micro. This flexibility allows the user to trade some performance for slower data RAMs if so desired. For the discussion that follows, a worst case timing scenario of zero stretch cycles will be assumed.

For maximum performance, i.e., with a zero stretch cycle data memory access programmed into the processor, a MOVX instruction requires two machine cycles. The fetch of the instruction takes one machine cycle leaving one machine cycle for the memory read or write. In the analysis of the data memory's timing requirements that follows, it will be assumed that the recommendations of Table 3 have been followed. Specifically, this means that an "F" family latch is used for CPU clock frequencies greater than 19.8 MHz, an "AC" family latch is used for frequencies greater than 16.8 MHz, and an "HC" family latch is used for lower frequencies.

Through analysis and a survey of memory products[2], it can be determined that four SRAM timing parameters are necessary and sufficient to meet the processor's timing requirements for most situations. These parameters and their values for various speed grades are shown in Table 4. During a data read operation, the processor expects the time from an address change until valid data is available to be 71 ns (t_{AVDV1}= $3t_{CLCL}$-20) or less. If the propagation delay from D to Q of an F373 latch (8 ns) is subtracted from this parameter, you obtain a memory address access (t_{AA}) requirement of 63 ns. Also for a data read operation, the time from the $\overline{RD}$ signal going low until valid data is received from the memory device must be 41 ns (t_{RLDV} = $2t_{CLCL}$ - 20) or less. Since the processor's $\overline{RD}$ signal is tied to the memory's $\overline{OE}$ pin, the memory must have an output enable access time (t_{OE}) of less than 41 ns. After the processor has read the data, the SRAM must relinquish the bus within 25 ns (t_{RHDZ} = t_{CLCL} - 5). This dictates that the SRAM parameter t_{OHZ} be less than 25 ns. For a write, the processor will provide a minimum write pulse of 56 ns (t_{WLWH} = 2 t_{CLCL} - 5), which is equal to the minimum required write pulse width (t_{WP}) of the SRAM. On the basis of these four calculated parameters and assumed SRAM speeds shown in Table 4, the appropriate speed device may be determined for a number of different clock frequencies. A summary of the recommended RAM speeds is given in Table 5. It should be noted that the critical timing parameter is not always the access time. Because of the high speed of the processor and variations in memory parameter relationships, all four parameters must be checked for any specific clock speed.

SRAM PARAMETERS Table 4

t_{AA} (ns)	t_{OE} (ns)	t_{OHZ} (ns)	t_{WP} (ns)
35	20	15	25
55	30	25	35
70	35	30	45
80	35	30	60
100	50	35	60
120	60	45	70
150	55	40	90
170	80	35	120
200	100	35	150

RECOMMENDED RAM SPEEDS Table 5

CLOCK (MHz)	LATCH	MEMORY SPEED (zero stretch)	MEMORY SPEED (one stretch)
33.0	F373	55 ns	150 ns
29.4912	F373	55 ns	170 ns
25.0	F373	80 ns	170 ns
22.1184	F373	100 ns	200 ns
20.0	F373	120 ns	200 ns
19.8	AC373	120 ns	200 ns
18.432	AC373	120 ns	200 ns
16.8	HC373	120 ns	200 ns
16.0	HC373	120 ns	200 ns
14.746	HC373	120 ns	200 ns
14.318	HC373	150 ns	200 ns
12	HC373	170 ns	200 ns
11.059	HC373	200 ns	200 ns
7.37	HC373	200 ns	200 ns
1.8432 and below	HC373	200 ns	200 ns

[2] Memory data books from Dallas Semiconductor 1992-93, Fujitsu 1990, Hitachi #M18, Micron 1992, Mosel 1991-92, NEC 1989, Sony 1991 were surveyed for suitable SRAM products.

ADDITIONAL CONSIDERATIONS

All of the timing calculations used in this application note are based on equations found in the DS87C520 data sheet. These specifications assume an approximately equal capacitive load on the signals specified. If the configuration of Figure 1 is used, this is achieved. If, however, any signal is connected to additional loads, then the capacitive loading including the additional devices should be evaluated. If there is a significant difference, additional margins should be used in the critical path analysis, and appropriate memory speeds selected. For older or otherwise unconventional SRAM devices, it may be wise to confirm other important timing parameters (such as data setup before write active). However, on the devices surveyed, meeting the four parameters discussed above will qualify the device for use.

EQUATION SUMMARY

For the user who wishes to calculate the memory speed requirements using a crystal frequency not shown in the preceding tables, the following equations provide a concise summary of the information needed.

EPROM Equations

$\overline{\text{PSEN}}$ Access	Address Access	Bus Release
$t_{OE} = t_{PLIV}$	$t_{ACC} = t_{AVIV}$ - latch delay	$t_{DF} = t_{PXIZ}$
$= 2t_{CLCL} - 20$	$= 3t_{CLCL} - 20$ - latch delay (same for RAM)	$= t_{CLCL} - 5$

RAM Equations

RAM Equations

Read Access	Write Pulse	Bus Release
$t_{OE} = t_{RLDV}$	$t_{WP} = t_{WLWH}$	$t_{OHZ} = t_{RHDZ}$
(zero stretch)	(zero stretch)	(zero stretch)
$= 2t_{CLCL} - 20$	$= 2t_{CLCL} - 5$	$= t_{CLCL} - 5$
(one stretch)	(one stretch)	(one stretch)
$= 4t_{CLCL} - 20$	$= 4t_{CLCL} - 10$	$= 2t_{CLCL} - 5$