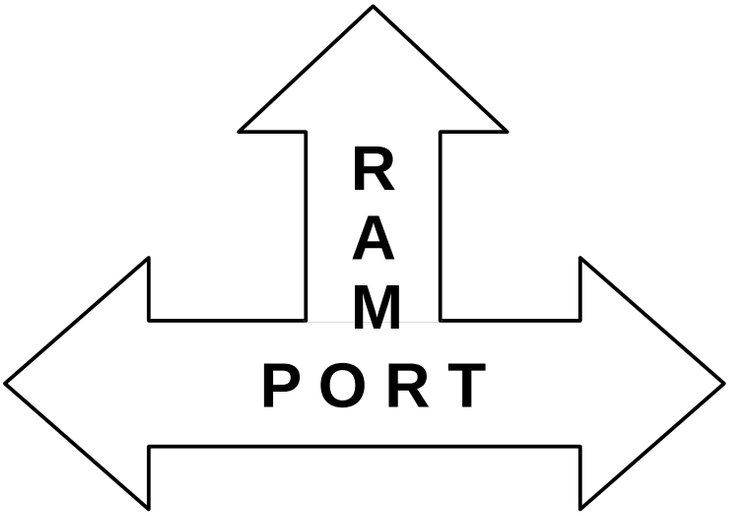
DALLAS SEMICONDUCTOR

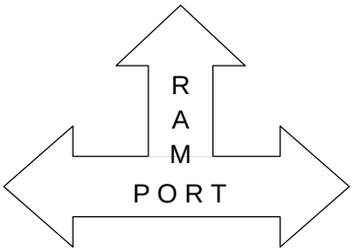
Application Note 61
RAMport



RAMport – 2K X 8 NV SRAM AND MORE

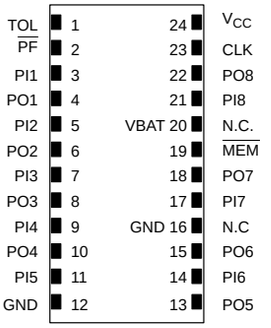
The RAMport memory developed by Dallas Semiconductor was designed to be connected to microcontrollers without robbing the device of valuable port pins. The name “RAMport” was chosen for the DS1381 to try to communicate this advantage to potential users (see Figure 1). Even if the name is effective in conveying this message, the overall capability of the device and the diversity of applications remains concealed.

DS1381 Figure 1



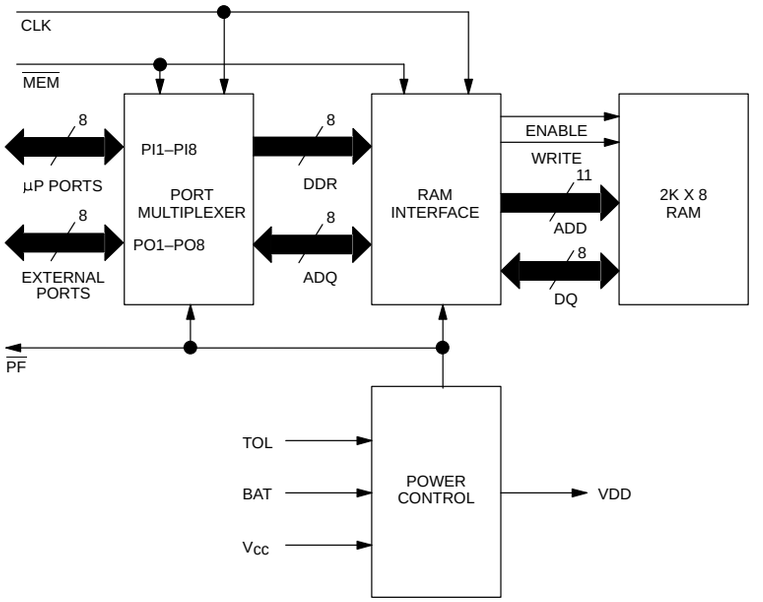
The DS1381 RAMport is a bytewide memory that uses a multiplexed address and data bus. The obvious disadvantage with this scheme is reduced performance because the address and data information is sent sequentially. The equally obvious advantage is reduced pin count (see Figure 2). The multiplexing scheme used with the DS1381 requires only 8 pins for address and data. The address is transferred to the device in two subsequent cycles. The first address transfer consists of A8 through A10 along with read or write command information. The second address transfer contains the low–order address bits and is followed by a third transfer which is data. Since the read or write command is transferred as part of the address, the need for read and write control signals is also eliminated, reducing control signal requirements to only two pins: memory and clock. The memory and clock signals direct data transfer to and from the memory and also command and control eight port input/outputs which are not found on conventional memories (see Figure 3). The total pin count for memory interface and port input/output plus V_{CC} and ground amounts to 20 pins. This leaves four pins for the special purpose of providing nonvolatility. Two pins provide for a direct connection to a data retention energy cell. These pins do not go outside the package, but are internally connected to a lithium coin cell. Since this connection is made with 2 of the 24 pins on a standard dual in line package, cost savings is achieved when compared to alternate interconnect systems or special lead frames. Finally, the DS1381 provides an output when power fail occurs which can be used to interrupt the processor, and a separate pin provides selection of the power fail detection point at 5% or 10% of the power supply voltage. The end result is a low–cost 24–pin 0.6” DIP which offers an I/O port and a power fail controller as a bonus.

DS1381 PIN INFORMATION Figure 2



PIN NAME	DESCRIPTION
$\overline{PF}$	POWER FAIL OUTPUT
PI1–PI8	PORT INPUTS (µP PORTS)
PO1–PO8	PORT OUTPUTS (EXTERNAL PORTS)
GND	GROUND
V_{CC}	+5 VOLTS
CLK	CLOCK
$\overline{MEM}$	MEMORY SELECT
N.C.	NO CONNECTION

DS1381 FUNCTIONAL BLOCK DIAGRAM Figure 3



REDUCING TO PRACTICAL – MICROCONTROLLER INTERFACE

As mentioned, the DS1381 was designed to offer the microcontroller user some external nonvolatile memory that does not consume all of the valuable port pins. When using the DS1381 with a microcontroller, the interconnect system is simple and straightforward. Eight port pins of the microcontroller connect directly to the eight input port pins (PI1 – PI8) of the DS1381 (see Figure 3). These port pins are reproduced at the port output pins (PO1 – PO8). During operation, when no memory transfer is taking place, the DS1381 port output pins look exactly like the eight microprocessor port pins with the only addition being a small series impedance. Two other port pins of the microprocessor are required to control the DS1381, namely CLOCK and $\overline{\text{MEMORY}}$. Since these port pins must be dedicated to control, they are not reproduced by the DS1381. The $\overline{\text{MEMORY}}$ and CLOCK signals must be generated using software within the microcontroller to establish the proper signal levels and timing relationships. The function of these two controls is to direct data to and from memory or to the data direction register within the DS1381. When data is being transferred to and from the DS1381, the port outputs are latched or become high impedance depending on their assigned function. More detailed information on the control signals is furnished in the DS1381 data sheet.

MICROPROCESSOR INTERFACE USING DS1381 MEMORY

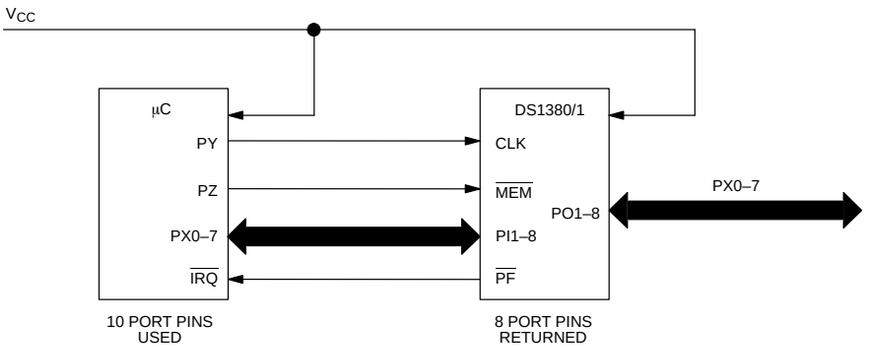
While the hardware interface between the DS1381 and a microcontroller is straightforward, the interface to a microprocessor is also simple, although not as obvious. Only the 2K X 8 nonvolatile memory and power fail controller features are useful in this application (see Figure 5). The key to interfacing the DS1381 to a microprocessor is to use only the data bus for both address and data. Since only the memory is to be used, the $\overline{\text{MEMORY}}$ signal should be grounded. This connection fixes the PO1 – PO8 pins to remain in a status as dictated by the data bus and the DS1381 data direction register at the time that the $\overline{\text{MEMORY}}$ signal is grounded. Because it is unlikely that these pins contain any useful information under this condition (although some type of programming mode might be implemented to make these outputs useful) these pins should be left unconnected. With the $\overline{\text{MEMORY}}$ pin grounded, the clock input becomes analogous to the chip enable or chip select on a standard bytewide memory. The clock signal can be easily derived with a decoder from selected address lines which place the DS1381 properly in the memory map. To achieve proper timing (setup and hold times) the decode must be gated by a microprocessor control signal. The names and purpose of usable control signals vary with the type of microprocessor used. Howev-

er, status signals, address latch enable, memory request, address strobe, and data strobe usually provide the proper timing relationship with respect to address and data for gating the decoder. The microprocessor and DS1381 data sheets should be consulted for exact timing details. Since only the data bus is used for both address and data, three separate memory cycles must be used to read or write each byte of data. However, this inconvenience is often a small price to pay for hiding a 2K X 8 of nonvolatile RAM in as small as one I/O or memory address space. An additional feature that standard memory does not provide is the power fail interrupt output.

IN CONCLUSION

The DS1381 is primarily tailored for use with microcontrollers. In microcontroller applications, the DS1381 provides an inexpensive nonvolatile RAM without using valuable port pins. In microprocessor applications, 2K X 8 of nonvolatile RAM is easily interfaced to a system with minimum impact on memory space by using the data bus for both address and data. Because of the multiplexed address/data bus, pin count and cost are kept to a minimum while additional and useful features are provided which are not found on standard memories. While the multiple uses of the RAMport are difficult to convey to potential users with only a name, closer inspection of the device reveals an economical, special–purpose nonvolatile memory with many microprocessor and microcontroller applications.

MICROCONTROLLER INTERFACE Figure 4



MICROPROCESSOR INTERFACE USING DS1380 2K X 8 NV RAM ONLY Figure 5