Interfacing the TMS320C54x Buffered Serial Ports to the DS21x5y Single Chip Transceivers (SCT)

I. Introduction

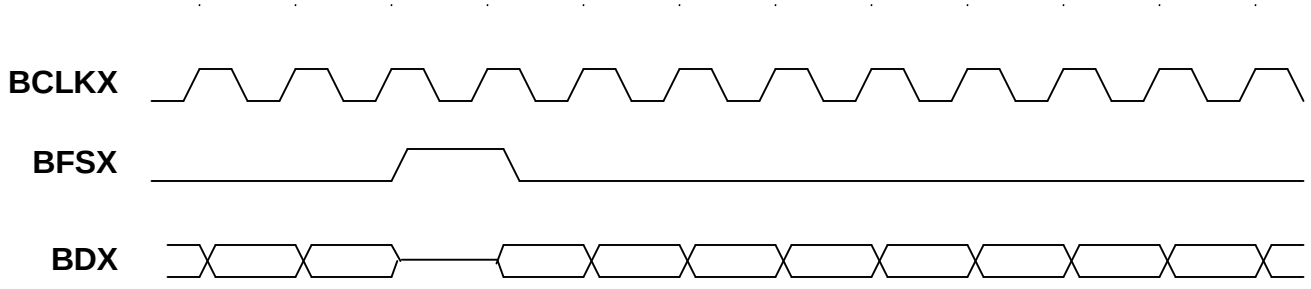
The TMS320c54x family of devices are fixed-point digital signal processors (DSP) offered by Texas Instruments. This family, referred as '54x, implements several types of serial port operations. The buffered serial port, commonly referred to as the BSP, provide full-duplex communication capabilities with either a T1 or an E1 data structure, due to these ports supporting the use of frame synchronization strobes. The BSP allows transfers of 8, 10-, 12-, or 16-bit data packets. In the continuous mode, the frame synchronization pulse occurs when the data transmission (or reception) is initiated. Any further pulses applied to this input during the reception or transmission of data packets will cause a receive or transmit abort condition, and one packet of data will be lost. In the burst mode, data packets are directed by a frame synchronization pulse every packet. To ensure that each timeslot of the T1 or E1 data stream is properly transferred between the '54x and the DS21x5y SCT, this application note outlines how to interconnect these two IC's for operation of the '54x in the both the continuous mode and the burst mode.

II. TMS320C54x BSP Continuous Mode Operation

The continuous mode of operation in the '54x is selected by setting FSM=0 in the Serial Port Control (SPC) register. The use of the Autobuffering Unit (ABU) is outlined here, as this will allow at least 125 µsecs between Buffer-Full/Buffer Empty interrupts to the CPU. The minimal buffer size for either transmit or receive path would be 48 bytes, since there are 24 8-bit timeslots per T1 frame (32 for E1). Please refer to *Section 9.1 Introduction to the Serial Ports*, of the TMS320C54x Reference Set, *Volume 1: CPU and Peripherals* for complete initialization and descriptions of BSP and ABU operations.

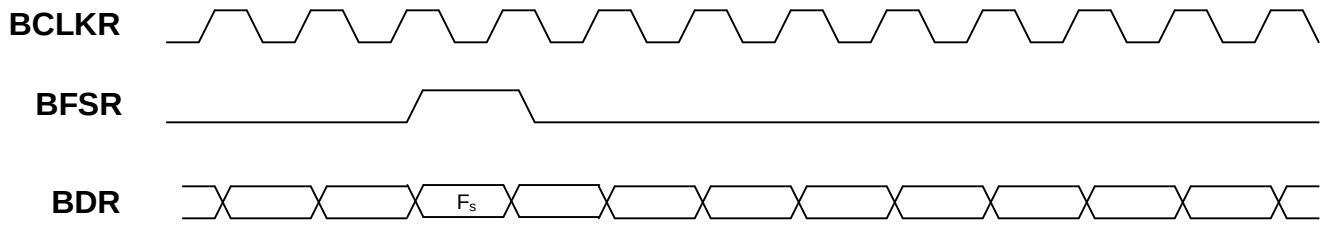
Continuous Mode transmit timing is shown in Figure 1 below.

Continuous Mode Transmit Timing (External Frame) - Figure 1



Note that in Figure 1, the Transmit synchronization pulse occurs at the location where the DS21x5y inserts a frame bit. Since the DS21x5y will internally generate the frame bit, and the '54x is not using the bit position where a frame synchronization pulse occurs, this allows a glueless interface between these two devices on this signal.

Continuous Mode Receive Timing (External Frame) - Figure 2



Note that in Figure 2, the Receive synchronization pulse occurs at the location where the DS21x5y located a frame bit in the receive stream. Since the '54x sees this as a FSR pulse reception during a *Receive in Progress* condition, the current receive buffer load will be aborted, and start over with the next received bit. This is acceptable, since the FSR did not occur during a valid bit condition (occurring during the framing bit, or F_{bit} position. The TMS320C54x will start clocking into the RSR with the first bit of the timeslot following the F_{bit}. This allows a glueless interface between these two devices on this signal.

TMS320C54x BSP Continuous Mode and the DS21x5y SCT Signal Descriptions

The table below describes how the TMS320C54x BSP connects to the DS21x5y SCT when operating the TMS320C54x in the continuous mode. A short description of each signal is given (note: all descriptions for the TMS320C54x device are taken from the data sheet entitled, *TMS320C54x,TMS320LC54x, TMS320VC54x Fixed-Point Digital Signal Processors).*

TMS320C54x BSP Signal	DS21x5y SCT Signal
BCLKR - Buffered Receive Clock Input only. External clock signal for clocking data from the Buffered Data-Receive (BDR) pin into the buffered serial port receive shift registers (RSRs).	**RCLK -** Receive Clock Output only. Either a 1.544 MHz (DS21x52), or a 2.048 MHz (DS21x54) clock that is used to clock data through the receive-side framer. (note: to ensure that this clock is recovered from the LIU's receive data path, the RCLKO pin should be tied to the RCLKI pin.
BDR - Buffered Data Receive Input only. Buffered serial receive data, clocked directly into the serial port receive shift registers (RSRs).	**RSER -** Receive Serial Data Output only. Received NRZ data. Updated on the rising edges of RCLK when the receive-side elastic store is disabled. Updated on the rising edge of RSYSCLK when the elastic store is enabled.
BFSR - Buffered Frame Synchronization Receive Input only. Frame synchronization pulse for the receive input. The falling edge of the BFSR pulse initiates the data-receive process, beginning the clocking of data into the RSR.	**RSYNC -** Receive Sync Configured for an output. An extracted pulse one RCLK wide, is output when an entire T1 (DS21x52) or an entire E1 (DS21x54) frame is beginning.
BCLKX - Buffered Transmit Clock Configured for an input[1]. Clock signal for clocking data from the serial port transmit shift register (XSR) to the Buffered Data Transmit	**TCLK -** Transmit Clock Input only[1]. Either a 1.544 MHz (DS21x52), or a 2.048 MHz (DS21x54) clock that is used to clock data through the transmit-side framer. (note: to

(BDX) pin. BCLKX is configured as an input by clearing the MCM bit in the serial port control register (SPCR).	ensure that this clock is recovered from the LIU's receive data path, the LIUC pin should be tied high.
BDX - Buffered Data Transmit Configured for an output. Buffered serial-port-transmit output. Serial data is transmitted from the serial port transmit shift register (XSR) through this pin. The EMU1/OFF signal should be set to 1, therefore preventing the BDX pin from going into a high-impedance state when not transmitting.	**TSER** - Transmit Serial Data Input only. Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit-side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit-side elastic store is enabled.
BFSX - Buffered Frame Synchronization Transmit Configured for an input[2]. Frame synchronization pulse for the transmit output. The falling edge initiates the data-transmit process, beginning the clocking of the XSR. Following reset, the BFSX pin's default operating condition is that of an input.	**TSYNC** - Transmit Sync Configured for an output[2]. A single TCLK wide pulse on this pin will establish a frame boundary on the transmit side.

Notes:

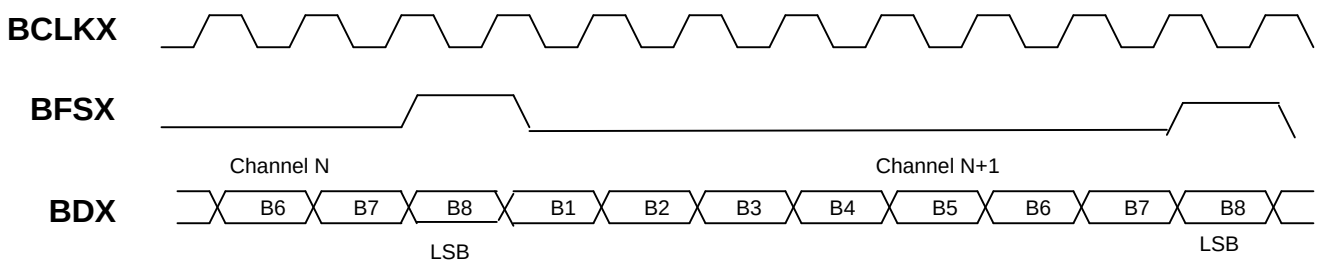
1. The timing options for the BCLKX signal on theTMS320C54x family are limited to either taking the clock directly from the BCLKX pin (MCM=0 in the SPC register), or from a clock generated from an on-chip clock source.

2. Normally the device attached to the DS21x5y will supply the TSYNC signal. But in this case the TMS320C54x family will operate in the continuous mode, and therefore would not output frame synchronization signals compatible with either a T1 or an E1 frame boundary. Therefore, the DS21x5y should be the source of this signal.

III. TMS320C54x BSP Burst Mode Operation using T1 Frames

The burst mode of operation in the '54x is selected by setting FSM=1 in the Serial Port Control (SPC) register. Like in the continuous mode of operation, the use of the Autobuffering Unit (ABU) allows at least 125 µsecs between Buffer-Full/Buffer Empty interrupts to the CPU. The minimal buffer size for either transmit or receive path would be 48 bytes, since there are 24 8-bit timeslots per T1 frame (32 for E1). Please refer to *Section 9.1 Introduction to the Serial Ports,* of the TMS320C54x Reference Set, *Volume 1: CPU and Peripherals* for complete initialization and descriptions of BSP and ABU operations.

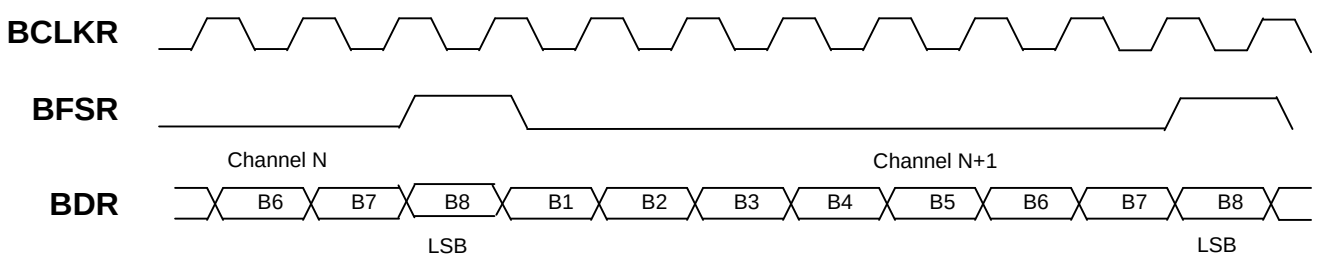
Burst Mode Transmit Timing (External Frame) - Figure 3



Note that in Figure 3, the Transmit synchronization pulse BFSX occurs at the LSB of each timeslot of the DS21x52 transmit datastream. The requirements needed for this signal is very much like the TCHCLK

signal of the DS21x5y, with the exception of the 24th timeslot. This exception will cause some external logic requirements to be implemented (see below).

Burst Mode Receive Timing (External Frame) - Figure 4



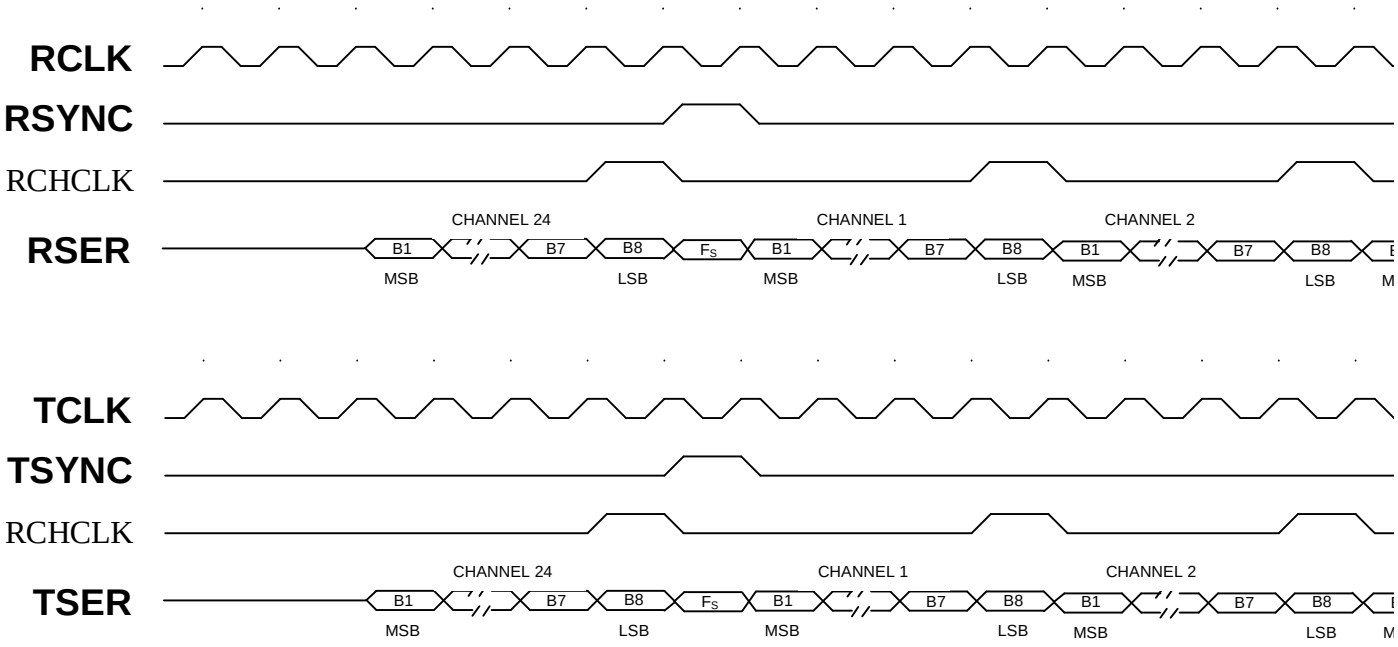
Note that in Figure 4, the Receive synchronization pulse BFSR occurs at the LSB of each timeslot of the DS21x52 transmit datastream. The requirements needed for this signal is very much like the RCHCLK signal of the DS21x5y, with the exception of the 24th timeslot. Like the transmit side, this exception will cause some external logic requirements to be implemented to ensure proper operation.

External Logic Requirements for Burst Mode using T1 frames

Using the TMS320C54x BSP's with the DS21x52 is not glueless, specifically if the user clocks data out of the SCT device at a T1 frame rate (1.544 MHz). This is due to the insertion of the framing bit between the 24th timeslot of the previous T1 frame and the 1st timeslot of the current T1 frame. If the TCHCLK or the RCHCLK signal is directly interconnected into the BFSX or the BFSR signals, then the 1st T1 frame of the current frame will contain errors. Specifically, the first timeslot's LSB will be the framing bit, and the MSB will be B7 of the timeslot.

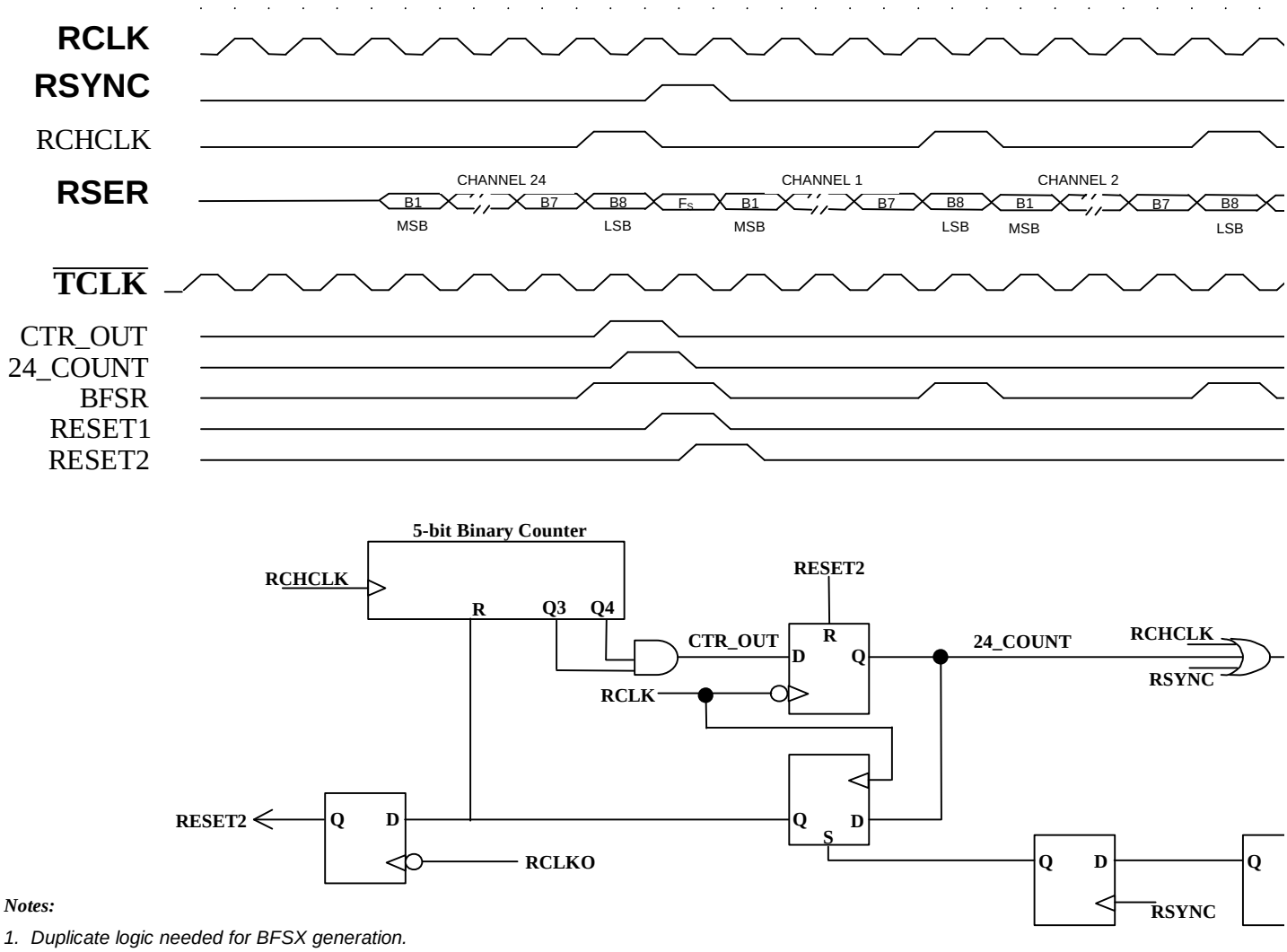
Figure 5 outlines the timing strobes available on the DS21x52 SCT when clocking data out at 1.544 MHz (T1) data rates. These signals will be used to generate the proper timing signals outlined in Figure 6. Figure 6 outlines the proper burst mode timing requirements needed to ensure proper operation of the TMS320C54x with the DS21x52 SCT using T1 timing, along with the external logic needed to implement the proper timing requirements.

Timing Strobes Available on the DS21x52 SCT - 1.544 MHz (T1) Timing - Figure 5



Generating BFSR[1] for Proper Burst Mode Operation of the TMS320C54x - 1.544 MHz

Figure 6



Notes:

1. Duplicate logic needed for BFSX generation.

IV. TMS320C54x BSP Burst Mode Operation using a 2.048 MHz Systems Clock

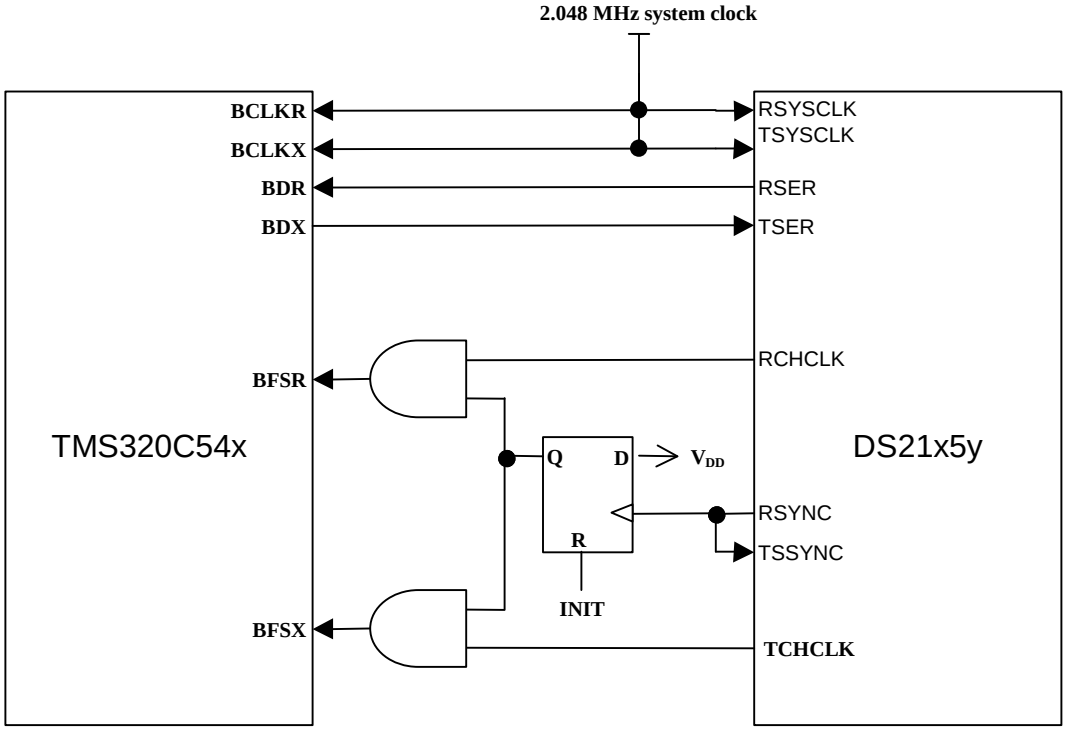
Another option which uses less external logic interfacing from the TMS320C54x to the DS21x5y SCT's in burst mode would be using a 2.048 MHz clock into the TSYSCLK and RSYSCLK inputs of the SCT's, and enabling the elastic stores. The SCT will then do a rate conversion between the T1 line rate and the 2.048MHz system clock. This is accomplished internal to the SCT by forcing timeslots 0,4,8,12,16,20,24, and 28 to all ones on the receive side, or ignoring these same timeslots on the transmit path. The F-bit will be deleted (unless selected to pass through in the LSB of timeslot 0).

In the case where the elastic store's system clock is locked to its network clock, the elastic store's minimum delay mode can be used. RSYNC would then be configured as an output and then connected to TSSYNC. Since both the transmit and the receive path are frequency-locked, then RSYSCLK and TSYSCLK can be connected together.

Also, with a 2.048 MHz system clock, the TCHCLK signal of the DS21x5y will be connected directly to the BFSX signal of the TMS320C54x. Likewise, the RCHCLK signal of the DS21x5y will be connected directly to the BFSR signal of the TMS320C54x. Very minimal external logic would then be required to synchronize these signals to the RSYNC and TSSYNC signals during initialization.

Figure 7 shows the block diagram of how the TMS320C54x and the DS21x5y SCT can be connected when operating with the elastic stores enabled and configured for the minimal delay mode and using a 2.048 MHz systems clock.

Block Diagram of the TMS320C54x and the DS21x5y SCT using a 2.048 MHz System Clock (Requires the 2.048 MHz System Clock to be Locked to the Network Clock) - Figure 7



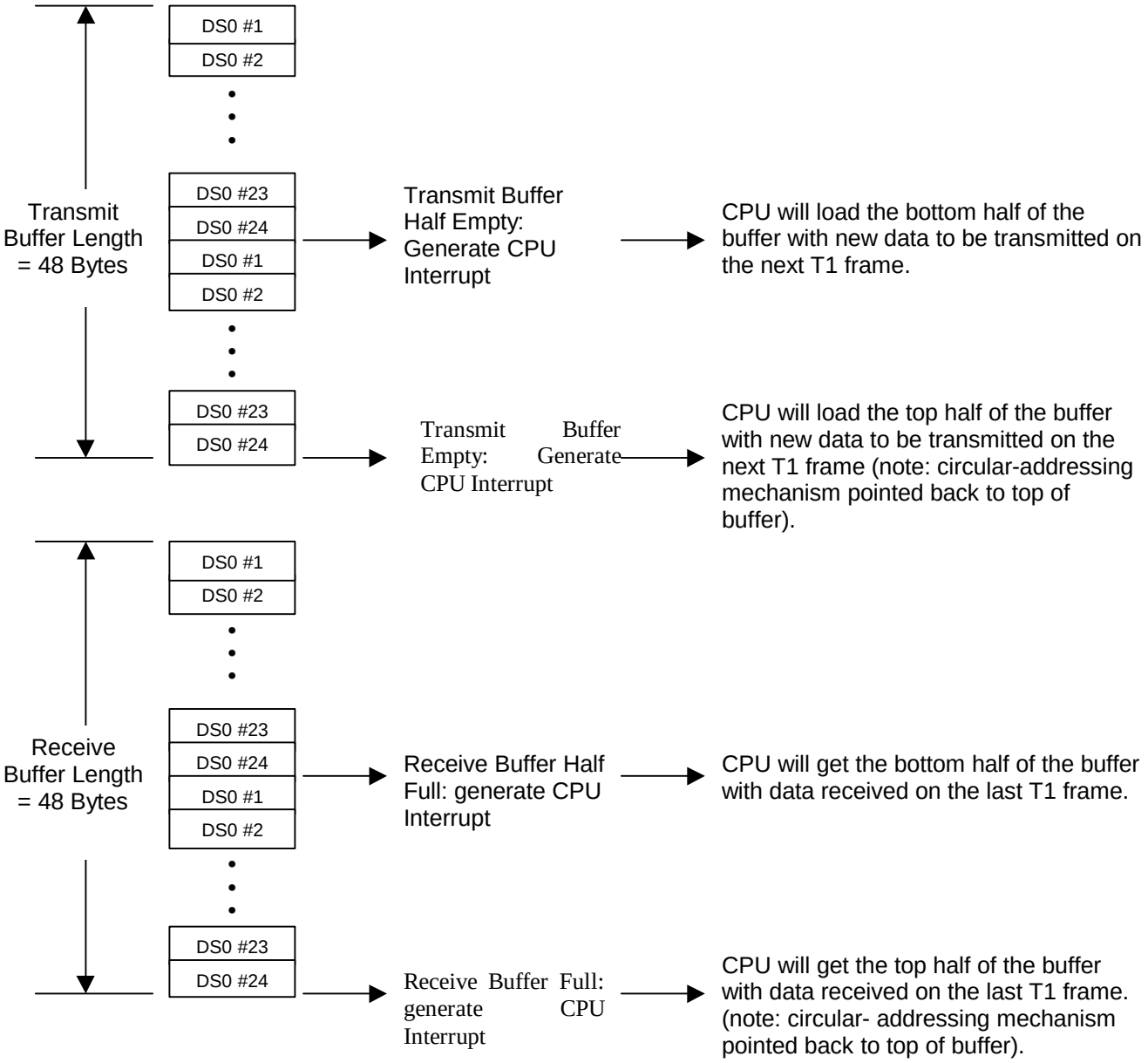
V. Autobuffering Unit (ABU) T1/E1 Operation

The ABU will implement CPU interrupts when its' transmit and receive buffers are halfway or entirely filled or emptied. By checking either the RH or the XH bit in the BSP Control Extension (BSPCE) Register, the CPU can operate on the data in the opposite half of the buffer being operated on. The circular addressing mechanism will automatically update the buffer pointers to ensure that once the end of the buffer is reached, the next reception will occur at the beginning of the buffer.

Consider the case where the input into the BSP is a T1 datastream. Initialization of the circular addressing mechanism would begin by loading both BKX/R with the exact size of the desired buffer (each buffer in this case being two T1 frames, or 48 bytes). Completion of the initialization would end with the base address values of these two 48-byte buffers within the 2K word block dedicated to this operation along with the initial starting address within the buffer (normally 00H). Loading would be into the ARX/R registers. Upon starting the ABU, an interrupt will occur when either of the buffers are half full (or empty). At this point the CPU should see which buffer caused the interrupt, and then see if the interrupt was caused by a half-full (empty) or full (empty) buffer. The CPU would then service the data in the portion of the buffer which is opposite of the buffer currently being serviced by the ABU. This allows the CPU to be working on the previous T1 frame of data. . Figure 8 outlines this entire procedure when using a T1 datastream.

When interfacing to an E1 datastream, the buffer sizes will now be 64 bytes, since an E1 frame consists of 32 timeslots, each with a single byte of data.

Autobuffering Unit Operation - Figure 8



References used:

- *TMS320C54x,TMS320LC54x,TMS320VC54x Fixed-Point Digital Signal Processors, Literature number SPRS039B - February 1996 - Revised February 1998, Texas Instruments, Inc.*
- *TMS320C54x DSP Reference Set - Volume 1: CPU and Peripherals, Literature number SPRU131F - April 1999, Texas Instruments, Inc.*
- *3.3V DS21352 and 5V DS21552 T1 Single Chip Transceivers (SCT), 121098, Dallas Semiconductor*