Application Note 358
DS3134 Application Note: PCI Bus Utilization

OVERVIEW
The DS3134 accesses the PCI Bus to obtain and store HDLC packets as they are sent and received. This Application Note details how to calculate how much of the available bus bandwidth will be required by the DS3134 to operate properly. Hopefully, with the information provided in the Application Note, the user can modify the numbers to exactly fit their particular application. Throughout the Application Note, the variables shown in Table 1 will be used.

Definition of Variables Table 1

Variable	Definition	Valid Range
B	the average number of packets processed before the Host updatesthe Receive Free Queue & Transmit Pending Queue or reads the Receive Done Queue & Transmit Done Queue	1, 2, 3, ...
C	the average number of bus cycles required per packet	1, 2, 3, ...
D	the number of bus cycles needed for data to be transferred	1, 2, 3, ...
P	the size of the Packet in bytes (always 64 in this Application Note)	64
R	the average number of bus cycles added due to latency in RAMaccess	0, 1, 2, ...
X	the average number of bus accesses required to send/obtainpacket data to/from the data buffers	1, 2, 3, ...

TYPES OF BUS ACCESSES
There are four types of bus accesses that are performed either by the DS3134 or by the Host to support the DMA in the DS3134. In the following descriptions, the variable D is defined as the number of data cycles and the variable R is defined as the number of bus cycles needed due to RAM access latency.

Type 1: Burst Read by the DMA from the Host RAM
The total number of bus cycles required when the DMA burst reads from the Host RAM is [3+R+D]. This equation was derived from Figure 9.1B of the DS3134 Data Sheet and as shown below.

Cycle	# Cycles Required
Address Cycle	1
Turn Around Cycle	1
RAM Access Latency Cycles	R
Data Cycles	D
Turn Around Cycles	1

Type 2: Burst Write by the DMA to the Host RAM

The total number of bus cycles required when the DMA burst writes to the Host RAM is [2+R+D]. This equation was derived from Figure 9.1C of the DS3134 Data Sheet and as shown below.

Cycle	# Cycles Required
Address Cycle	1
Turn Around Cycle	1
RAM Access Latency Cycles	R
Data Cycles	D
Turn Around Cycles	1

Type 3: Write by the Host to the DS3134

The total number of bus cycles required when the Host writes to the DS3134 is 7.

Type 4: Read by the Host to the DS3134

The total number of bus cycles required when the Host reads from the DS3134 is 7.

Note: For Type 3 and 4 the 7 cycle is inherent to Chateau and can not be changed.

NUMBER OF BUS CYCLES NEEDED PER PACKET

In order to calculate bus utilization, the number of bus cycles required must be known. To obtain this number, several assumptions have been made and are listed in Table 2. Figure 1 shows the standard sequence that the Host and DMA will follow for each packet received or transmitted. From Figure 1 we can create a formula to calculate the average number of bus cycles required per packet which is the variable C.

Receive Side

Cr = [(3+R+24)/12] + [(P/4)+(2+R)X] + [2+R+3] + [(2+R+6)/6] + [4(7/B)]

Transmit Side

Ct = [(3+R+12)/12] + [2+R+1] + [3+R+4] + [(P/4)+(3+R)X] + [(2+R+6)/6] + [4(7/B)]

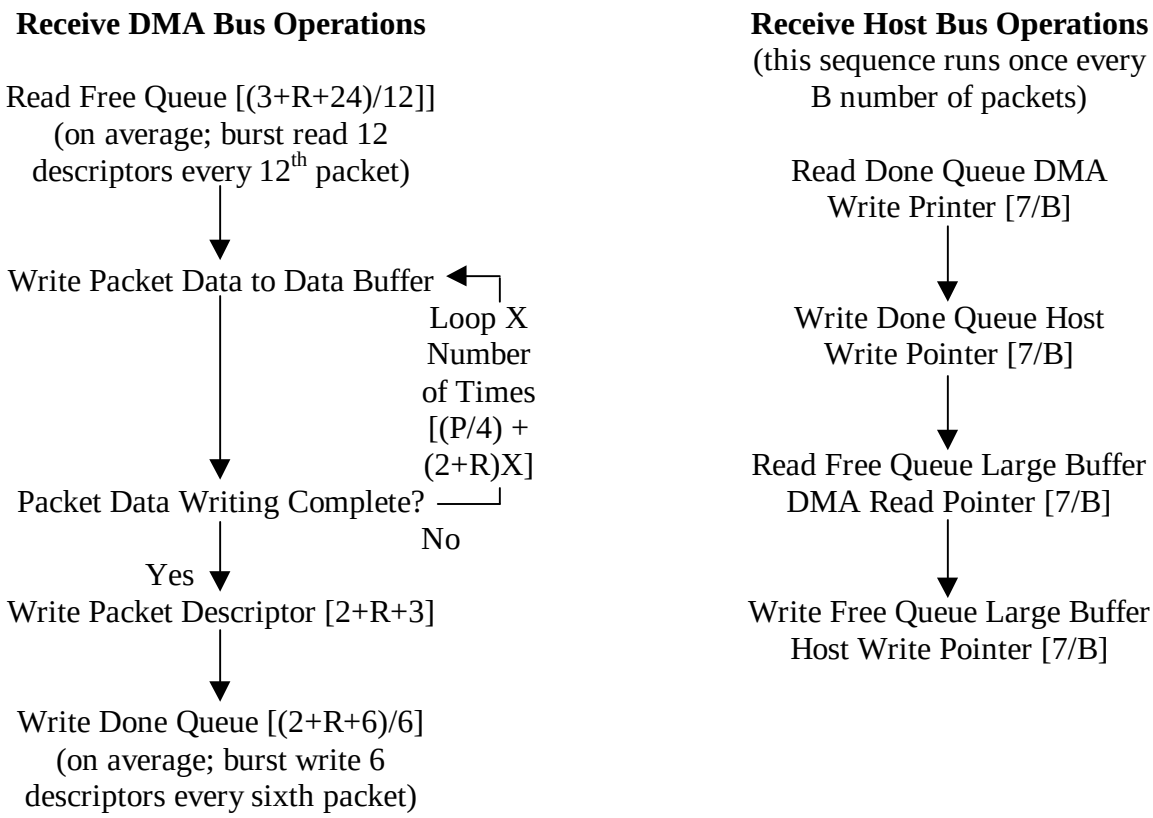
Total Formula

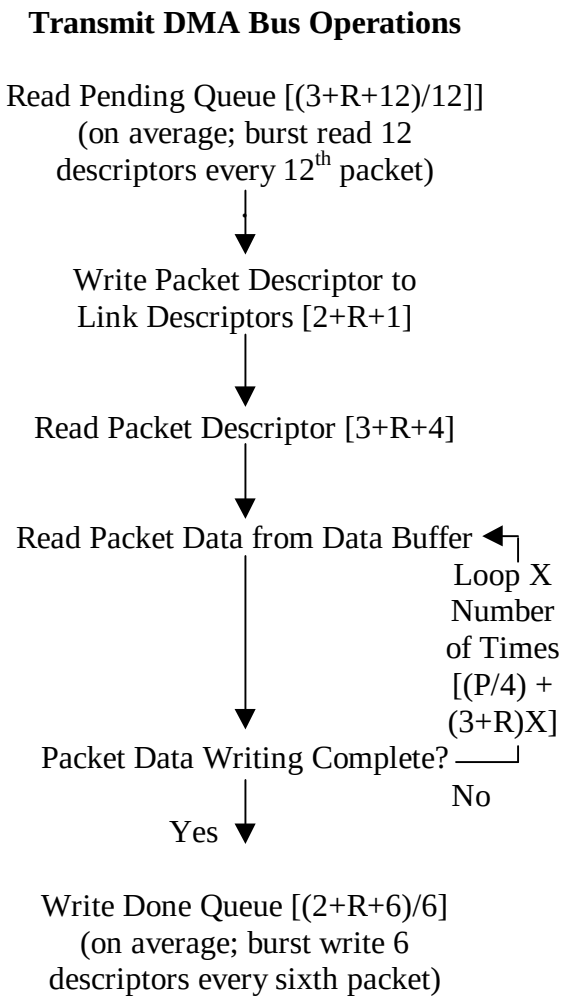
C = 21.16 + 3.5R + 0.5P + 56/B + (5 + 2R)X

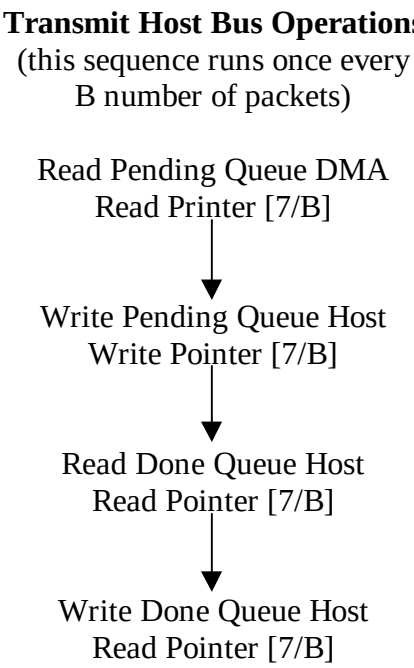
Assumptions Made to Calculate the Number of Bus Cycles Required Per Packet Table 2

- All packets are 64 bytes (seen as worse case)
- The FCS of the HDLC packet is not transferred to or from the PCI Bus
- On the receive side, only Large Buffers are used (small buffers are disabled)
- The receive DMA will burst read the Free Queue and burst write to the Done Queue
- The transmit DMA will burst read the Pending Queue and burst write the Done Queue
- All packets fit within a single buffer (i.e. only one descriptor); reasonable since packets are 64 bytes
- All physical layer links are filled with packets, no idle codes sent or received
- Interrupt routines and overhead (like accesses to the Local Bus) are not considered

Per Packet Bus Cycle Flowchart Figure 1







BUS UTILIZATION

With the known number of bus cycles required per packet, the bus utilization can be calculated. Bus utilization is defined as the number of bus cycles required by the DS3134 in a one second period divided by the total number of bus cycles available in one second which for the purposes of this Application Note will be 33,000,000 since the PCI clock rate is assumed to be 33MHz. The following two formulas can be used to calculate bus utilization.

# of Bus Cycles Required per second	=	# Packets Per Second	*	# Bus Cycles Needed Per Packet [C]	*	# Channels

Bus Utilization	=	# of Bus Cycles Required Per Second	/	33,000,000

Below is some examples of bus utilization. Three cases were chosen. In each case, it was assumed that all the incoming and outgoing packets were 64 bytes long (P = 64) and that the Host would update and read the queues used by the DMA on the DS3134 on average, every eight packets (B = 8). In each case there are two scenarios. In scenario A, the Host RAM is tightly coupled and on average only adds one bus cycle for each access. In scenario B, the Host RAM is not tightly coupled and on average, adds seven bus cycles for each access. These three examples can be modified to fit the exact application.

DESCRIPTION OF EXAMPLES Table 3

Case#	Description	# of Packets Per Second
Case 1	256 channels at 64 Kbps	125
Case 2	64 clear channel T1	3000
Case 3	2 clear channel T3	84000

EXAMPLES OF BUS UTILIZATION Table 4

Case	R	P	B	X	# of Bus Cycles Required Per Packet [C]	Bus Utilization
1A	1	64	8	3	84.7	8.2%
1B	4	64	8	3	113.2	11.0%
2A	1	64	8	1	70.7	41.1%
2B	4	64	8	1	87.2	50.7%
3A	1	64	8	1	70.7	36.0%
3B	4	64	8	1	87.2	44.4%

Assumption: B = 8, cases #A R = 1 and cases #B R = 4.

Notes:

Case 1

1. There is 1024 block in the Chateau internal FIFO, each block is four word (16 bytes). With 256 channels loaded each channel can only be assigned to 1024/256 = four blocks (4x16 = 64 bytes)/ ch.

2. Since each FIFO block is 64 bytes, therefore a 64 bytes packet in the FIFO can be fill or empty in two bus access. For worst case assumptions, we use three in this example.

Case 2

1. There is 64 channel in case two, therefore the block size in the FIFO can be 1024/64 = 16 (16 x 16 = 256 bytes)/ch.

2. Each FIFO block size is 256 bytes; therefore a 64 bytes packet in the FIFO can be fill or empty in one bus access.

Case 3

1. There is 64 channel in case two, therefore the block size in the FIFO can be 1024/2 = 16 (16 x 16 = 256 bytes)/ch.

2. Each FIFO block size is 256 bytes; therefore a 64 bytes packet in the FIFO can be fill or empty in one bus access.

REVISION HISTORY:

VERSION	DATE	CHANGES
1	02/24/98	Original Release.
2	12/2/98	1. Corrected the formulas on page 2 from 4(B/7) to 4(7/B) and from 1.143B to 56/B. 2. Changed R & X values in Table 4 to reflect more realistic values. 3. Corrected minor grammatical errors.
3	03/02/99 Modified by Ming	1. Added borders to tables. 2. Added a few notes to clarify some assumptions and constants. 3. Change the symbol X on page 4 equation to 8.
4		1. Correct typo on page 2 by removing the extra term "+ [2 + R + 3]" from equation Ct.