1.0   INTRODUCTION

This application note highlights the differences between the DS21Q44 and the DS21Q43A Quad E1 Framers. The DS21Q44 is a superset of the DS21Q43A. The DS21Q44 is offered in a 3.3 volt version with 5 volt tolerant I/O. All of the original features of the DS21Q43A (except the Loss of Receive Clock status bit) have been retained and software created for the DS21Q43A is transferable to the DS21Q44 with minimal effort.

2.0   ADDITIONAL FUNCTIONALITY

New Features	Data Sheet Section
• Framer Mode Select (FMS) hardware pin provides DS21Q43A emulation mode	1
• 8.192 MHz clock synthesizer	1 & 3
• Expanded receive and transmit elastic store reset functions	6
• Device identification register	6
• Automatic RAI generation to ETS 300 011 specifications	6
• RCL, RLOS, RRA, and RUA1 alarms now interrupt on change of state	7
• Ability to monitor DS0 channel in both the transmit and receive paths	9
• Additional hardware signaling capability	10
- Receive signaling reinsertion to a backplane multiframe sync	
- Signaling freezing	
• Per–channel loopback capability	11
• Per–channel idle control	11
• HDLC controller	15
- 64 byte buffers	
- Can be used on Sa bits or DS0 channels	
• 8 Mbps interleaved PCM bus operation	16
• JTAG support	17
• 3.3V operation with 5V tolerant I/O	19

3.0 CHANGES IN REGISTER DEFINITIONS

When implementing the new features of the DS21Q44, a priority was placed on preserving the DS21Q43A's register map to facilitate code migration from existing DS21Q43A designs. This section highlights register additions and differences found in the DS21Q44.

3.1 Register Map Comparison

ADDRESS	R/W	DS21Q44 REGISTER NAME	DS21Q43A REGISTER NAME
00	R	RBPV or Code Violation Count 1	Same
01	R	BPV or Code Violation Count 2	Same
02	R	CRC4 Error Count 1 / FAS Error Count 1	Same
03	R	CRC4 Error Count 2	Same
04	R	E–Bit Count 1 / FAS Error Count 2	Same
05	R	E–Bit Count 2	Same
06	R/W	Status 1	Bit Difference
07	R/W	Status 2	Bit Difference
08	R/W	Receive Information	Bit Difference
09	R/W	Test 2	Not Used
0A	-	Not Used	Not Used
0B	-	Not Used	Not Used
0C	-	Not Used	Not Used
0D	-	Not Used	Not Used
0E	-	Not Used	Not Used
0F	R	Device ID	Not Used
10	R/W	Receive Control 1	Same
11	R/W	Receive Control 2	Same
12	R/W	Transmit Control 1	Same
13	R/W	Transmit Control 2	Same
14	R/W	Common Control 1	Same
15	R/W	Test 1	Same
16	R/W	Interrupt Mask 1	Bit Difference
17	R/W	Interrupt Mask 2	Same
18	-	Not Used	Same
19	-	Not Used	Same
1A	R/W	Common Control 2	Bit Difference
1B	R/W	Common Control 3	Bit Difference
1C	R/W	Transmit Sa Bit Control	Same
1D	R/W	Common Control 6	Same
1E	R	Synchronizer Status	Same
1F	R	Receive Non–Align Frame	Same
20	R/W	Transmit Align Frame	Same
21	R/W	Transmit Non-Align Frame	Same
22	R/W	Transmit Channel Blocking 1	Same
23	R/W	Transmit Channel Blocking 2	Same
24	R/W	Transmit Channel Blocking 3	Same
25	R/W	Transmit Channel Blocking 4	Same
26	R/W	Transmit Idle 1	Same

ADDRESS	R/W	DS21Q44 REGISTER NAME	DS21Q43A REGISTER NAME
27	R/W	Transmit Idle 2	Same
28	R/W	Transmit Idle 3	Same
29	R/W	Transmit Idle 4	Same
2A	R/W	Transmit Idle Definition	Same
2B	R/W	Receive Channel Blocking 1	Same
2C	R/W	Receive Channel Blocking 2	Same
2D	R/W	Receive Channel Blocking 3	Same
2E	R/W	Receive Channel Blocking 4	Same
2F	R	Receive Align Frame	Same
30	R	Receive Signaling 1	Same
31	R	Receive Signaling 2	Same
32	R	Receive Signaling 3	Same
33	R	Receive Signaling 4	Same
34	R	Receive Signaling 5	Same
35	R	Receive Signaling 6	Same
36	R	Receive Signaling 7	Same
37	R	Receive Signaling 8	Same
38	R	Receive Signaling 9	Same
39	R	Receive Signaling 10	Same
3A	R	Receive Signaling 11	Same
3B	R	Receive Signaling 12	Same
3C	R	Receive Signaling 13	Same
3D	R	Receive Signaling 14	Same
3E	R	Receive Signaling 15	Same
3F	R	Receive Signaling 16	Same
40	R/W	Transmit Signaling 1	Same
41	R/W	Transmit Signaling 2	Same
42	R/W	Transmit Signaling 3	Same
43	R/W	Transmit Signaling 4	Same
44	R/W	Transmit Signaling 5	Same
45	R/W	Transmit Signaling 6	Same
46	R/W	Transmit Signaling 7	Same
47	R/W	Transmit Signaling 8	Same
48	R/W	Transmit Signaling 9	Same
49	R/W	Transmit Signaling 10	Same
4A	R/W	Transmit Signaling 11	Same
4B	R/W	Transmit Signaling 12	Same
4C	R/W	Transmit Signaling 13	Same
4D	R/W	Transmit Signaling 14	Same
4E	R/W	Transmit Signaling 15	Same
4F	R/W	Transmit Signaling 16	Same
50	R/W	Transmit Si Bits Align Frame	Same
51	R/W	Transmit Si Bits Non–Align Frame	Same
52	R/W	Transmit Remote Alarm Bits	Same
53	R/W	Transmit Sa4 Bits	Same
54	R/W	Transmit Sa5 Bits	Same

ADDRESS	R/W	DS21Q44 REGISTER NAME	DS21Q43A REGISTER NAME
55	R/W	Transmit Sa6 Bits	Same
56	R/W	Transmit Sa7 Bits	Same
57	R/W	Transmit Sa8 Bits	Same
58	R	Receive Si bits Align Frame	Same
59	R	Receive Si bits Non–Align Frame	Same
5A	R	Receive Remote Alarm Bits	Same
5B	R	Receive Sa4 Bits	Same
5C	R	Receive Sa5 Bits	Same
5D	R	Receive Sa6 Bits	Same
5E	R	Receive Sa7 Bits	Same
5F	R	Receive Sa8 Bits	Same
60	R/W	Transmit Channel 1	Not Used
61	R/W	Transmit Channel 2	Not Used
62	R/W	Transmit Channel 3	Not Used
63	R/W	Transmit Channel 4	Not Used
64	R/W	Transmit Channel 5	Not Used
65	R/W	Transmit Channel 6	Not Used
66	R/W	Transmit Channel 7	Not Used
67	R/W	Transmit Channel 8	Not Used
68	R/W	Transmit Channel 9	Not Used
69	R/W	Transmit Channel 10	Not Used
6A	R/W	Transmit Channel 11	Not Used
6B	R/W	Transmit Channel 12	Not Used
6C	R/W	Transmit Channel 13	Not Used
6D	R/W	Transmit Channel 14	Not Used
6E	R/W	Transmit Channel 15	Not Used
6F	R/W	Transmit Channel 16	Not Used
70	R/W	Transmit Channel 17	Not Used
71	R/W	Transmit Channel 18	Not Used
72	R/W	Transmit Channel 19	Not Used
73	R/W	Transmit Channel 20	Not Used
74	R/W	Transmit Channel 21	Not Used
75	R/W	Transmit Channel 22	Not Used
76	R/W	Transmit Channel 23	Not Used
77	R/W	Transmit Channel 24	Not Used
78	R/W	Transmit Channel 25	Not Used
79	R/W	Transmit Channel 26	Not Used
7A	R/W	Transmit Channel 27	Not Used
7B	R/W	Transmit Channel 28	Not Used
7C	R/W	Transmit Channel 29	Not Used
7D	R/W	Transmit Channel 30	Not Used
7E	R/W	Transmit Channel 31	Not Used
7F	R/W	Transmit Channel 32	Not Used
80	R/W	Receive Channel 1	Not Used
81	R/W	Receive Channel 2	Not Used
82	R/W	Receive Channel 3	Not Used

ADDRESS	R/W	DS21Q44 REGISTER NAME	DS21Q43A REGISTER NAME
83	R/W	Receive Channel 4	Not Used
84	R/W	Receive Channel 5	Not Used
85	R/W	Receive Channel 6	Not Used
86	R/W	Receive Channel 7	Not Used
87	R/W	Receive Channel 8	Not Used
88	R/W	Receive Channel 9	Not Used
89	R/W	Receive Channel 10	Not Used
8A	R/W	Receive Channel 11	Not Used
8B	R/W	Receive Channel 12	Not Used
9C	R/W	Receive Channel 13	Not Used
8D	R/W	Receive Channel 14	Not Used
8E	R/W	Receive Channel 15	Not Used
8F	R/W	Receive Channel 16	Not Used
90	R/W	Receive Channel 17	Not Used
91	R/W	Receive Channel 18	Not Used
92	R/W	Receive Channel 19	Not Used
93	R/W	Receive Channel 20	Not Used
94	R/W	Receive Channel 21	Not Used
95	R/W	Receive Channel 22	Not Used
96	R/W	Receive Channel 23	Not Used
97	R/W	Receive Channel 24	Not Used
98	R/W	Receive Channel 25	Not Used
99	R/W	Receive Channel 26	Not Used
9A	R/W	Receive Channel 27	Not Used
9B	R/W	Receive Channel 28	Not Used
9C	R/W	Receive Channel 29	Not Used
9D	R/W	Receive Channel 30	Not Used
9E	R/W	Receive Channel 31	Not Used
9F	R/W	Receive Channel 32	Not Used
A0	R/W	Transmit Channel Control 1	Not Used
A1	R/W	Transmit Channel Control 2	Not Used
A2	R/W	Transmit Channel Control 3	Not Used
A3	R/W	Transmit Channel Control 4	Not Used
A4	R/W	Receive Channel Control 1	Not Used
A5	R/W	Receive Channel Control 2	Not Used
A6	R/W	Receive Channel Control 3	Not Used
A7	R/W	Receive Channel Control 4	Not Used
A8	R/W	Common Control 4	Not Used
A9	R	Transmit DS0 Monitor	Not Used
AA	R/W	Common Control 5	Not Used
AB	R	Receive DS0 Monitor	Not Used
AC	R/W	Test 3	Not Used
AD	-	Not Used	Not Used
AE	-	Not Used	Not Used
AF	-	Not Used	Not Used
B0	R/W	HDLC Control Register	Not Used

ADDRESS	R/W	DS21Q44 REGISTER NAME	DS21Q43A REGISTER NAME
B1	R/W	HDLC Status Register	Not Used
B2	R/W	HDLC Interrupt Mask Register	Not Used
B3	R/W	Receive HDLC Information Register	Not Used
B4	R/W	Receive HDLC FIFO Register	Not Used
B5	R/W	Interleave Bus Operation Register	Not Used
B6	R/W	Transmit HDLC Information Register	Not Used
B7	R/W	Transmit HDLC FIFO Register	Not Used
B8	R/W	Receive HDLC DS0 Control Register 1	Not Used
B9	R/W	Receive HDLC DS0 Control Register 2	Not Used
BA	R/W	Transmit HDLC DS0 Control Register 1	Not Used
BB	R/W	Transmit HDLC DS0 Control Register 2	Not Used
BC	-	Not Used	Not Used
BD	-	Not Used	Not Used
BE	-	Not Used	Not Used
BF	-	Not Used	Not Used

NOTE:

Test Registers 1 and 2 are used only by the factory; these registers must be cleared (set to all zeros) on power up initialization to insure proper operation.

3.2   New Feature Register Usage

Highlights specific registers containing bit locations related to new features. Each item can be found in the data sheet under the listed sections.

3.2.1 Device Identification (section 6)

Register	Description
IDR	Device Identification Register

3.2.2 Expanded Elastic Stores Reset Functions (section 6)

Register	Description
CCR5	Common Control Register 5
CCR6	Common Control Register 6

3.2.3 Interrupt on Change of Signaling State (section 7 and 10)

Register	Description
SR1	Status Register 2 (bits 7 and 5)
IMR1	Interrupt Mask Register 2 (bits 7 and 5)

3.2.4 DS0 Monitoring (section 6 and 9)

Register	Description
CCR4	Common Control 4 (bits 4–0)
CCR5	Common Control 5 (bits 4–0)

TDSOM	Transmit DS0 Monitor
RDSOM	Receive DS0 Monitor

3.2.5 Hardware Based Signaling (section 6 and 10.2)

Register	Description
TCBR1–3	Transmit Channel Block Registers 1 – 3
CCR3	Common Control 3 (bits 3 and 2)

3.2.6 Signaling Freeze (section 6 and 10.2)

Register	Description
CCR2	Common Control 2 (bits 1 and 0)

3.2.7 Per Channel Loopback (section 6 and 11.1)

Register	Description
CCR3	Common Control 3 (bit 5)
*TIR1–3	Transmit Idle Register 1 – 3

*Note: Alternate function for existing register set

3.2.8 Per Channel Code (Idle) Insertion (section 11.1 and 11.2)

Register	Description
TCC1 – TCC4	Transmit Channel Control 1 – 4
TC1 – TC32	Transmit Channels Registers 1 – 32
RCC1 – RCC4	Receive Channel Control 1 – 4
RC1 – RC32	Receive Channels Registers 1 – 32

102199

3.2.9 Full HDLC & BOC Controller For FDL Support (section 15)

Register	Description
HCR	HDLC Control Register
HSR	HDLC Status Register
HIMR	HDLC Interrupt Mask Register
RHIR	Receive HDLC Information Register
RHFR	Receive HDLC FIFO Register
RDC1	Receive HDLC DS0 Control Register 1
RDC2	Receive HDLC DS0 Control Register 2
THIR	Transmit HDLC Information Register
THFR	Transmit HDLC FIFO Register
TDC1	Transmit HDLC DS0 Control Register 1
TDC2	Transmit HDLC DS0 Control Register 2

3.2.10   Interleaved PCM Bus Operation (section 16)

Register	Description
IBO	Interleave Bus Operation

3.3 Bit Assignment Changes within Existing Registers

Highlights bit locations in the DS21Q44 which have changed from the DS21Q43A.

Register	Bit #	DS21Q43A Symbol	DS21Q43A Description	DS21Q44A Symbol	DS21Q44A Description
CCR2	0	N/A	Not assigned	RFE	Receive Freeze Enable
CCR2	1	N/A	Not assigned	RFF	Receive Force Freeze
CCR3	0	N/A	Not assigned	RCLA	Receive Carrier Loss Alternate Criteria
CCR3	2	N/A	Not assigned	THSE	Transmit Side Hardware Signaling Insertion Enable
CCR3	3	N/A	Not assigned	RSRE	Receive Side Signaling Re–Insertion Enable
CCR3	4	ESR	Elastic Stores Reset	N/A	Not Assigned
ISR	0	F3SR2	Status of Interrupt for SR2 in Framer 3	F3HDLC	Framer 3 HDLC Controller Int. Request
ISR	1	F3SR1	Status of Interrupt for SR1 in Framer 3	F3SR	Framer 3 SR1 or SR2 Interrupt Request
ISR	2	F2SR2	Status of Interrupt for SR2 in Framer 2	F2HDLC	Framer 3 HDLC Controller Int. Request
ISR	3	F2SR1	Status of Interrupt for SR1 in Framer 2	F2SR	Framer 3 SR1 or SR2 Interrupt Request
ISR	4	F1SR2	Status of Interrupt for SR2 in Framer 1	F1HDLC	Framer 3 HDLC Controller Int. Request
ISR	5	F1SR1	Status of Interrupt for SR1 in Framer 1	F1SR	Framer 3 SR1 or SR2 Interrupt Request
ISR	6	F0SR2	Status of Interrupt for SR2 in Framer 0	F0HDLC	Framer 3 HDLC Controller Int. Request
ISR	7	F0SR1	Status of Interrupt for SR1 in Framer 0	F0SR	Framer 3 SR1 or SR2 Interrupt Request
RIR	5	LORC	Loss of Receive Clock	N/A	Not assigned
SR1	5	RSA1	Receive Signaling All Ones	RSA1	Receive Signaling All Ones / Signaling Change
SR1	7	RSA0	Receive Signaling All Zeroes	RSA0	Receive Signaling All Zeroes / Signaling Change
IMR1	5	RSA1	Receive Signaling All Ones	RSA1	Receive Signaling All Ones / Signaling Change
IMR1	7	RSA0	Receive Signaling All Zeroes	RSA0	Receive Signaling All Zeroes / Signaling Change

102199

3.4   Register Bit Moves

Function	DS21Q43A Location	DS21Q44 Location
ESR	CCR3.4	Split into RESR (CCR6.1) and TESR (CCR6.0)

3.5   Register Address Moves

Function	DS21Q43A Location	DS21Q44 Location
ISR	Any address between 60h to 7Fh or between E0h and FFh	Any address from C0h to FFh

4.0 Changes in Device Pin Out

4.1 Package types

The DS21Q43A and DS21Q44 are both offered in a 128 pin 20 x 14 x 1.4 mm TQFP. Values listed are for body dimensions.

4.2   Device Pin Differences

4.2.1 Control Port Pins

DS21Q44	DS21Q43A	DESCRIPTION
A7	V_{SS}	Address Bus Bit 7
FMS	V_{dd}	Framer Mode Select
CLKSI [RLOS/LOTC3]	RLOS/LOTC3	8 MHz Clock Reference Input [Receive Loss of Sync / Loss of Transmit Clock from Framer 3]
8MCLK [RMSYNC3]	RMSYNC3	8 MHz Clock [Receive Multiframe Sync from Framer 3]

NOTE:

Brackets [ ] indicate pin function when DS21Q44 is configured for emulation of the DS21Q43A, (FMS = 1).

4.2.2 Transmit Side Digital Pins

DS21Q44	DS21Q43A	DESCRIPTION
TSIG0 [TCHCLK0]	TCHCLK0	Transmit Signaling Input for Framer 0 [Transmit Channel Clock from Framer 0]
TSIG1 [TCHCLK1]	TCHCLK1	Transmit Signaling Input for Framer 1 [Transmit Channel Clock from Framer 1]
TSIG2 [TCHCLK2]	TCHCLK2	Transmit Signaling Input for Framer 2 [Transmit Channel Clock from Framer 2]
TSIG3 [TCHCLK3]	TCHCLK3	Transmit Signaling Input for Framer 3 [Transmit Channel Clock from Framer 3]

NOTE:

Brackets [ ] indicate pin function when DS21Q44 is configured for emulation of the DS21Q43A, (FMS = 1).

4.2.3 Receive Side Digital / JTAG Pins

DS21Q44	DS21Q43A	DESCRIPTION
JTRST* [RLOS/LOTC0]	RLOS/LOTC0	JTAG Reset [Receive Loss of Sync / Loss of Transmit Clock from Framer 0]
JTCLK [RLOS/LOTC1]	RLOS/LOTC1	JTAG Test Clock [Receive Loss of Sync / Loss of Transmit Clock from Framer 1]
JTDO [RLOS/LOTC2]	RLOS/LOTC2	JTAG Test Data Output [Receive Loss of Sync / Loss of Transmit Clock from Framer 2]
CLKSI [RLOS/LOTC3]	RLOS/LOTC3	MHz Clock [Receive Loss of Sync / Loss of Transmit Clock from Framer 3]
SPARE1 [RMSYNC0]	RMSYNC0	RESERVED – must be left unconnected for normal operation [Receive Multiframe Sync from Framer 0]
JTMS [RMSYNC1]	RMSYNC1	JTAG Test Mode Select [Receive Multiframe Sync from Framer 1]
JTDI [RMSYNC2]	RMSYNC2	JTAG Test Data Input [Receive Multiframe Sync from Framer 2]
8MCLK [RMSYNC3]	RMSYNC3	MCLK Clock Reference Input [Receive Multiframe Sync from Framer 3]
RSIG0 [RCHCLK0]	RCHCLK0	Receive Signaling Output from Framer 0 [Receive Channel Clock from Framer 0]
RSIG0 [RCHCLK1]	RCHCLK1	Receive Signaling Output from Framer 1 [Receive Channel Clock from Framer 1]
RSIG0 [RCHCLK2]	RCHCLK2	Receive Signaling Output from Framer 2 [Receive Channel Clock from Framer 2]
RSIG0 [RCHCLK3]	RCHCLK3	Receive Signaling Output from Framer 3 [Receive Channel Clock from Framer 3]

NOTE:
Brackets [ ] indicate pin function when DS21Q44 is configured for emulation of the DS21Q43A, (FMS = 1).

5.0 Operating the DS21Q44 in DS21Q43A Emulation Mode
The DS21Q44 is a superset of the DS21Q43A and can be configured to emulate the latter. This mode is enabled by tying the Framer Mode Select (FMS) pin to Vcc. Since the DS21Q44 supports an expanded register set, the A7 address pin was added to the device. Although the DS21Q44 does not require the functionality associated with the additional registers when in DS21Q43A emulation mode, the A7 pin must be used. This is necessary because the device does not automatically clear its register space on power–up. After the supplies are stable, each of four framers register space should be configured for operation by writing to all of the internal registers. This can be accomplished in a two–pass approach on each framer.
1. Clear framers register space by writing 00h to the addresses 00h through BFh.
2. Program required registers to achieve desired operating mode.