Application Note 342
Initialization and Programming

This application note applies to the following product.

DS2151	DS2153
DS2152	DS2154
DS21352	DS21354
DS21552	DS21554

GENERAL INITIALIZATION

After power–up, when supplies and clocks have stabilized, internal registers must be initialized. It is a good idea to clear, set to 00H, **ALL** R/W registers. Certain registers have bits which control special test modes and features which can provide confusing indications.

These registers are:

DS2151:	**TEST, TCR2, LICR**	DS2153:	**TEST 1, TEST 2, LICR**
DS2152:	**TEST 1, TEST 2, TCR2, LICR**	DS2154:	**TEST 1, TEST 2, LICR**
DS21352:	**TEST 1, TEST 2, TCR2, LICR**	DS21354:	**TEST 1, TEST 2, TCR2, LICR**
DS21552:	**TEST 1, TEST 2, TCR2, LICR**	DS21554:	**TEST 1, TEST 2, TCR2, LICR**

Depending on the interrupt structure implemented, it may be a good idea to clear **IMR1** and **IMR2** first. Prior to clearing these two registers, spurious interrupt signals may occur without an external interrupt disable.

Once the registers have be initialized and set up with the transceiver's mode of operation. The Line Interface Reset bit should be set high then low. Also, if the elastic store is enabled, the **ESR** bit should be set then cleared.

SPECIAL INITIALIZATION FOR DS2153 (DS2154, DS21354 & DS21554)

TCLK (Transmit Clock) must be present for proper port initialization. Network signals (Loop Timing cannot be guaranteed to replace a missing TCLK during initialization. The following sequence should be used to initialize the **DS2153 (DS2154)** in which TCLK is not present or TCLK is derived from RCLK (a loop timed system).

- WRITE 04h TO **CCR2** REGISTER (SET **LOTCMC** BIT)
- WAIT 10ms MINIMUM
- WRITE 00h TO ALL OTHER R/W REGISTERS
- WRITE INITIAL DEVICE CONFIGURATION DATA
- SET **LIRST** BIT IN **CCR3 (CCR5)** REGISTER HIGH
- WAIT FOR SYSCLK (RSYSCLK & TSYSCLK) TO STABILIZE—IF ELASTIC STORE(S) ENABLED

- SET **ESR** BIT IN **CCR3** REGISTER HIGH—IF ELASTIC STORE ENABLED
- CLEAR **LIRST** AND **ESR** BITS.

NOTES:

1. In Loop Timed configurations or when TCLK is not guaranteed to always be present it is recommended that **LOTCMC** in **CCR2** be enabled (= 1).
2. If the SYSCLK pin is tied high, registers can be initialized (written to), but not read.