DALLAS SEMICONDUCTOR

Application Note 336
Transparent Operation

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This application note applies to the following products.

T1 Framers	E1 Framers	T1 SCT's	E1 SCT's
DS21Q41	DS21Q43	DS2151	DS2153
DS21Q42	DS21Q44	DS2152	DS2154
DS21FF42	DS21FF44	DS21352	DS21354
DS21FT42	DS21FT44	DS21552	DS21554
		DS21Q352	DS21Q354
		DS21Q553	DS21Q554

The Dallas Semiconductor framers can operate in a transparent mode in both the receive and transmit directions. The transmitter will not insert framing, signaling, or other information such as CRC or FDL. Generally, the receive side of the framers is always transparent. Data received at RTIP and RRING is passed through intact to RSER. All configurations are with the elastic stores disabled. The elastic stores will not alter data except during slip conditions or if configured for 1.544MHz / 2.048MHz conversion or signaling reinsertion.

DS21Q42 DS21FF42 DS21FT42 DS21352 DS21552 DS21Q352 DS21Q552:

Register configurations:
TCR1.2, TCR1.5, TCR1.6 = 1
TCR1.0, TCR1.1, TCR1.4 = 0
TCR2.0 = 0
TIR1, TIR2, TIR3 = 00h
TCC1, TCC2, TCC3 = 00h
RCC1, RCC2, RCC3 = 00h
TDC1.7 = 0
CCR1.5 = 0
RMR1, RMR2, RMR3 = 00h

DS21Q44 DS21FF44 DS21FT44 DS21354 DS21554 DS21Q354 DS21Q554:

Register configurations:
TCR1.6 = 1
TCR1.2, TCR1.3, TCR1.4, TCR1.5 = 0
TCR2.1, TCR2.2, TCR2.3, TCR2.4, TCR2.5, TCR2.6, TCR2.7 = 0
CCR1.4 = 0
CCR2.3, CCR2.4, CCR2.5 = 0
TIR1, TIR2, TIR3, TIR4 = 00h
TCC1, TCC2, TCC3, TCC4 = 00h
RCC1, RCC2, RCC3, RCC4 = 00h
TSaCR = 00h
TDC1.7 = 0

DS2152:

Register configurations:
TCR1.2, TCR1.5, TCR1.6 = 1
TCR1.0, TCR1.1, TCR1.4 = 0
TCR2.0 = 0
TIR1, TIR2, TIR3 = 00h
TCC1, TCC2, TCC3 = 00h
RCC1, RCC2, RCC3 = 00h
CCR1.5 = 0
RMR1, RMR2, RMR3 = 00h

DS2154:

Register configurations:
TCR1.6 = 1
TCR1.2, TCR1.3, TCR1.4, TCR1.5 = 0
TCR2.1, TCR2.2, TCR2.3, TCR2.4, TCR2.5, TCR2.6, TCR2.7 = 0
CCR1.4 = 0
CCR2.3, CCR2.4, CCR2.5 = 0
CCR4.5 = 0
TIR1, TIR2, TIR3, TIR4 = 00h
TCC1, TCC2, TCC3, TCC4 = 00h
RCC1, RCC2, RCC3, RCC4 = 00h

DS2151 DS21Q41:

Hardware considerations:
TSER and TLINK must be tied together either logically or physically.

Register configurations:
TCR1.2, TCR1.5, TCR1.6 = 1
TCR1.0, TCR1.1, TCR1.4 = 0
TCR2.0 = 0
TIR1, TIR2, TIR3 = 00h
CCR1.5 = 0
RMR1, RMR2, RMR3 = 00h

DS2153 DS21Q43:

Hardware considerations:
Need rev A5 or better for complete receive transparency with elastic store enabled (DS2153 only).

Register configurations:
TCR1.6 = 1
TCR1.2, TCR1.3, TCR1.4, TCR1.5 = 0
CCR1.4 = 0
CCR2.3, CCR2.4, CCR2.5 = 0
TIR1, TIR2, TIR3, TIR4 = 00h
TCR2.1, TCR2.2, TCR2.3, TCR2.4, TCR2.5, TCR2.6, TCR2.7 = 0
RCR2.1 = 0 (required on rev A2 devices only)