DALLAS SEMICONDUCTOR

Application Note 333
DS2172 Pattern Synchronization

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This application note applies to the DS2172.

The DS2172 can be used to generate repetitive patterns up to 32 bits in length. Operation of the synchronizer differs in this mode from the Pseudo random Pattern mode. In the Repetitive Pattern mode the receiver looks for a repeating pattern of the same length (or multiple of) as the one being transmitted. It does not verify a pattern match with what is being transmitted. Once it has found a pattern of the same length it declares synchronization and will count any deviations in that pattern, not the one being transmitted, as bit errors. An all zero or all one's pattern received at RDATA will emulate any length pattern and the DS2172 will synchronize to it no matter what has been programmed into the Pattern Set Register. Consider the following examples where the pattern at RDATA emulates the 6 bit pattern programmed into the transmitter.

Transmit patter 101110

Received pattern 000000 will synchronize
Received pattern 111111 will synchronize
Received pattern 101010 will synchronize

After synchronization has been established it is up to the user to check the Pattern Receive Register to verify that the correct pattern is being received. The pattern in the Pattern Receive Registers will likely be shifted one or more positions from the pattern in the Pattern Set registers. The flow chart in figure 1 describes the basic algorithm that will verify that the received pattern is the same as the transmitted pattern. Also, the Received All Zeros and Received All Ones indicators the Status Register can be used to verify pattern synchronization. The user should always check the status register after synchronization to make sure the system is operating as expected.

Both the Bit Count Register and the Bit Error Count Register are inhibited during a loss of sync condition.

Once sync is established the Bit Count Register will increment on every RCLK. The Bit Error Count Register will increment for every bit error in the pattern to which the receiver synchronized.

Both receive and transmit functions operate off of RCLK and TCLK respectively. Typically events such as Latch Count, Transmit Load and Receive Data Load are triggered off the rising edge of the clocks. These operation may take several clock cycles to complete. At low clock rates and high processor speeds the user should allow for sufficient time for operations such as reading the counters to take place. Also note that using RDIS and TDIS to gap the receive and transmit signal, inhibits all associated functions in the device.

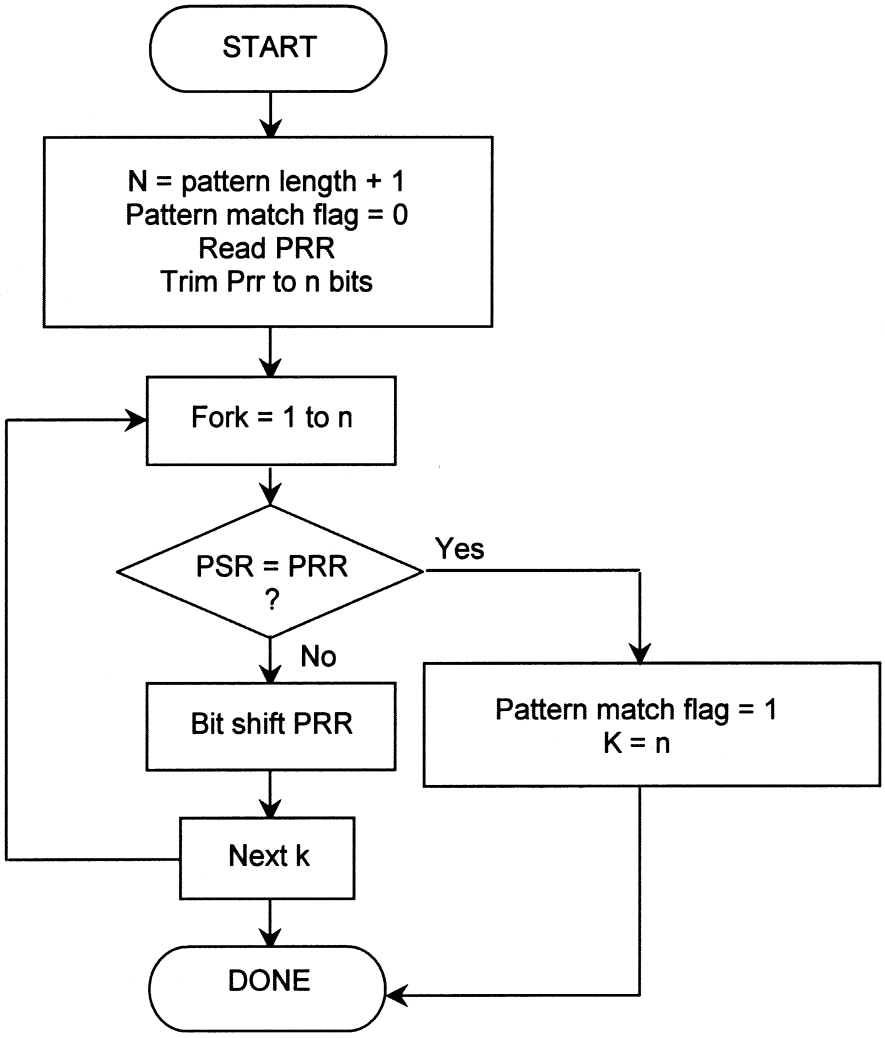
START
N = pattern length + 1
Pattern match flag = 0
Read PRR
Trim Prr to n bits
Fork = 1 to n
PSR = PRR
?
Yes
No
Bit shift PRR
Pattern match flag = 1
K = n
Next k
DONE

Figure 1