Application Note 310
D4 Framing and Signaling

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This application note applies to the following products.

T1 Framers	T1 SCT's
DS21Q41	DS2151
DS21Q42	DS2152
DS21FF42	DS21352
DS21FT42	DS21552
	DS21Q352
	DS21Q553

Several control settings are required to generate D4 multi framing in the transmit direction.

CCR2.7, CCR2.3 = 0. Selects D4 multi framing in the transmit and receive directions.
CCR2.5 = 1. Enables insertion of the 6 bit Fs pattern.
TFDL = 1Ch. This is the 6 bit Fs pattern.
RCR1.3 = 1. If this bit is cleared, the receiver will declare synchronization on the Ft pattern only and will not be guaranteed to find the D4 multiframe boundary.
After configuring these control registers, toggle RCR1.0 to force resynchronization

Notes on the signaling registers:

Transmit signaling registers:
In D4 multi framing, only 6 of the 12 transmit signaling registers are needed to load a multiframe of signaling. The transmitter alternates, loading the contents of TS1 through TS6 into one multiframe, followed by the contents of TS7 through TS12 into the next multiframe, then back again. Therefore, load the transmit signaling bytes into two registers.

TS1 and TS7	A bits for channels 1 through 8
TS2 and TS8	A bits for channels 9 through 16
TS3 and TS9	A bits for channels 17 through 24
TS4 and TS10	B bits for channels 1 through 8
TS5 and TS11	B bits for channels 9 through 16
TS6 and TS12	B bits for channels 17 through 24

Receive signaling registers:
Signaling from the most recent multiframe is loaded into RS7 through RS12.
Signaling from the previous multiframe is moved from RS7 through RS12 and copied to RS1 through RS6.
Older signaling is discarded.

When responding to an RSC (receive signaling change interrupt), or RMF (receive multiframe interrupt), the most recent multiframe of signaling is available in RS7 through RS12, not RS1 through RS6.