Application Note 301
8 MHz System Clock Operation

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This application note applies to the following products.

T1 Framers	E1 Framers	T1 SCT's	E1 SCT's
DS2141	DS2143	DS2151	DS2153
DS21Q41	DS21Q43	DS2152	DS2154

T1 or E1 PCM signals can interface to an 8 MHz system backplane. Typically this application is used to multiplex four PCM streams onto a single 8 MHz PCM stream. To accomplish this the elastic stores are enabled and placed in the 2.048 MHz SYSCLK mode. Figure 1 illustrates a circuit in which a single SYNC signal is generated for all four framers. Each framer in turn is driven with an 8.192 MHz clock burst of 8 cycles. Each clock burst causes the elastic store to output 1 DS0. This results in a "Byte Interleaved" 8.192 MHz PCM steam, Figure 2.

Figure 1:

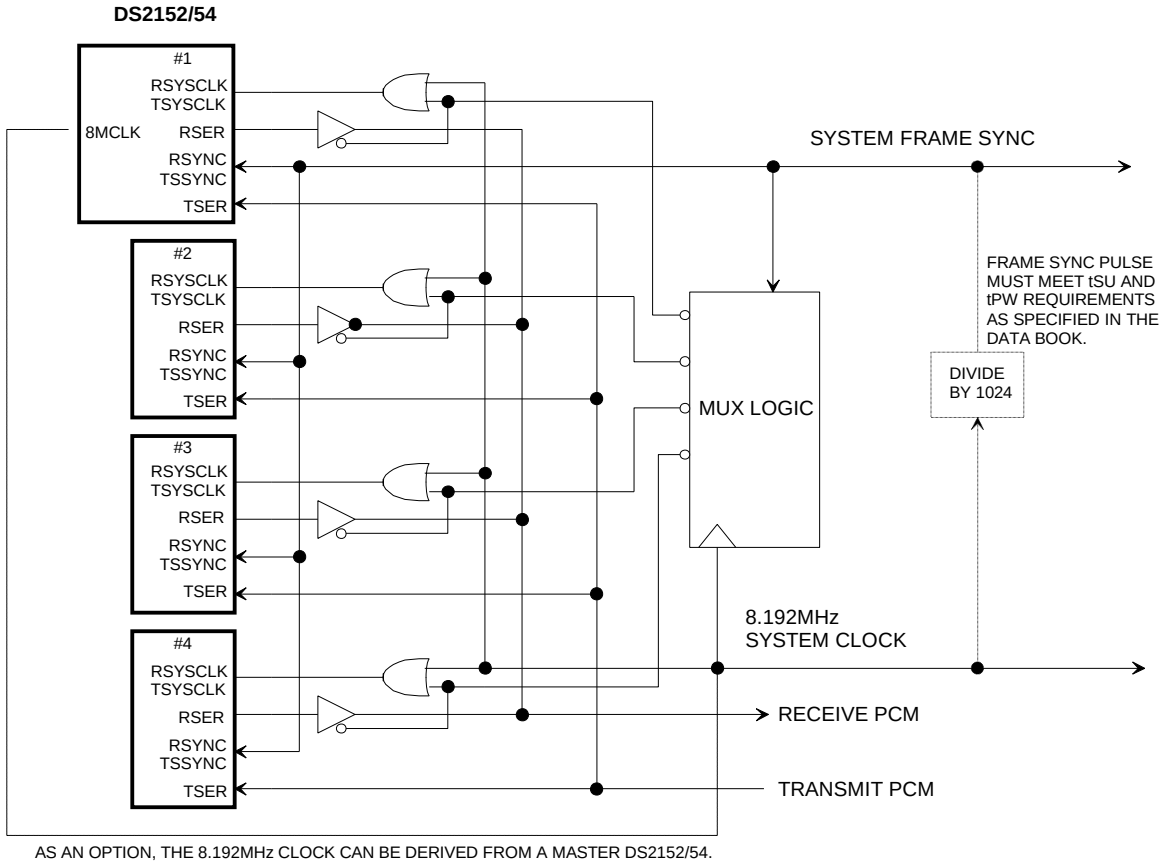
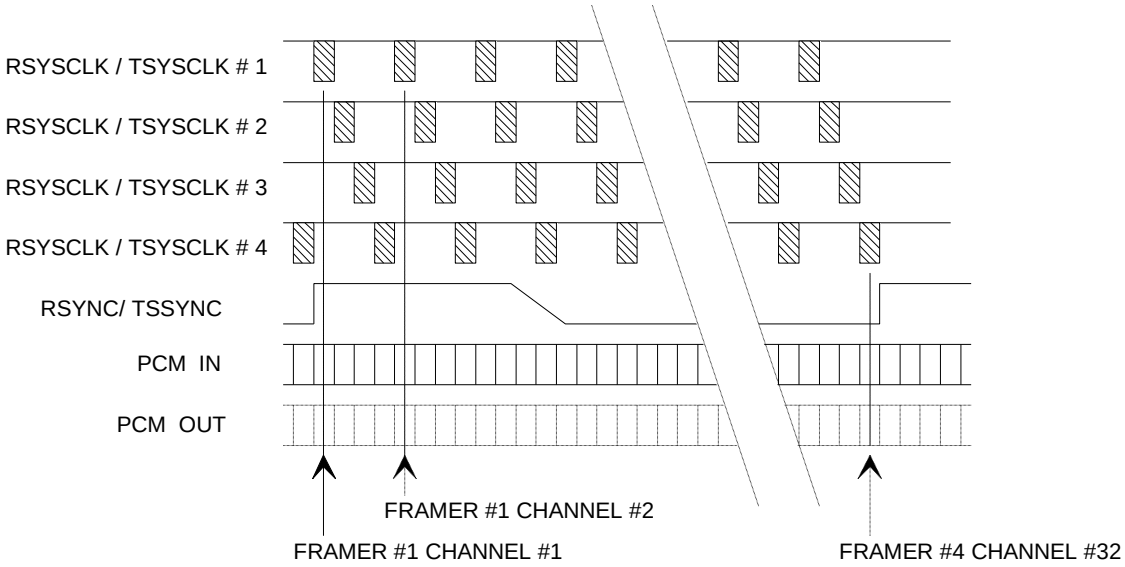
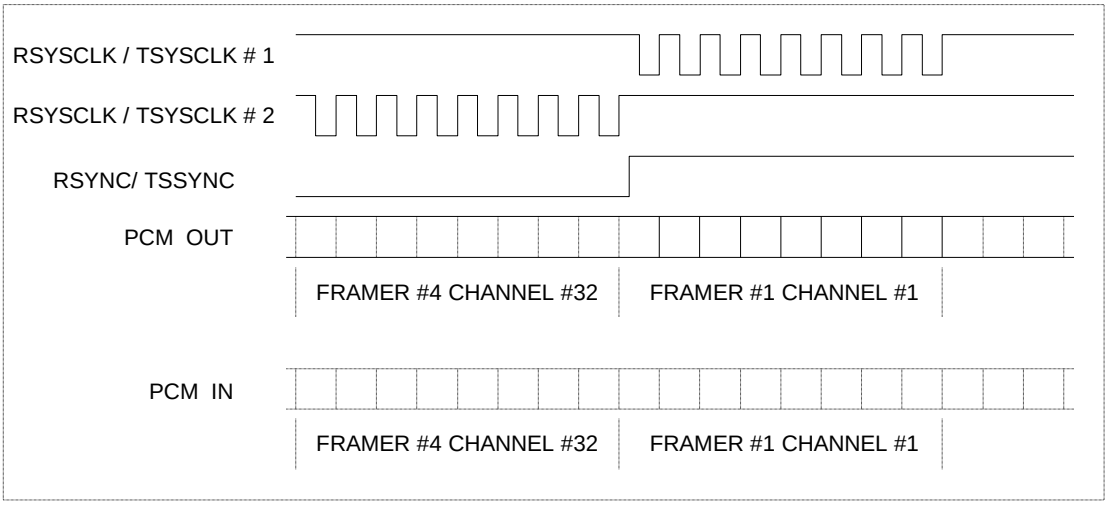


Figure 2:





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MASTER CLOCK SOURCE

In Figure 1, the 8.192 MHz system clock may be derived from a T1/E1 line as indicated by the dotted line. This line becomes the timing "Master" for the other three devices. In this example, device #1 is used as the master. The other three devices may experience frame slips since there is no guarantee that their inbound T1/E1 rates are synchronous to device #1's inbound rate. The elastic store's will manage frame slip events in a logical manner by either repeating or deleting a full frame.

MASTER CLOCK FAILURE

In the event that the master lines fails (goes in Carrier Loss) the following events will occur. RCLK will be replaced by MCLK. If the jitter attenuator is enabled in the receive path this transition will be very smooth. Consequently, the 8.192 MHz clock output on the 8 MCLK pin will make a slight and smooth transition to be phase locked to the clock at MCLK. The 8.192 MHz system timing will not experience any disturbance of the byte interleave structure. Device #1 will report an RCL (Receive Carrier Loss)

event via the status registers. When the failure of the master line is detected by the host processor selection logic may be used to switch to another active line.

Figures 3 and 4 apply to the DS2141, DS21Q41, DS2143, DS21Q43, DS2151 and DS2153.

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Figure 3:

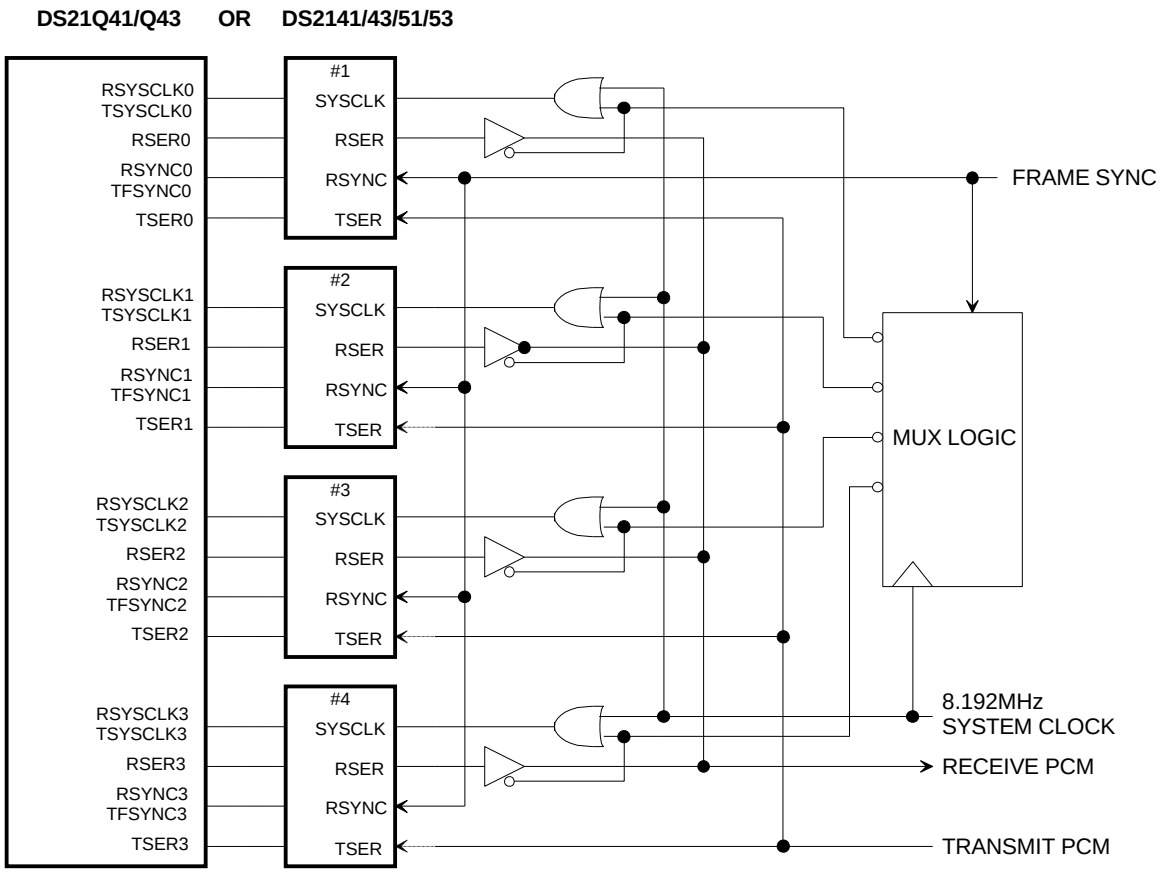
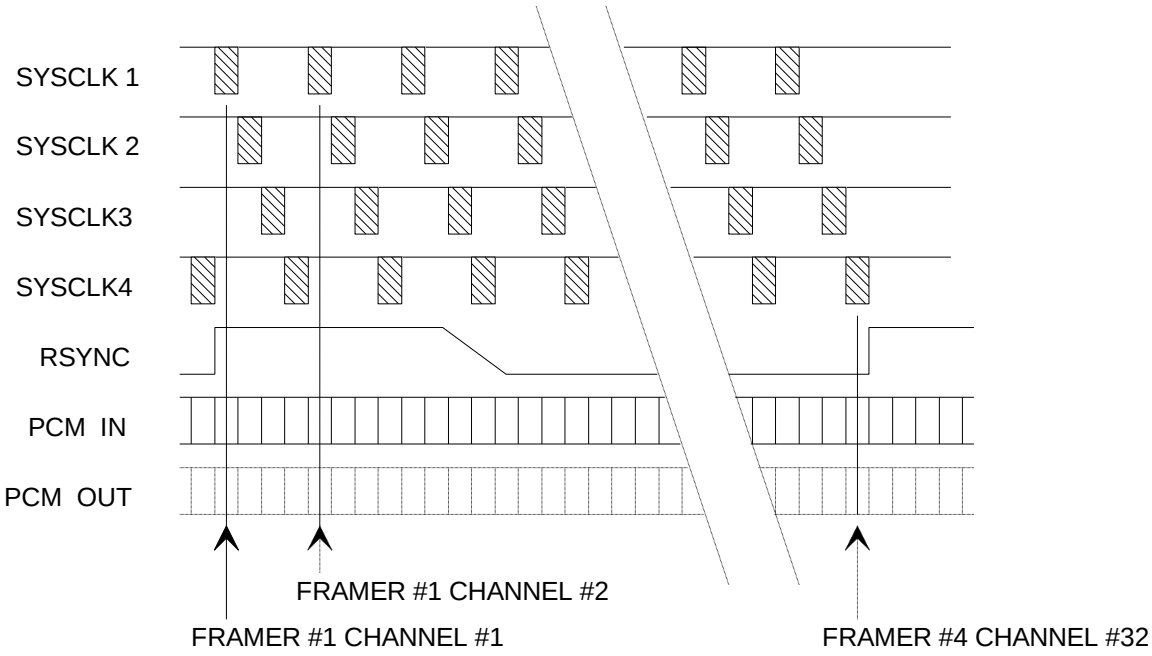
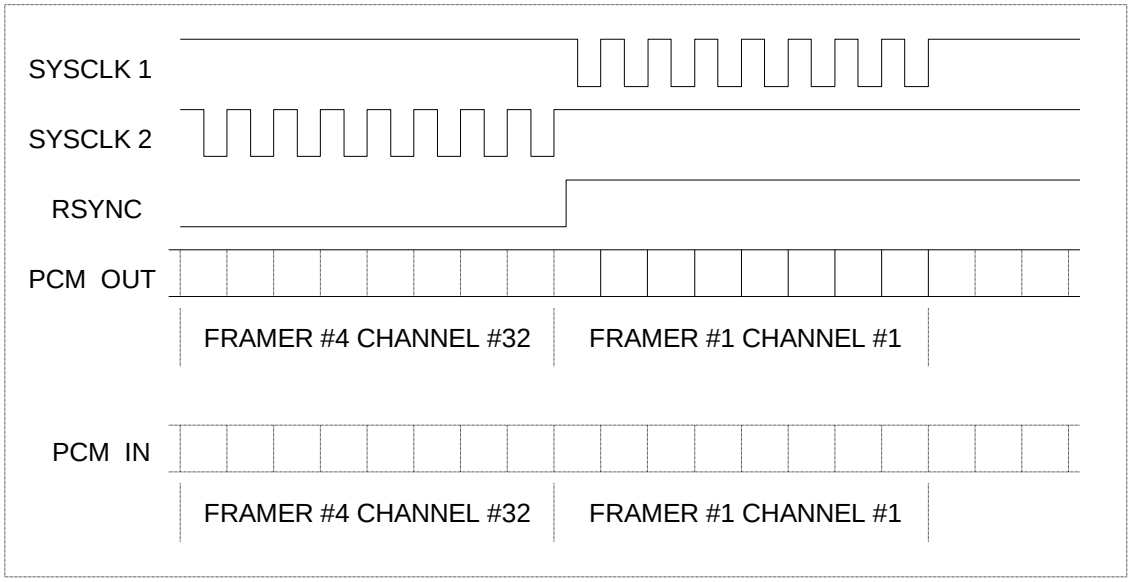


Figure 4:


SYSCLK 1
SYSCLK 2
SYSCLK3
SYSCLK4
RSYNC
PCM IN
PCM OUT
FRAMER #1 CHANNEL #2
FRAMER #1 CHANNEL #1
FRAMER #4 CHANNEL #32


SYSCLK 1
SYSCLK 2
RSYNC
PCM OUT
FRAMER #4 CHANNEL #32
FRAMER #1 CHANNEL #1
PCM IN
FRAMER #4 CHANNEL #32
FRAMER #1 CHANNEL #1