



Application Note 3

Device Characteristics of the DS1045 Dual 4-Bit Programmable Delay Line

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PRODUCT DESCRIPTION

The DS1045 is a 4-Bit Dual Programmable Delay Line that supports two programmable outputs from a single input. This CMOS device is capable of producing outputs in binary steps for maximum delays of up to 84 ns. The selection of one of four standard devices will allow steps of 2, 3, 4, or 5 ns. Table 1 indicates the standard product part for each delay and the maximum delay that can be obtained by each part.

Each half of the device can be programmed through separate input ports. Inputs A0 through A3 control side A output while inputs B0 through B3 control side B output. The inputs can either be held in a static mode or changed dynamically. In the dynamic mode the data enable, setup and hold times must be met. Typically the delay to a valid output is 15 ns. During the transition period the outputs are in an undefined state. The pulse widths of the output will be a reproduction of the input delayed by the selected input delay value. Typical applications are included in the following section.

Each of the outputs is capable of driving 10 standard 74LS type loads. The device is compatible with both TTL and CMOS and is specified driving a 15 pF load. Input capacitance is 10 pF. All timing measurements are measured at 1.5 volts with the exception of rise and fall times. Input and output rise and fall times are measured between 0.6 volts and 2.4 volts.

DELAY VS. PROGRAMMED VALUE Table 1

PART NUMBER	OUTPUT DELAY VALUE															
	DS1045-2	9	11	13	15	17	19	21	23	25	27	29	31	33	35	37
DS1045-3	9	12	15	18	21	24	27	30	33	36	39	42	45	48	51	54
DS1045-4	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69
DS1045-5	9	14	19	24	29	34	39	44	49	54	59	64	69	74	79	84
	PROGRAM VALUES FOR EACH DELAY VALUE															
A0 or B0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
A1 or B1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
A2 or B2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
A3 or B3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

MAXIMUM OPERATIONAL CHARACTERISTICS

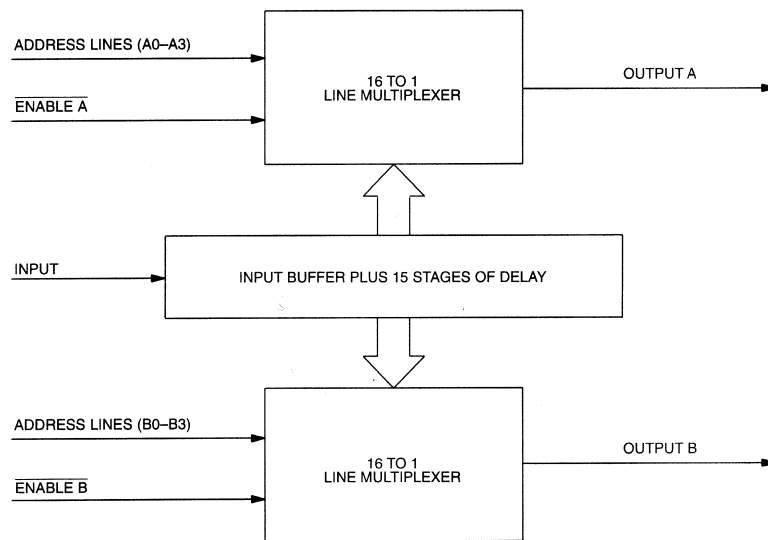
The DS1045 is capable of operation at a very high speed. Consideration should be given with respect to the minimum pulse width of the input signal when the maximum delay step is selected. For example, if a delay of a DS1045-5 of 84 ns is selected, then the input pulse width must not be shorter than 9 ns. Table 2 summarizes the minimum pulse widths (step zero delay), maximum delay times and the delay tolerance for each part number.

PART NUMBER TABLE Table 2

PART NUMBER	STEP ZERO DELAY	MAX DELAY TIME	MAX DELAY TOLERANCE
DS1045-2	9 ± 1 ns	39 ns	± 1.8 ns
DS1045-3	9 ± 1 ns	54 ns	± 2.5 ns
DS1045-4	9 ± 1 ns	69 ns	± 3.3 ns
DS1045-5	9 ± 1 ns	84 ns	± 4.1 ns

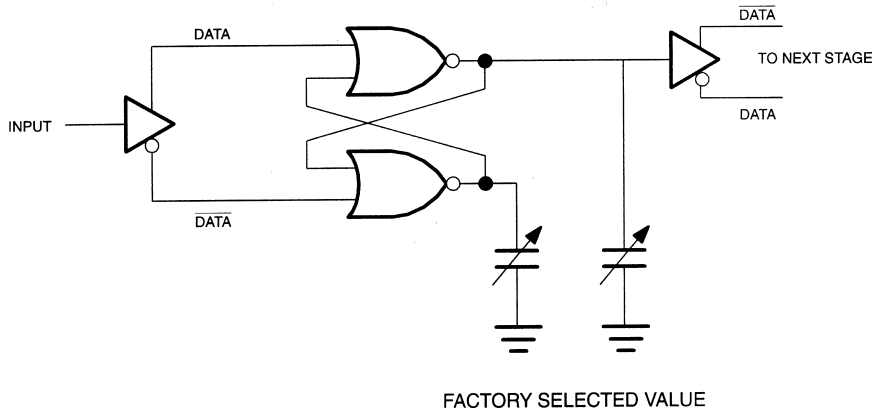
BLOCK DIAGRAM

The DS1045 is composed of a 16 stage delay line and two sets of digital multiplexers. Each side of the device can select an appropriate output delay stage by providing an input to the control code specified in Table 1. The binary value selects the individual stage of delay that becomes the output.

DS1045 BLOCK DIAGRAM Figure 1**CIRCUIT ANALYSIS**

Individual stages may be thought of as RS flip-flops that have a variable capacitive load. Increasing the capacitive load increases the delay. Similarly, a decrease in the load capacitance decreases the delay. The operation of the variable capacitive load is similar to the operation of a varistor. The effect of this variable capacitive loading is that the individual stage set and reset times are precisely controlled. This process establishes controlled rise and fall times and improve the input to output waveform signal integrity of the device. The exact capacitive load is established at the factory in the final stages of the manufacturing process. A simplified schematic of the circuit is shown in Figure 2.

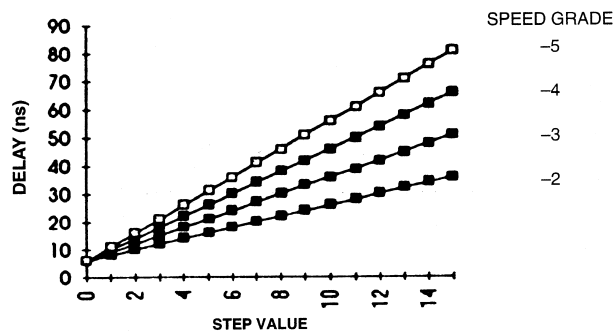
DS1045 CIRCUIT DIAGRAM Figure 2



FAMILY STEP CHARACTERISTICS

Figure 3 indicates the general characteristic of each of the DS1045 devices in this family as a function of Binary Step Value vs. Delay Time.

DS1045 FAMILY DELAY BY PART TYPE Figure 3



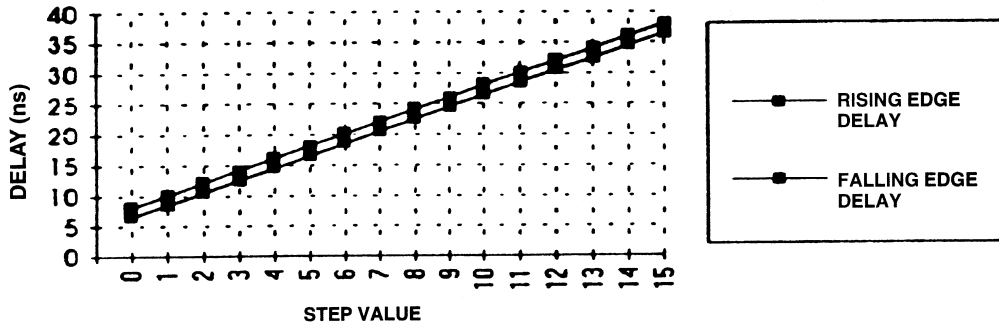
STEP LINEARITY CHARACTERISTICS

Figure 4 indicates step linearity for rising and falling edge signals. Each of the devices exhibits a virtual straight line in step linearity. The device specification limits indicate that the starting delay of the zero position on the chart is the same for each of the devices (9 ns).

This is due to the inherent delay of the first stage. The maximum deviation for any given step is indicated in Table 2. The maximum step tolerance is specified as ± 2.5 ns for a DS1045-3 over the full binary range. The delay time at step zero is the initial buffer delay of 9 ns ± 1 ns.

DS1045-2 RISING AND FALLING EDGE DELAY TIMES VS. STEP SIZE

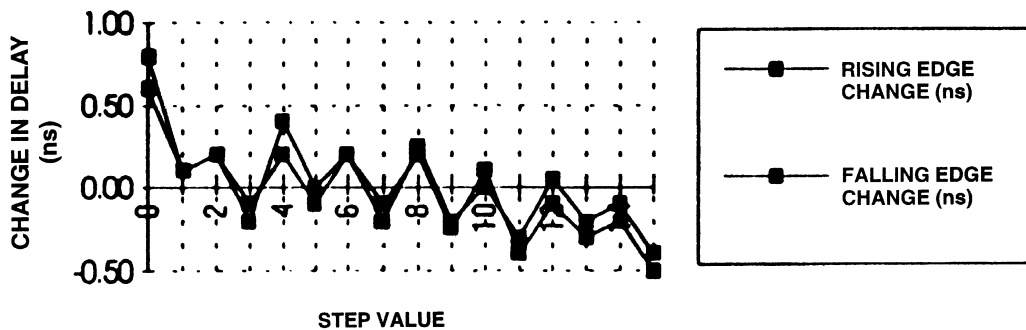
Figure 4



TEMPERATURE CHARACTERISTICS

The DS1045 exhibits excellent temperature characteristics. Figure 5 indicates how the change in delay times for each step is effected by temperature. The data was taken with a 5.0 volt supply voltage. A maximum total excursion (delta) of less than ± 1 ns for both rising and falling edge signal are indicated.

TEMPERATURE CHANGES (0°C TO 70°C) Figure 5

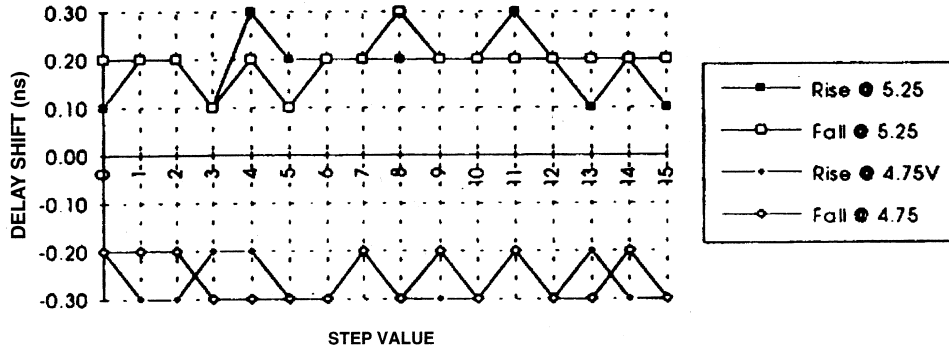


Step Value	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Rising Edge Change (ns)	0.80	0.10	0.20	-0.20	0.40	0.00	0.20	-0.20	0.25	-0.20	0.00	-0.30	0.05	-0.20	-0.10	-0.40
Falling Edge Change (ns)	0.60	0.10	0.20	-0.10	0.20	-0.10	0.20	-0.10	0.20	-0.25	0.10	-0.40	-0.10	-0.30	-0.20	-0.50

VOLTAGE CHARACTERISTICS

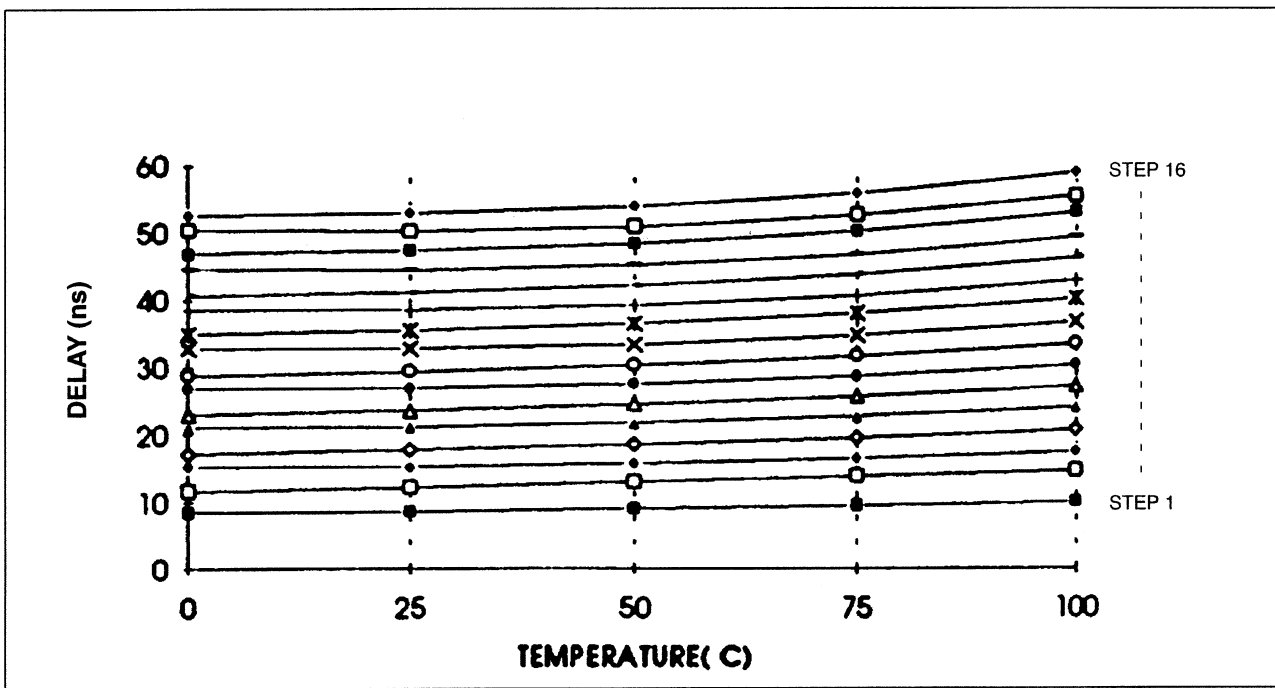
The DS1045 is a voltage compensated device whose outputs, both rising and falling edges, vary less than 300 picoseconds with voltage excursions from 4.75 to 5.25 volts. Figure 6 indicates the values for each of the 16 delay steps.

DS1045 VOLTAGE COMPENSATION Figure 6

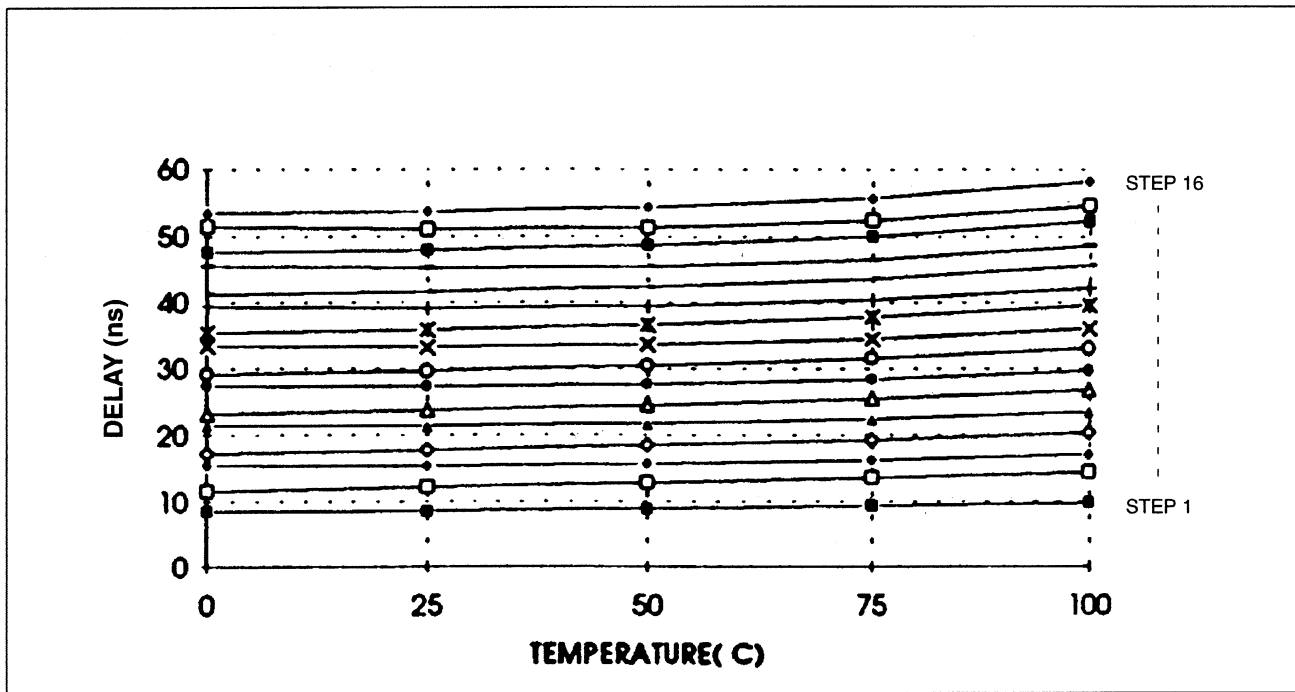


DELAY VS. TEMPERATURE

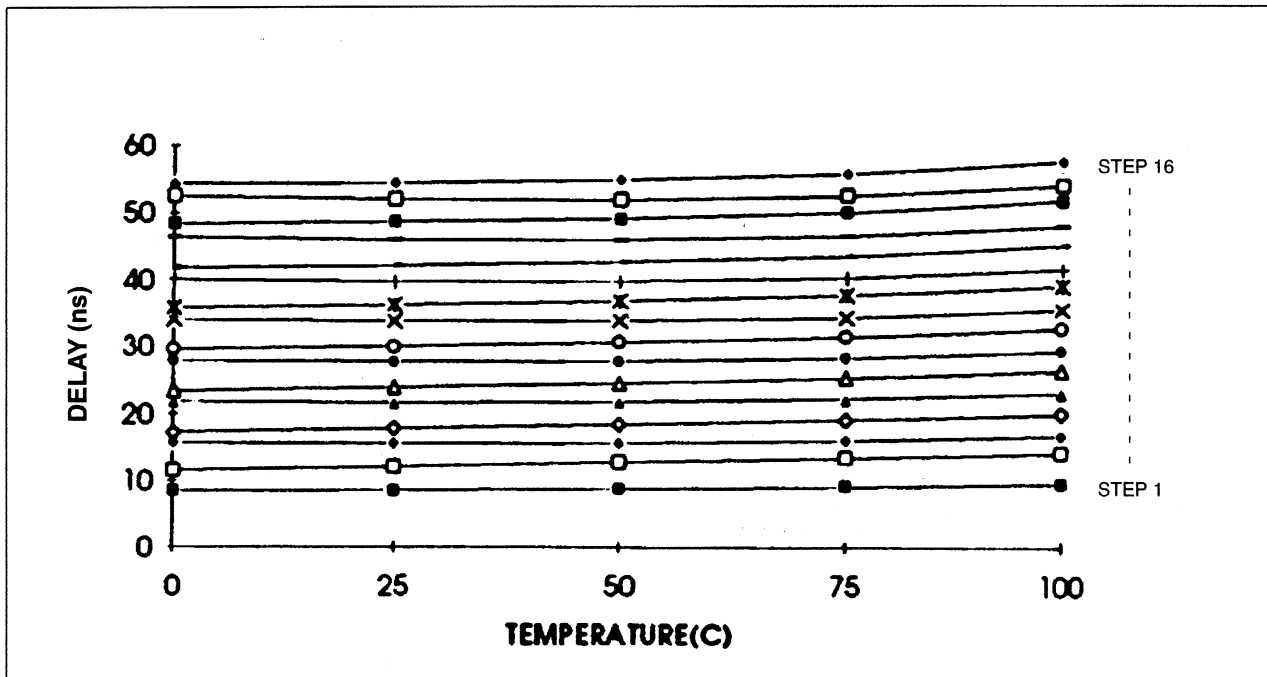
DS1045-3 SIDE A RISING EDGE SIGNAL @ VOLTAGE = 4.75 VOLTS



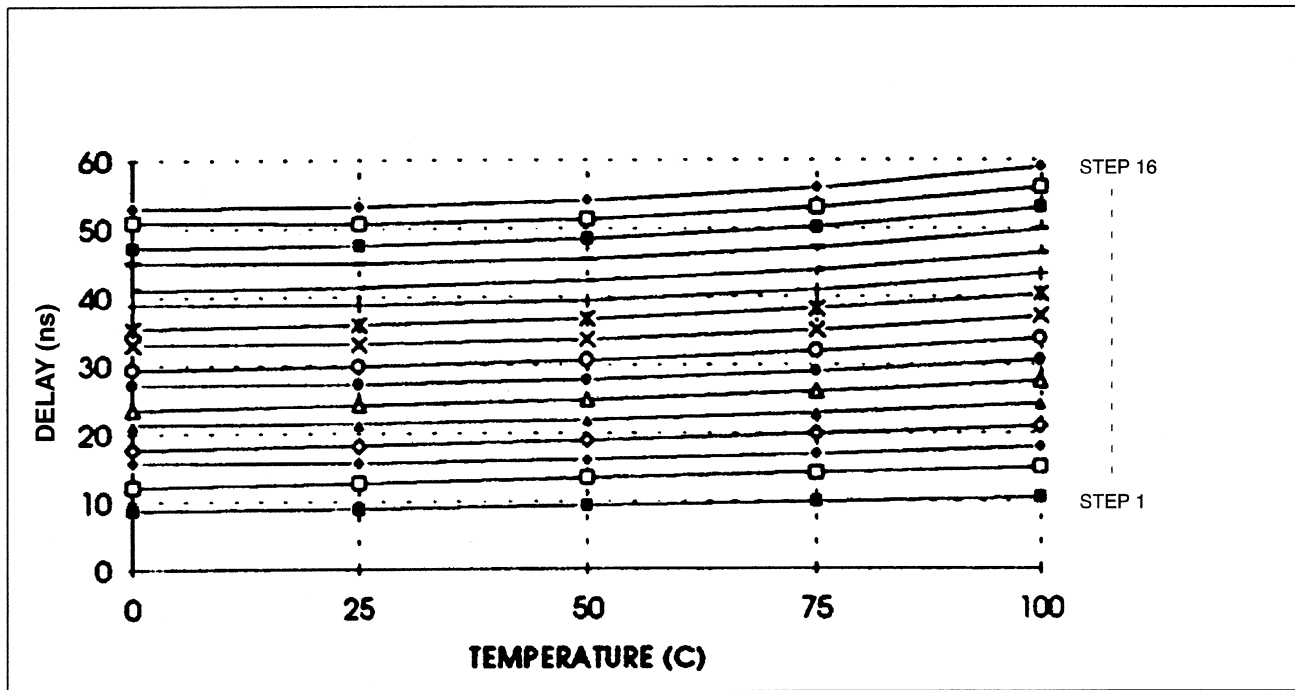
PROGRAM STEP	DELAY (ns)				
	0°C	25°C	50°C	75°C	100°C
1	8.474	8.629	9.005	9.506	10.063
2	11.587	12.223	12.966	13.769	14.602
3	15.260	15.205	15.667	16.453	17.453
4	17.075	17.678	18.491	19.468	20.632
5	21.084	21.150	21.703	22.675	24.042
6	22.963	23.576	24.496	25.674	27.182
7	26.874	26.910	27.504	28.661	30.333
8	28.820	29.393	30.340	31.674	33.528
9	32.791	32.774	33.409	34.722	36.744
10	34.957	35.502	36.512	38.035	40.193
11	38.597	38.529	39.189	40.651	42.948
12	40.635	41.125	42.133	43.787	46.259
13	44.614	44.486	45.150	46.728	49.368
14	46.891	47.321	48.367	50.188	53.020
15	50.397	50.197	50.868	52.569	55.463
16	52.545	52.878	53.918	55.857	58.977

DELAY VS. TEMPERATURE**DS1045-3 SIDE A RISING EDGE SIGNAL @ VOLTAGE = 5.00 VOLTS**

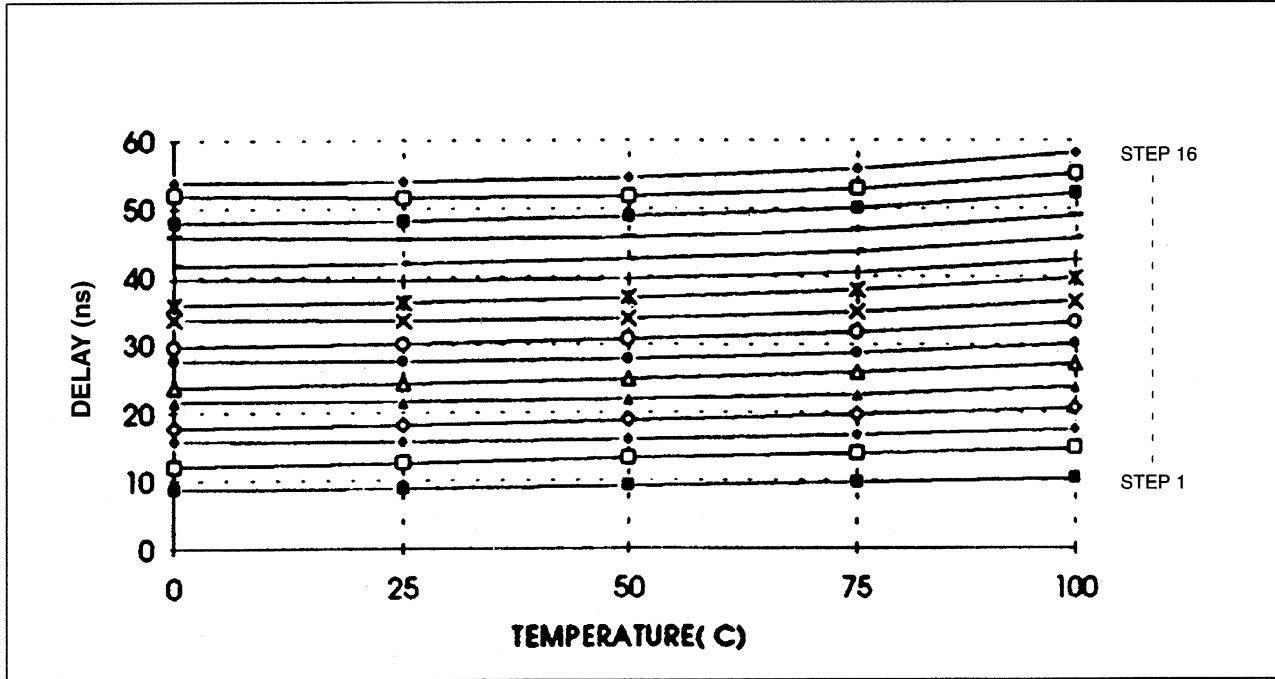
PROGRAM STEP	DELAY (ns)				
	0°C	25°C	50°C	75°C	100°C
1	8.546	8.594	8.898	9.33	9.835
2	11.539	12.162	12.869	13.619	14.388
3	15.459	15.341	15.622	16.217	17.056
4	17.179	17.716	18.449	19.293	20.333
5	21.45	21.378	21.698	22.413	23.515
6	23.168	23.713	24.491	25.46	26.761
7	27.362	27.241	27.567	28.381	29.717
8	29.151	29.638	30.405	31.46	33.01
9	33.405	33.22	33.535	34.442	36.035
10	35.399	35.852	36.646	37.805	39.591
11	39.357	39.107	39.402	40.381	42.179
12	41.217	41.592	42.342	43.57	45.603
13	45.492	45.185	45.442	46.491	48.56
14	47.597	47.914	48.667	49.989	52.243
15	51.413	51.04	51.272	52.368	54.579
16	53.398	53.622	54.304	55.676	58.13

DELAY VS. TEMPERATURE**DS1045-3 SIDE A RISING EDGE SIGNAL @ VOLTAGE = 5.25 VOLTS**

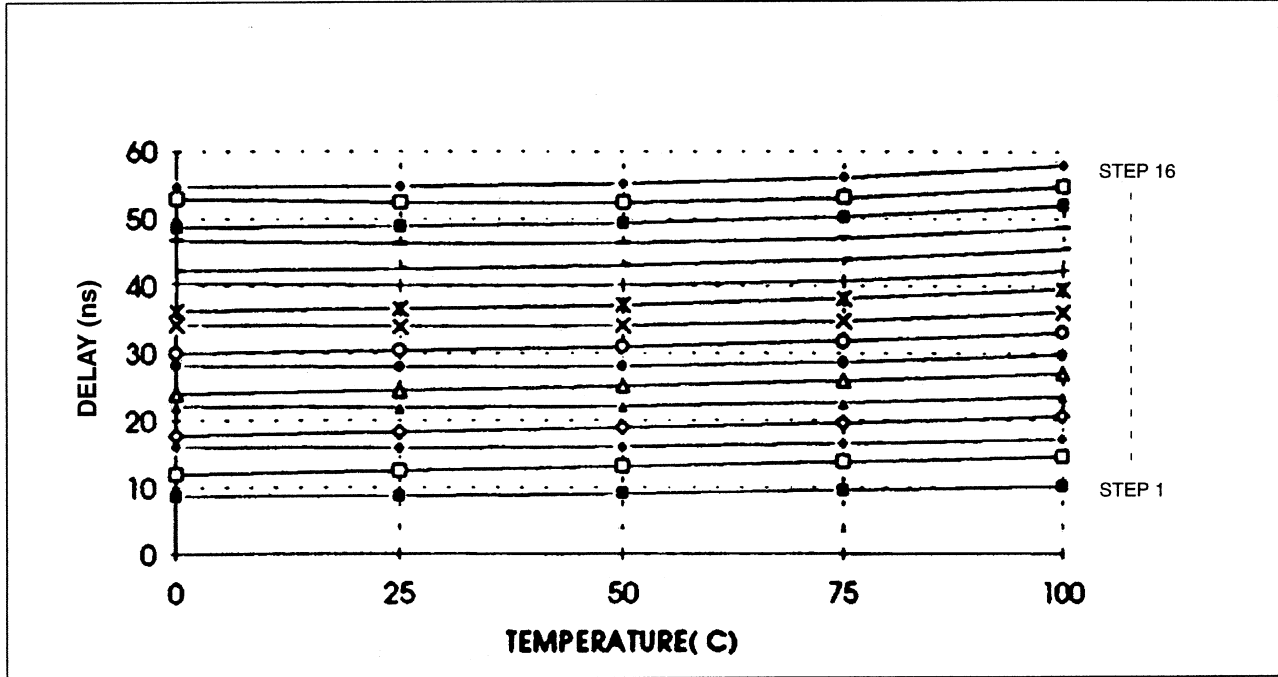
PROGRAM STEP	DELAY (ns)				
	0°C	25°C	50°C	75°C	100°C
1	8.545	8.579	8.829	9.202	9.658
2	11.542	12.114	12.801	13.515	14.257
3	15.695	15.531	15.681	16.134	16.811
4	17.264	17.814	18.478	19.234	20.153
5	21.815	21.674	21.834	22.348	23.227
6	23.400	23.911	24.598	25.428	26.555
7	27.856	27.666	27.799	28.37	29.406
8	29.512	29.956	30.612	31.476	32.787
9	34.033	33.764	33.863	34.482	35.715
10	35.881	36.304	36.943	37.895	39.354
11	40.136	39.793	39.848	40.509	41.879
12	41.824	42.154	42.759	43.715	45.358
13	46.388	45.981	46.010	46.679	48.235
14	48.349	48.619	49.181	50.196	51.990
15	52.467	51.979	51.963	52.651	54.331
16	54.285	54.453	54.963	55.975	57.906

DELAY VS. TEMPERATURE**DS1045-3 SIDE A FALLING EDGE SIGNAL @ VOLTAGE = 4.75 VOLTS**

PROGRAM STEP	DELAY (ns)				
	0°C	25°C	50°C	75°C	100°C
1	8.741	8.901	9.368	9.941	10.558
2	12.066	12.637	13.352	14.115	14.922
3	15.645	15.565	16.071	16.874	17.899
4	17.586	18.14	18.924	19.864	21.012
5	21.306	21.378	21.949	22.954	24.33
6	23.517	24.096	24.944	26.075	27.575
7	27.156	27.195	27.814	29.006	30.682
8	29.296	29.806	30.697	31.968	33.814
9	33.025	33.018	33.677	35.03	37.076
10	35.355	35.81	36.736	38.201	40.341
11	38.887	38.816	39.464	40.95	43.304
12	41.014	41.387	42.317	43.916	46.385
13	44.944	44.822	45.493	47.119	49.784
14	47.186	47.499	48.439	50.169	52.938
15	50.828	50.618	51.28	53.015	55.946
16	52.914	53.122	54.036	55.895	58.934

DELAY VS. TEMPERATURE**DS1045-3 SIDE A FALLING EDGE SIGNAL @ VOLTAGE = 5.00 VOLTS**

PROGRAM STEP	DELAY (ns)				
	0°C	25°C	50°C	75°C	100°C
1	8.721	8.817	9.210	9.724	10.300
2	12.031	12.565	13.245	13.967	14.722
3	15.825	15.689	15.994	16.616	17.485
4	17.687	18.185	18.874	19.691	20.699
5	21.681	21.591	21.926	22.667	23.797
6	23.736	24.242	24.943	25.881	27.152
7	27.649	27.514	27.851	28.704	30.083
8	29.638	30.065	30.766	31.783	33.299
9	33.651	33.451	33.787	34.721	36.371
10	35.812	36.206	36.887	37.994	39.729
11	39.638	39.384	39.683	40.678	42.51
12	41.601	41.904	42.547	43.717	45.677
13	45.846	45.512	45.789	46.832	48.914
14	47.913	48.146	48.756	50.001	52.144
15	51.867	51.459	51.682	52.79	55.052
16	53.801	53.903	54.460	55.745	58.141

DELAY VS. TEMPERATURE**DS1045-3 SIDE A FALLING EDGE SIGNAL @ VOLTAGE = 5.25 VOLTS**

PROGRAM STEP	DELAY (ns)				
	0°C	25°C	50°C	75°C	100°C
1	8.713	8.76	9.091	9.547	10.079
2	11.987	12.505	13.173	13.856	14.563
3	16.143	15.884	16.05	16.494	17.216
4	17.767	18.269	18.901	19.621	20.528
5	22.07	21.893	22.052	22.578	23.501
6	23.963	24.438	25.058	25.85	26.94
7	28.182	27.936	28.091	28.67	29.769
8	29.992	30.392	30.986	31.807	33.08
9	34.287	33.999	34.111	34.749	36.022
10	36.31	36.652	37.211	38.093	39.511
11	40.423	40.067	40.128	40.775	42.204
12	42.224	42.477	42.985	43.875	45.467
13	46.739	46.318	46.346	47.033	48.62
14	48.669	48.854	49.31	50.238	51.973
15	52.909	52.401	52.379	53.062	54.774
16	54.702	54.754	55.151	56.081	57.944

DELAY VS. TEMPERATURE**DS1045-4**

The following table indicates the performance of the DS1045-4 Programmable Delay. The plotted data is similar to the plots obtained for the DS1045-3. All steps are monotonic and show consistent variations with voltage and temperature.

DS1045-4 LOT#: 22804, DATE CODE: 4292A1

V_{CC}=4.75 VOLTS RISING EDGE

PROGRAM STEP	DELAY (ns)				
	0°C	25°C	50°C	75°C	100°C
1	7.775	7.923	8.361	8.880	9.450
2	11.547	11.545	11.933	12.640	13.55
3	15.751	16.140	16.656	17.281	18.041
4	19.229	19.264	19.632	20.328	21.270
5	23.533	23.973	24.485	25.097	25.931
6	27.207	27.283	27.637	28.332	29.353
7	31.417	31.844	32.287	32.850	33.697
8	35.129	35.202	35.479	36.124	37.175
9	39.374	39.817	40.226	40.763	41.667
10	43.061	43.172	43.449	44.118	45.229
11	47.382	47.811	48.136	48.597	49.490
12	50.877	51.000	51.213	51.823	52.970
13	55.357	55.797	56.087	56.518	57.462
14	59.099	59.227	59.417	60.014	61.238
15	63.287	63.690	63.842	64.194	65.131
16	67.211	67.337	67.442	67.943	69.168

DS1045-4 LOT#: 22804, DATE CODE: 4292A1

V_{CC}=5.0 VOLTS RISING EDGE

PROGRAM STEP	DELAY (ns)				
	0°C	25°C	50°C	75°C	100°C
1	7.622	7.784	8.169	8.642	9.184
2	11.941	11.878	12.076	12.561	13.347
3	15.584	15.953	16.451	17.022	17.714
4	19.708	19.654	19.791	20.278	21.075
5	23.363	23.816	24.304	24.858	25.596
6	27.671	27.677	27.817	28.3	29.164
7	31.23	31.699	32.142	32.649	33.39
8	35.585	35.626	35.705	36.149	37.005
9	39.171	39.691	40.115	40.599	41.361
10	43.503	43.609	43.698	44.143	45.058
11	47.187	47.737	48.083	48.486	49.233
12	51.306	51.455	51.501	51.89	52.834
13	55.136	55.727	56.058	56.437	57.202
14	59.525	59.706	59.745	60.123	61.101
15	63.073	63.659	63.884	64.182	64.928
16	67.635	67.843	67.822	68.131	69.081

V_{CC}=5.25 VOLTS RISING EDGE

PROGRAM STEP	DELAY (ns)				
	0°C	25°C	50°C	75°C	100°C
1	7.510	7.668	8.015	8.453	8.957
2	12.359	12.304	12.378	12.696	13.329
3	15.445	15.82	16.297	16.824	17.465
4	20.203	20.156	20.178	20.452	21.096
5	23.215	23.69	24.175	24.683	25.355
6	28.143	28.19	28.225	28.507	29.174
7	31.064	31.596	32.056	32.529	33.178
8	36.051	36.165	36.159	36.404	37.067
9	39.010	39.614	40.062	40.517	41.17
10	43.933	44.152	44.177	44.420	45.134
11	47.004	47.672	48.098	48.475	49.104
12	51.734	52.003	52.015	52.241	52.949
13	54.945	55.683	56.095	56.447	57.101
14	59.929	60.281	60.306	60.493	61.23
15	62.861	63.646	63.984	64.276	64.886
16	68.064	68.472	68.446	68.577	69.271

DS1045-4 LOT#: 22804, DATE CODE: 4292A1**V_{CC}=4.75 VOLTS FALLING EDGE**

PROGRAM STEP	DELAY (ns)				
	0°C	25°C	50°C	75°C	100°C
1	7.996	8.349	8.944	9.58	10.236
2	11.924	11.926	12.359	13.069	13.979
3	16.287	16.674	17.213	17.859	18.638
4	19.568	19.611	20.008	20.705	21.657
5	24.109	24.565	25.077	25.705	26.576
6	27.496	27.529	27.863	28.545	29.537
7	32.092	32.543	32.986	33.566	34.432
8	35.557	35.564	35.813	36.436	37.431
9	39.881	40.374	40.818	41.422	42.346
10	43.588	43.616	43.831	44.436	45.47
11	47.817	48.307	48.66	49.203	50.163
12	51.395	51.414	51.549	52.099	53.154
13	56.12	56.603	56.917	57.417	58.412
14	59.297	59.33	59.456	59.977	61.117
15	63.943	64.415	64.64	65.068	66.065
16	67.238	67.244	67.285	67.73	68.877

V_{CC}=5.00 VOLTS FALLING EDGE

PROGRAM STEP	DELAY (ns)				
	0°C	25°C	50°C	75°C	100°C
1	7.794	8.145	8.698	9.297	9.912
2	12.311	12.233	12.432	12.945	13.732
3	16.093	16.491	16.994	17.587	18.297
4	20.018	19.957	20.127	20.622	21.442
5	23.88	24.383	24.876	25.46	26.225
6	27.944	27.904	28.026	28.49	29.329
7	31.854	32.387	32.826	33.354	34.114
8	36.017	35.986	36.029	36.429	37.259
9	39.641	40.226	40.672	41.216	42.045
10	44.04	44.051	44.068	44.455	45.315
11	47.564	48.164	48.559	49.044	49.861
12	51.824	51.857	51.821	52.172	53.021
13	55.838	56.478	56.848	57.291	58.132
14	59.709	59.782	59.757	60.099	60.973
15	63.662	64.338	64.627	64.997	65.83
16	67.644	67.735	67.628	67.891	68.808

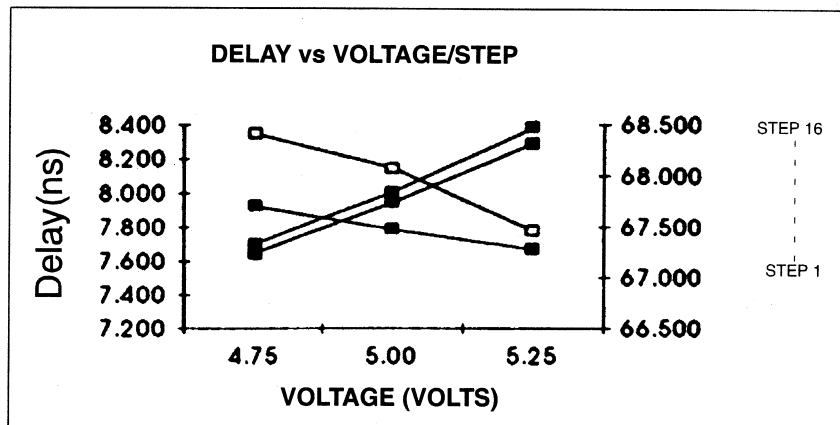
V_{CC}=5.25 VOLTS FALLING EDGE

PROGRAM STEP	DELAY (ns)				
	0°C	25°C	50°C	75°C	100°C
1	7.622	7.94	8.481	9.05	9.649
2	12.668	12.594	12.683	13.016	13.659
3	15.9	16.335	16.822	17.368	18.023
4	20.457	20.417	20.446	20.749	21.411
5	23.694	24.23	24.723	25.263	25.961
6	28.397	28.392	28.393	28.664	29.308
7	31.634	32.24	32.711	33.202	33.885
8	36.456	36.496	36.443	36.661	37.305
9	39.416	40.091	40.579	41.084	41.821
10	44.454	44.558	44.502	44.717	45.384
11	47.314	48.057	48.506	48.966	49.688
12	52.26	52.417	52.335	52.496	53.141
13	55.586	56.39	56.844	57.261	57.985
14	60.119	60.348	60.284	60.437	61.135
15	63.412	64.272	64.682	65.038	65.741
16	68.048	68.321	68.216	68.314	68.996

DS1045-4 DELAY VS. VOLTAGE CHARACTERISTICS

The following chart indicates how the DS1045-4 delay changes for the positive and negative edges of step 1 and step 16 over voltage variations of 5 volts $\pm 5\%$. For step 1, the falling edge starts at 7.923 ns and declines to 7.579 ns over an increasing voltage. The rising edge of step 1 follows a similar curve. For step 16, the slope is positive for increasing voltage. The exact values for each device are indicated in the following tables. Characteristics for the DS1045-3 and 5 are similar to the DS1045-4.

DS1045-4 GRAPH



DS1045-3 STEP DELAY VARIATION VS. VOLTAGE

VOLTAGE (volts)	4.75V	5.00V	5.25V
Programming Step 1 Falling Edge	8.629	8.594	8.579
Programming Step 1 Rising Edge	8.901	8.817	8.760
Programming Step 16 Falling Edge	52.878	53.622	55.346
Programming Step 16 Rising Edge	53.122	53.903	55.675

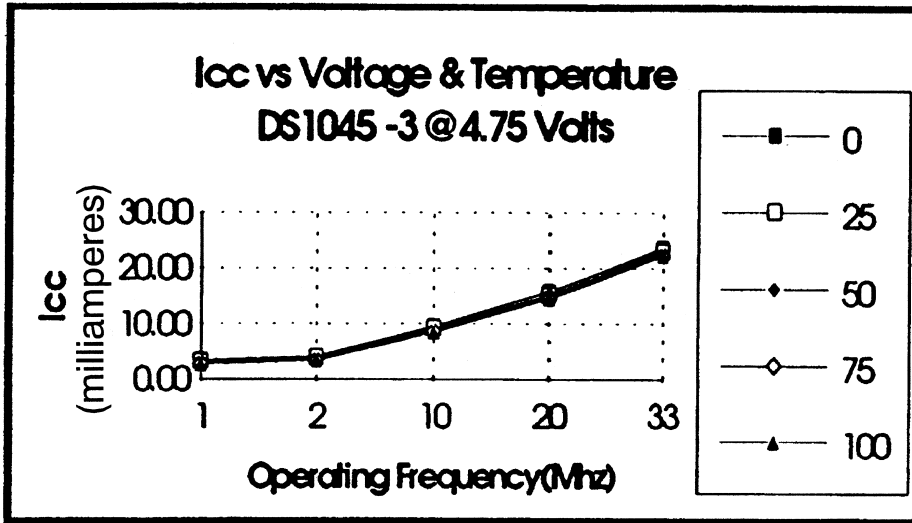
DS1045-4 STEP DELAY VARIATION VS. VOLTAGE

VOLTAGE (volts)	4.75V	5.00V	5.25V
Programming Step 1 Falling Edge	7.923	7.784	7.579
Programming Step 1 Rising Edge	8.349	8.145	7.940
Programming Step 16 Falling Edge	67.337	67.843	68.472
Programming Step 16 Rising Edge	67.244	67.735	68.321

DS1045-5 STEP DELAY VARIATION VS. VOLTAGE

VOLTAGE (volts)	4.75V	5.00V	5.25V
Programming Step 1 Falling Edge	7.817	7.681	7.574
Programming Step 1 Rising Edge	8.213	8.005	7.815
Programming Step 16 Falling Edge	82.506	82.961	82.395
Programming Step 16 Rising Edge	82.958	83.363	83.720

OPERATING CURRENT VS. FREQUENCY



DS1045-3 @ 4.75 VOLTS

FREQUENCY	I _{cc} (MA)				
	TEMPERATURE				
	0°C	25°C	50°C	75°C	100°C
1 MHz	3.41	3.22	3.02	2.88	2.75
2 MHz	4.11	3.89	3.68	3.54	3.41
10 MHz	9.59	9.15	8.83	8.66	8.52
20 MHz	15.83	15.18	14.86	14.75	14.69
33 MHz	23.65	23.02	22.63	22.34	22.32

DS1045-3 @ 5.00 VOLTS

FREQUENCY	I _{cc} (MA)				
	TEMPERATURE				
	0°C	25°C	50°C	75°C	100°C
1 MHz	3.69	3.48	3.26	3.11	2.97
2 MHz	4.45	4.20	3.98	3.82	3.68
10 MHz	10.37	9.89	9.56	9.35	9.18
20 MHz	17.10	16.37	15.98	15.81	15.77
33 MHz	25.41	24.63	24.34	24.07	23.81

DS1045-3 @ 5.25 VOLTS

FREQUENCY	I _{cc} (MA)				
	TEMPERATURE				
	0°C	25°C	50°C	75°C	100°C
1 MHz	4.02	3.78	3.53	3.37	3.22
2 MHz	4.83	4.55	4.30	4.13	3.98
10 MHz	11.21	10.68	10.31	10.01	9.89
20 MHz	18.44	17.63	17.17	16.96	16.83
33 MHz	27.26	26.29	26.03	25.80	25.53

TEST CONSIDERATIONS

The DS1045 is a high speed device and as such care should be exercised when testing. Good ground planes and power supply decoupling techniques should be used. It is also required that pin 2 be connected to V_{CC} . A precision time interval counter is required with test resolution ten times better than the required data measurement.

TEST CONDITIONS

Input source: 50 ohms maximum with measurements taken at the 1.5 volt level.

Input signal pulse of 250 ns and a period of 1 ms.

Rise and Fall times of 3 ns between 0.6 and 3.0 volts.

Load Capacitance = 15 pF.

APPLICATIONS

The ability to use the DS1045 Dual Programmable Delay Line in multiple delay line applications makes it unique in the industry. It not only allows you to reduce inventory cost by having a lower number of parts in stock, but it also affords the designer the ability to improve system performance much later in the design cycle. All of the usual applications for delay lines are applicable to this part, but with much greater flexibility.

CAUTION

A word of caution is in order when loading the input delay registers with the binary value of the desired delay function. In order to insure that the input signal integrity is maintained after the register has been loaded, the input signal must be allowed to propagate through the DS1045 for at least twice the selected delay value. For example, if you were using the DS1045-3, and selected a binary 8, then you should allow at least 32 ns times 2 or 64 ns before the input integrity is established.