DS5000FP
Soft Microprocessor Chip

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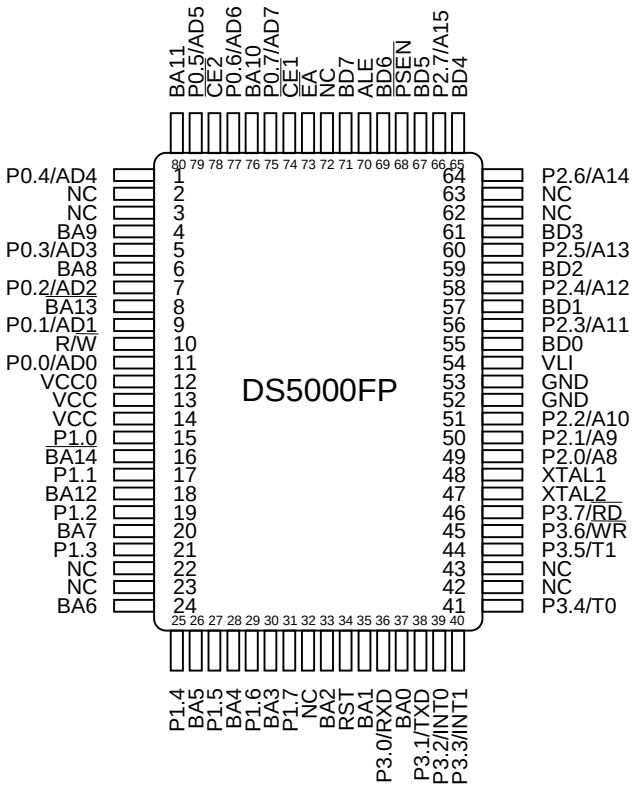
FEATURES

- 8051-compatible microprocessor adapts to its task
  - Accesses between 8 and 64 kbytes of nonvolatile SRAM
  - In-system programming via on-chip serial port
  - Can modify its own program or data memory
  - Accesses memory on a separate Byte-wide bus
- Crashproof operation
  - Maintains all nonvolatile resources for over 10 years
  - Power-fail Reset
  - Early Warning Power-fail Interrupt
  - Watchdog Timer
  - User-supplied lithium battery backs user SRAM for program/data storage
- Software security
  - Executes encrypted programs to prevent observation
  - Security lock prevents download
  - Unlocking destroys contents
- Fully 8051-compatible
  - 128 bytes scratchpad RAM
  - Two timer/counters
  - On-chip serial port
  - 32 parallel I/O port pins

PIN ASSIGNMENT



DESCRIPTION

The DS5000FP Soft Microprocessor Chip is an 8051-compatible processor based on nonvolatile RAM technology. It is substantially more flexible than a standard 8051, yet provides full compatibility with the 8051 instruction set, timers, serial port, and parallel I/O ports. By using NV RAM instead of ROM, the user can program, then reprogram the microcontroller while in-system. The application software can even change its own operation. This allows frequent software upgrades, adaptive programs, customized systems, etc. In addition, by using NV SRAM, the DS5000FP is ideal for data logging applications. It connects easily to a Dallas Real Time Clock for time stamp and date.

The DS5000FP provides the benefits of NV RAM without using I/O resources. It uses a non-multiplexed Byte-wide address and data bus for memory access. This bus can perform all memory access and

provides decoded chip enables for SRAM. This leaves the 32 I/O port pins free for application use. The DS5000FP uses ordinary SRAM and battery backs the memory contents with a user's external lithium cell. Data is maintained for over 10 years with a very small lithium cell. A DS5000FP also provides crashproof operation in portable systems or systems with unreliable power. These features include the ability to save the operating state, Power-fail Reset, Power-fail Interrupt, and Watchdog Timer.

A user loads programs into the DS5000FP via its on-chip Serial Bootstrap Loader. This function supervises the loading of code into NV RAM, validates it, then becomes transparent to the user. Software can be stored in an 8-kbyte or 32-kbyte CMOS SRAM. Using its internal Partitioning, the DS5000FP will divide this common RAM into user programmable code and data segments. This Partition can be selected at program loading time, but can be modified anytime later. It will decode memory access to the SRAM, communicate via its Byte-wide bus and write-protect the memory portion designated as ROM. Combining program and data storage in one device saves board space and cost. The DS5000FP can also access a second 32 kbytes of NV RAM but this area is restricted to data memory. For a user that wants a pre-constructed module using the DS5000FP, RAM, lithium cell, and optional real time clock; the DS2250(T) and DS5000(T) are available and described in separate data sheets. More details are also contained in the User's Guide section of the Secure Microcontroller Data Book.

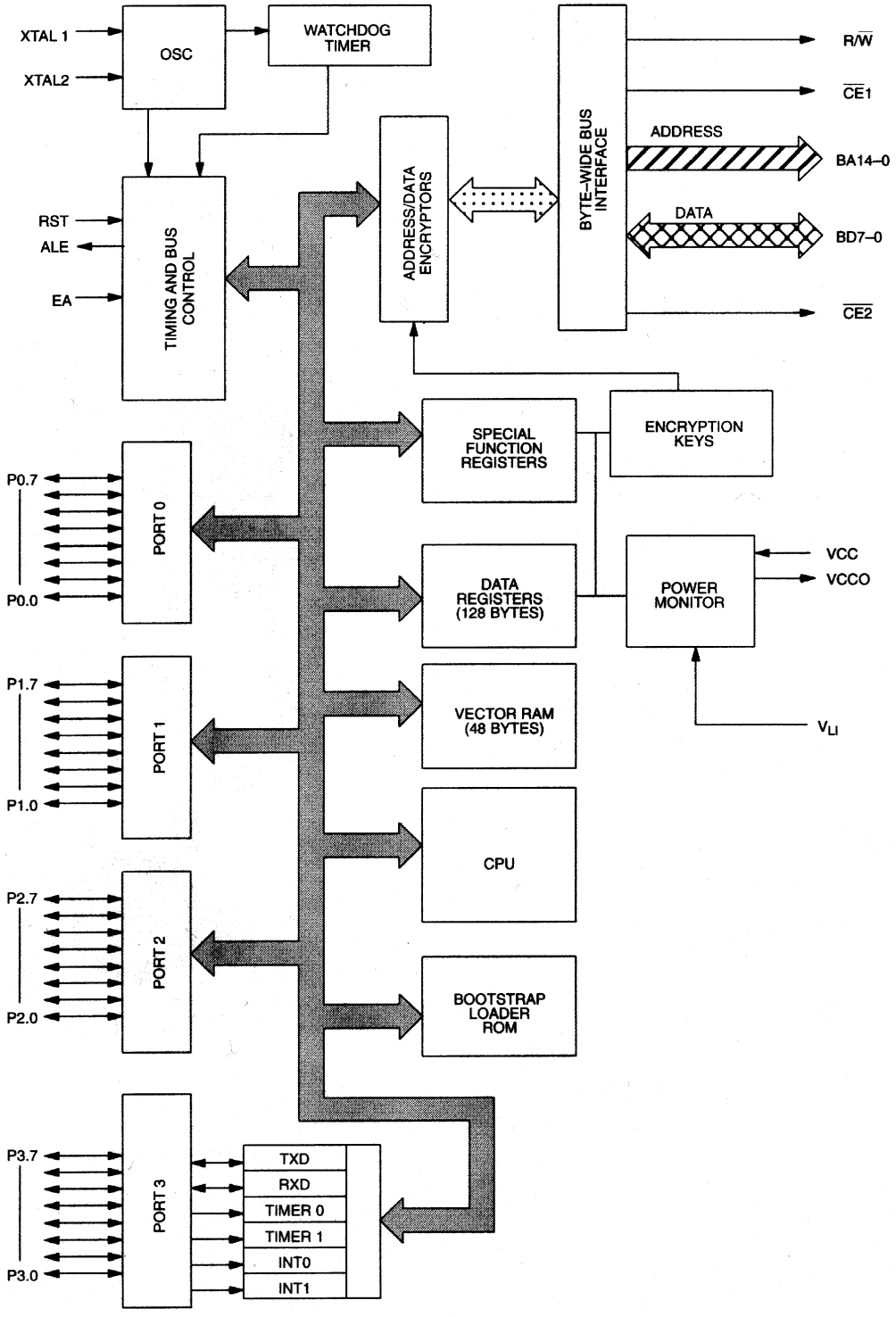
ORDERING INFORMATION

The following devices are available as standard products from Dallas Semiconductor:

PART #	DESCRIPTION
DS5000FP-16	80-pin QFP, Max. clock speed 16 MHz, 0° to 70°C operation

Operating information is contained in the User's Guide section of the Secure Microcontroller Data Book. This data sheet provides ordering information, pin-out, and electrical specifications.

DS5000FP BLOCK DIAGRAM Figure 1



PIN DESCRIPTION

PIN	DESCRIPTION
15, 17, 19, 21, 25, 27, 29, 31	**P1.0 - P1.7.** General purpose I/O Port 1.
34	**RST** - Active high reset input. A logic 1 applied to this pin will activate a reset state. This pin is pulled down internally so this pin can be left unconnected if not used.
36	**P3.0 RXD.** General purpose I/O port pin 3.0. Also serves as the receive signal for the on board UART. This pin should not be connected directly to a PC COM port.
38	**P3.1 TXD.** General purpose I/O port pin 3.1. Also serves as the transmit signal for the on board UART. This pin should not be connected directly to a PC COM port.
39	**P3.2 $\overline{\text{INT0}}$.** General purpose I/O port pin 3.2. Also serves as the active low External Interrupt 0.
40	**P3.3 $\overline{\text{INT1}}$.** General purpose I/O port pin 3.3. Also serves as the active low External Interrupt 1.
41	**P3.4 T0.** General purpose I/O port pin 3.4. Also serves as the Timer 0 input.
44	**P3.5 T1.** General purpose I/O port pin 3.5. Also serves as the Timer 1 input.
45	**P3.6 $\overline{\text{WR}}$.** General purpose I/O port pin. Also serves as the write strobe for Expanded bus operation.
46	**P3.7 $\overline{\text{RD}}$.** General purpose I/O port pin. Also serves as the read strobe for Expanded bus operation.
47, 48	**XTAL2, XTAL1.** Used to connect an external crystal to the internal oscillator. XTAL1 is the input to an inverting amplifier and XTAL2 is the output.
52, 53	**GND.** Logic ground.
49, 50, 51, 56, 58, 60, 64, 66	**P2.0-P2.7.** General purpose I/O Port 2. Also serves as the MSB of the Expanded Address bus.
68	**$\overline{\text{PSEN}}$** - Program Store Enable. This active low signal is used to enable an external program memory when using the Expanded bus. It is normally an output and should be unconnected if not used. $\overline{\text{PSEN}}$ is also used to invoke the Bootstrap Loader. At this time, $\overline{\text{PSEN}}$ will be pulled down externally. This should only be done once the DS5000FP is already in a reset state. The device that pulls down should be open drain since it must not interfere with $\overline{\text{PSEN}}$ under normal operation.
70	**ALE** - Address Latch Enable. Used to de-multiplex the multiplexed Expanded Address/Data bus on Port 0. This pin is normally connected to the clock input on a ’373 type transparent latch. When using a parallel programmer, this pin also assumes the $\overline{\text{PROG}}$ function for programming pulses.
73	**$\overline{\text{EA}}$** - External Access. This pin forces the DS5000FP to behave like an 8031. No internal memory (or clock) will be available when this pin is at a logic low. Since this pin is pulled down internally, it should be connected to +5V to use NV RAM. In a parallel programmer, this pin also serves as V_{PP} for super voltage pulses.

PIN	DESCRIPTION
11, 9, 7, 5, 1, 79, 77, 75	**P0.0-P0.7.** General purpose I/O Port 0. This port is open-drain and can not drive a logic 1. It requires external pullups. Port 0 is also the multiplexed Expanded Address/Data bus. When used in this mode, it does not require pullups.
13, 14	**V_{CC} - +5V**
16, 8, 18, 80, 76, 4, 6, 20, 24, 26, 28, 30, 33, 35, 37	**BA14-0.** Byte-wide Address bus bits 14-0. This 15 bit bus is combined with the non-multiplexed data bus (BD7-0) to access NV SRAM. Decoding is performed on $\overline{CE1}$ and $\overline{CE2}$. Read/write access is controlled by R/$\overline{W}$. BA14-0 connect directly to an 8k or 32k SRAM. If an 8k RAM is used, BA13 and BA14 will be unconnected. Note BA13 and BA14 are inverted from the true logical address. Also note that BA14 is lithium backed.
71, 69, 67, 65, 61, 59, 57, 55	**BD7-0.** Byte-wide Data bus bits 7-0. This 8-bit bi-directional bus is combined with the non-multiplexed address bus (BA14-0) to access NV SRAM. Decoding is performed on $\overline{CE1}$ and $\overline{CE2}$. Read/write access is controlled by R/W. BD7-0 connect directly to an 8k or 32k SRAM, and optionally to a Real-time Clock.
10	**R/W -** Read/Write. This signal provides the write enable to the SRAMs on the Byte-wide bus. It is controlled by the memory map and Partition. The blocks selected as Program (ROM) will be write protected.
74	**$\overline{CE1}$ -** Chip Enable 1. This is the primary decoded chip enable for memory access on the Byte-wide bus. It connects to the chip enable input of one SRAM. $\overline{CE1}$ is lithium backed. It will remain in a logic high inactive state when V_{CC} falls below V_{LI}.
78	**$\overline{CE2}$ -** Chip Enable 2. This chip enable is provided to bank switch to a second block of 32k bytes of nonvolatile data memory. It connects to the chip enable input of one SRAM or one lithium-backed peripheral such a DS1283 clock. $\overline{CE2}$ is lithium backed. It will remain in a logic high inactive state when V_{CC} falls below V_{LI}.
12	**V_{CCO} -** V_{CC} Output. This is switched between V_{CC} and V_{LI} by internal circuits based on the level of V_{CC}. When power is above the lithium input, power will be drawn from V_{CC}. The lithium cell remains isolated from a load. When V_{CC} is below V_{LI}, the V_{CCO} switches to the V_{LI} source. V_{CCO} is connected to the V_{CC} pin of an SRAM.
54	**V_{LI}L -** Lithium Voltage Input. Connect to a lithium cell greater than V_{LImin} and no greater than V_{LImax} as shown in the electrical specifications. Nominal value is +3V.
2, 3, 22, 23, 32, 42, 43, 62, 63, 72	**NC do not connect.**

INSTRUCTION SET

The DS5000FP executes an instruction set that is object code compatible with the industry standard 8051 microcontroller. As a result, software development packages such as assemblers and compilers that have been written for the 8051 are compatible with the DS5000FP. A complete description of the instruction set and operation are provided in the User's Guide section of the Secure Microcontroller Data Book.

Also note that the DS5000FP is embodied in the DS5000(T) and DS2250(T) modules. The DS5000(T) combines the DS5000FP with one SRAM of either 8 or 32 kbytes and a lithium cell. An optional Real Time Clock is also available in the DS5000T. This is packaged in a 40-pin DIP module. The DS2250(T)

is an identical function in a SIMM form factor. It also offers the option of a second 32k SRAM mapped as data on Chip Enable 2.

MEMORY ORGANIZATION

Figure 2 illustrates the memory map accessed by the DS5000FP. The entire 64k of program and 64k of data is available. The DS5000FP maps 32k of this space into the SRAM connected to the Byte-wide bus. This is the area from 0000h to 7FFFh (32k) and is reached via $\overline{CE1}$. Any area not mapped into the NV RAM is reached via the Expanded bus on Ports 0 & 2. Selecting $\overline{CE2}$ provides another 32k of potential data storage. When $\overline{CE2}$ is used, no data is available on the ports. The memory map is covered in detail in the User's Guide section of the Secure Microcontroller Data Book.

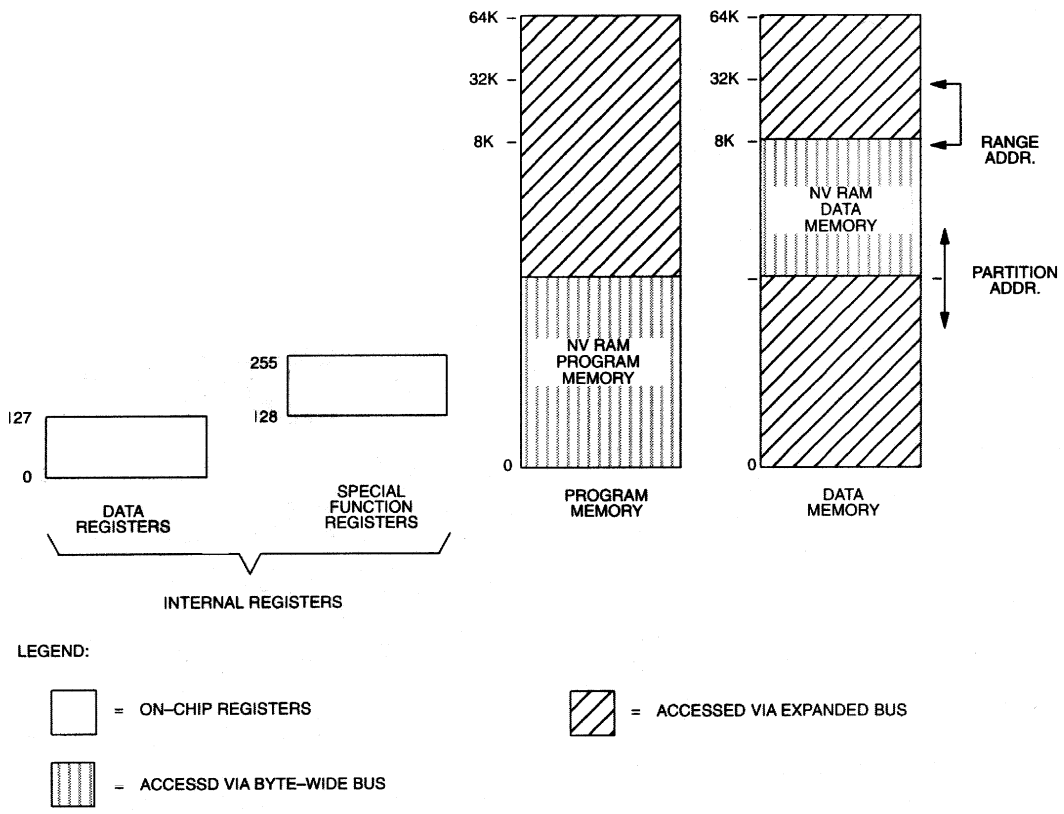
Figure 3 illustrates a typical memory connection for a system using 8k bytes of SRAM. Figure 4 shows a similar system with 32 kbytes. The Byte-wide Address bus connects to the SRAM address lines. The bi-directional Byte-wide data bus connects the data I/O lines of the SRAM. $\overline{CE1}$ provides the chip enable and R/$\overline{W}$ is the write enable. An additional RAM could be connected to $\overline{CE2}$, with common connections for R/$\overline{W}$, BA14-0, and BD7-0.

POWER MANAGEMENT

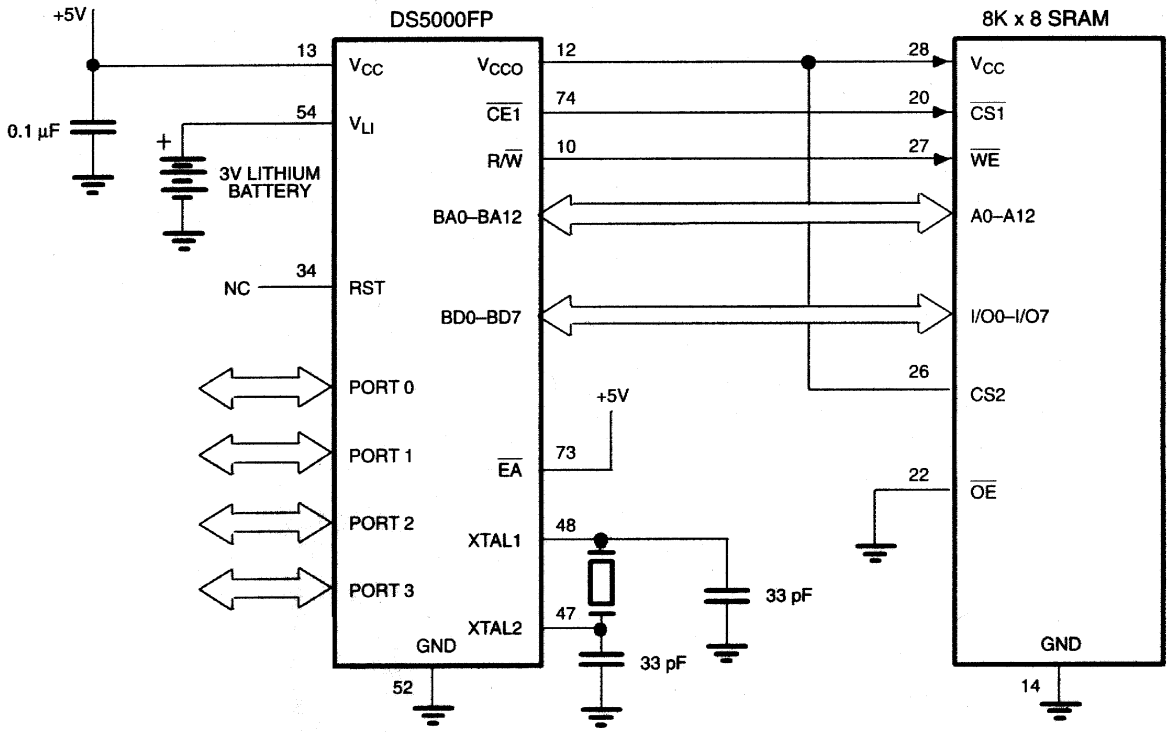
The DS5000FP monitors power to provide Power-fail Reset, early warning Power-fail Interrupt, and switch-over to lithium backup. It uses the Lithium cell at V_{LI} as a reference in determining the switch points. These are called V_{PFW}, V_{CCMIN}, and V_{LI} respectively. When V_{CC} drops below V_{PFW}, the DS5000FP will perform an interrupt vector to location 2Bh if the power-fail warning was enabled. Full processor operation continues regardless. When power falls further to V_{CCMIN}, the DS5000FP invokes a reset state. No further code execution will be performed unless power rises back above V_{CCMIN}. $\overline{CE1}$, $\overline{CE2}$, R/$\overline{W}$ go to an inactive (logic 1) state. Any address lines that are high (due to encryption) will follow V_{CC}, except for BA14, which is lithium backed. V_{CC} is still the power source at this time. When V_{CC} drops further to below V_{LI}, internal circuitry will switch to the lithium cell for power. The majority of internal circuits will be disabled and the remaining nonvolatile states will be retained. Any devices connected to V_{CCO} will be powered by the lithium cell at this time. V_{CCO} will be at the lithium battery voltage less a diode drop. This drop will vary depending on the load. Low leakage SRAMs should be used for this reason. When a module is used, the lithium cell is selected by Dallas so absolute specifications are provided for the switch thresholds. When using the DS5000FP, the user must select the appropriate battery. The following formulas apply to the switch function.

$V_{PFW} = 1.45 * V_{LI}$
$V_{CCMIN} = 1.40 * V_{LI}$
V_{LI} Switch $= 1.0 * V_{LI}$

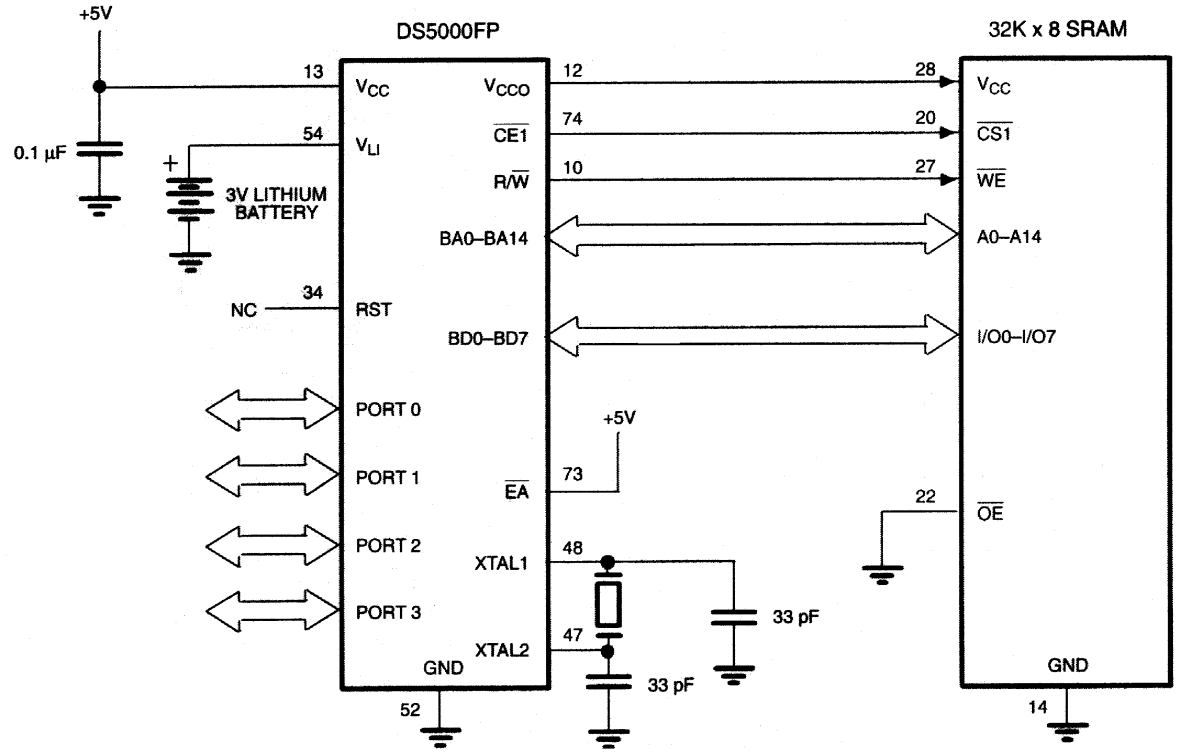
MEMORY MAP OF THE DS5000FP Figure 2



DS5000FP CONNECTION TO 8k X 8 SRAM Figure 3



DS5000FP CONNECTION TO 32k X 8 SRAM Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC CHARACTERISTICS

(t_A=0°C to70°C; V_{CC}=5V ± 5%)

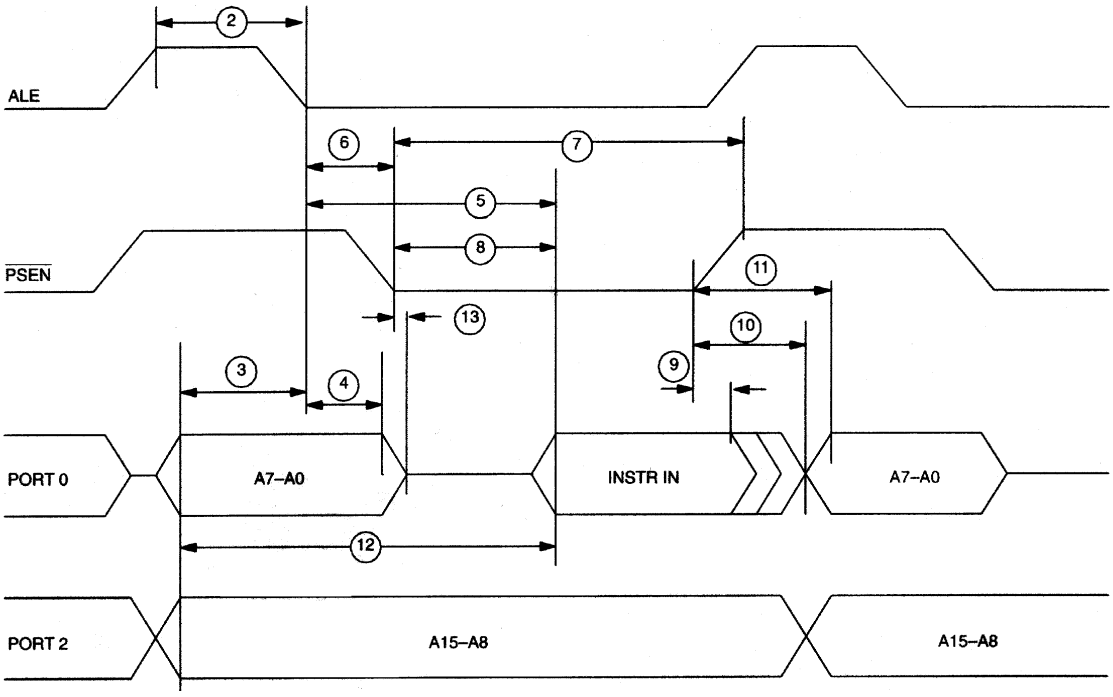
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Low Voltage	V_{IL}	-0.3		0.8	V	1
Input High Voltage	V_{IH1}	2.0		V_{CC}+0.3	V	1
Input High Voltage RST, XTAL1	V_{IH2}	3.5		V_{CC}+0.3	V	1
Output Low Voltage @ I_{OL}=1.6 mA (Ports 1, 2, 3)	V_{OL1}		0.15	0.45	V	
Output Low Voltage @ I_{OL}=3.2 mA (Ports 0, ALE, $\overline{PSEN}$, BA14-0, BD7-0, R/$\overline{W}$, $\overline{CE}$ 1-2)	V_{OL2}		0.15	0.45	V	1
Output High Voltage @ I_{OH}= -80 µA (Ports 1, 2, 3)	V_{OH1}	2.4	4.8		V	1
Output High Voltage @ I_{OH}=-400 µA (Ports 0, ALE, $\overline{PSEN}$, BA14-0, BD7-0, R/$\overline{W}$, $\overline{CE}$ 1-2)	V_{OH2}	2.4	4.8		V	1
Input Low Current V_{IN} = 0.45V (Ports 1, 2, 3)	I_{IL}			-50	µA	
Transition Current; 1 to 0 V_{IN} = 2.0V (Ports 1, 2, 3)	I_{TL}			-500	µA	
Input Leakage Current 0.45 < V_{IN} < V_{CC} (Port 0)	I_L			±10	µA	
RST, $\overline{EA}$ Pulldown Resistor	R_{RE}	40		125	kΩ	
Stop Mode Current	I_{SM}			80	µA	4
Power-Fail Warning Voltage	V_{PFW}	4.15	4.6	4.75	V	1, 6
Minimum Operating Voltage	V_{CCmin}	4.05	4.5	4.65	V	1, 6
Lithium Supply Voltage	V_{LI}	2.9		3.3	V	1
Programming Supply Voltage (Parallel Program Mode)	V_{PP}	12.5		13	V	1
Program Supply Current	I_{PP}		15	20	mA	
Operating Current @ 16 MHz	I_{CC}			36	mA	2
Idle Mode Current @ 12 MHz	I_{IDLE}			6.2	mA	3
Output Supply Voltage	V_{CCO1}	V_{CC}-0.3			V	1
Output Supply Voltage (Battery-backed mode)	V_{CCO2}	V_{LI}-0.65	V_{LI}-0.5		V	8
Output Supply Current @ V_{CCO} = V_{CC}-0.3V	I_{CCO1}		80		mA	2
Battery-Backed Quiescent Current	I_{LI}		5	75	nA	7

AC CHARACTERISTICS: EXPANDED BUS MODE TIMING SPECIFICATIONS

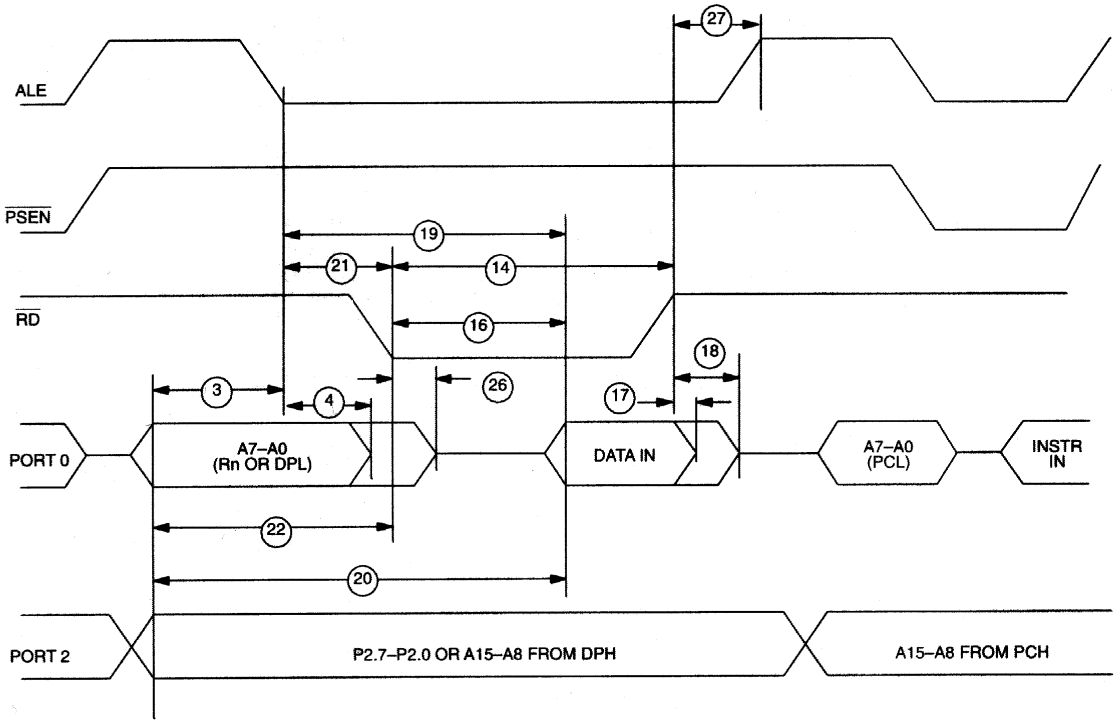
(t_A=0°C to70°C; V_{CC}=5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
1	Oscillator Frequency	$1/t_{CLK}$	1.0	16	MHz
2	ALE Pulse Width	t_{ALPW}	$2t_{CLK}$ -40		ns
3	Address Valid to ALE Low	t_{AVALL}	t_{CLK} -40		ns
4	Address Hold After ALE Low	t_{AVAAV}	t_{CLK} -35		ns
5	ALE Low to Valid Instr. In @ 12 MHz @ 16 MHz	t_{ALLVI}		$4t_{CLK}$ -150 $4t_{CLK}$ -90	ns ns
6	ALE Low to $\overline{PSEN}$ Low	t_{ALLPSL}	t_{CLK} -25		ns
7	$\overline{PSEN}$ Pulse Width	t_{PSPW}	$3t_{CLK}$ -35		ns
8	$\overline{PSEN}$ Low to Valid Instr. In @ 12 MHz @ 16 MHz	t_{PSLVI}		$3t_{CLK}$ -150 $3t_{CLK}$ -90	ns ns
9	Input Instr. Hold after $\overline{PSEN}$ Going High	t_{PSIV}	0		ns
10	Input Instr. Float after $\overline{PSEN}$ Going High	t_{PSIX}		t_{CLK} -20	ns
11	Address Hold after $\overline{PSEN}$ Going High	t_{PSAV}	t_{CLK} -8		ns
12	Address Valid to Valid Instr. In @ 12 MHz @ 16 MHz	t_{AVVI}		$5t_{CLK}$ -150 $5t_{CLK}$ -90	ns ns
13	$\overline{PSEN}$ Low to Address Float	t_{PSLAZ}	0		ns
14	$\overline{RD}$ Pulse Width	t_{RDPW}	$6t_{CLK}$ -100		ns
15	$\overline{WR}$ Pulse Width	t_{WRPW}	$6t_{CLK}$ -100		ns
16	$\overline{RD}$ Low to Valid Data In @ 12 MHz @ 16 MHz	t_{RDLDV}		$5t_{CLK}$ -165 $5t_{CLK}$ -105	ns ns
17	Data Hold after $\overline{RD}$ High	t_{RDHDV}	0		ns
18	Data Float after $\overline{RD}$ High	t_{RDHDZ}		$2t_{CLK}$ -70	ns
19	ALE Low to Valid Data In @ 12 MHz @ 16 MHz	t_{ALLVD}		8_{CLK} -150 $8t_{CLK}$ -90	ns ns
20	Valid Addr. to Valid Data In @ 12 MHz @ 16 MHz	t_{AVDV}		$9t_{CLK}$ -165 $9t_{CLK}$ -105	ns ns
21	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{ALLRDL}	$3t_{CLK}$ -50	$3t_{CLK}$ +50	ns
22	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVRDL}	$4t_{CLK}$ -130		ns
23	Data Valid to $\overline{WR}$ Going Low	t_{DVWRL}	t_{CLK} -60		ns
24	Data Valid to $\overline{WR}$ High @ 12 MHz @ 16 MHz	t_{DVWRH}	$7t_{CLK}$ -150 $7t_{CLK}$ -90		ns ns
25	Data Valid after $\overline{WR}$ High	t_{WRHDV}	t_{CLK} -50		ns
26	$\overline{RD}$ Low to Address Float	t_{RDLAZ}		0	ns
27	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{RDHALH}	t_{CLK} -40	t_{CLK} +50	ns

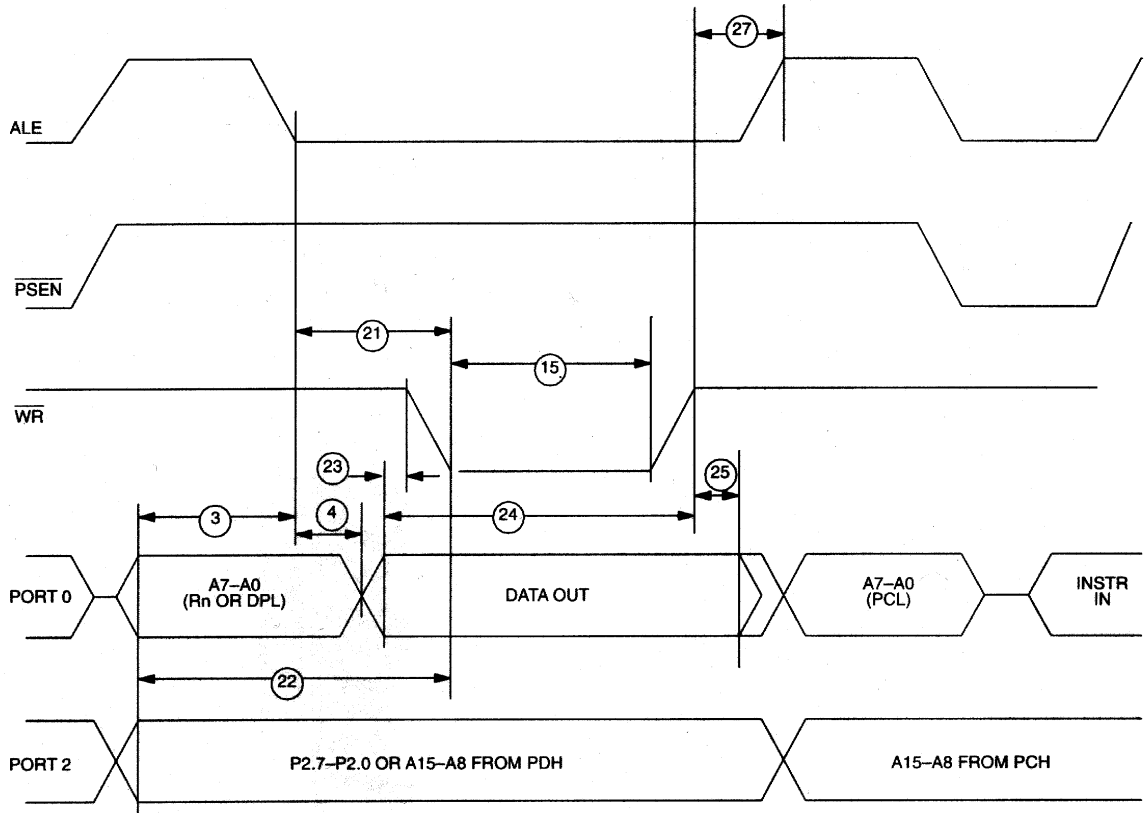
EXPANDED PROGRAM MEMORY READ CYCLE



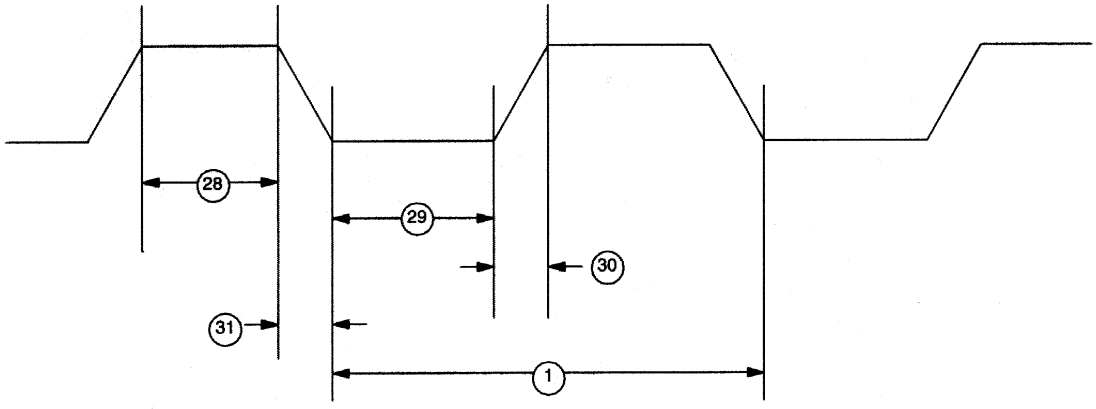
EXPANDED DATA MEMORY READ CYCLE



EXPANDED DATA MEMORY WRITE CYCLE



EXTERNAL CLOCK TIMING



AC CHARACTERISTICS (cont'd)

EXTERNAL CLOCK DRIVE

(t_A=0°C to70°C; V_{CC}=5V ± 5%)

#	PARAMETER		SYMBOL	MIN	MAX	UNITS
28	External Clock High Time	@ 12 MHz @ 16 MHz	t_{CLKHPW}	20 15		ns ns
29	External Clock Low Time	@ 12 MHz @ 16 MHz	t_{CLKLPW}	20 15		ns ns
30	External Clock Rise Time	@ 12 MHz @ 16 MHz	t_{CLKR}		20 15	ns ns
31	External Clock Fall Time	@ 12 MHz @ 16 MHz	t_{CLKF}		20 15	ns ns

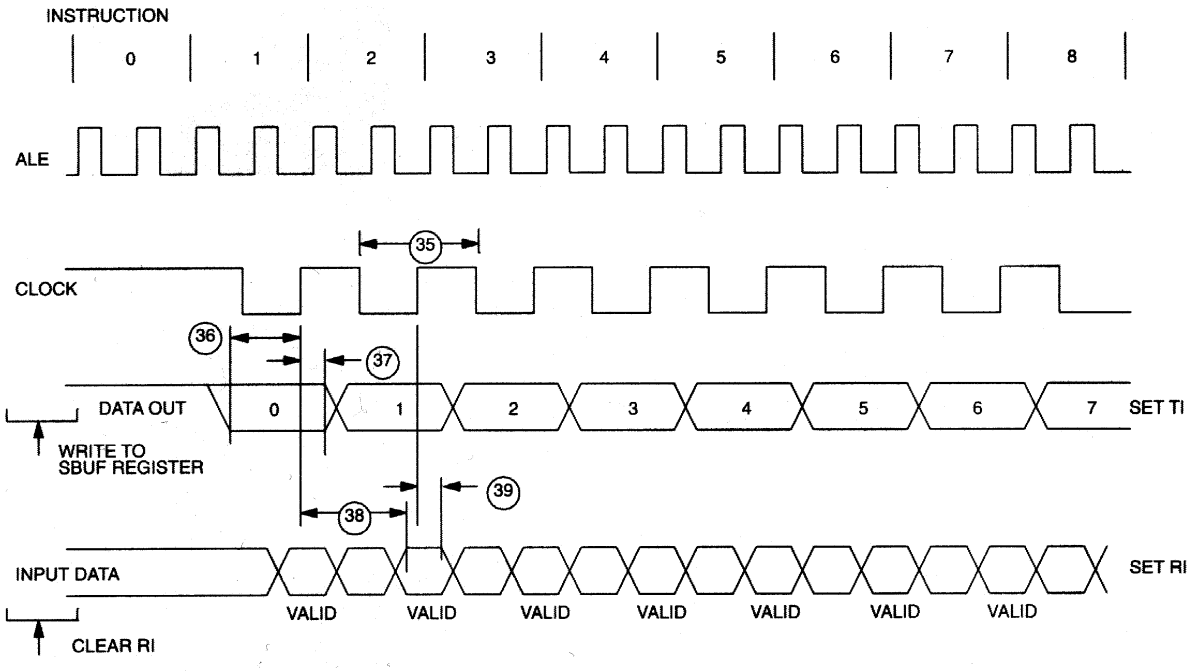
AC CHARACTERISTICS (cont'd)

SERIAL PORT TIMING - MODE 0

(t_A=0°C to70°C; V_{CC}=5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
35	Serial Port Cycle Time	t_{SPCLK}	$12t_{CLK}$		µs
36	Output Data Setup to Rising Clock Edge	t_{DOCH}	$10t_{CLK}$ -133		ns
37	Output Data Hold after Rising Clock Edge	t_{CHDO}	$2t_{CLK}$ -117		ns
38	Clock Rising Edge to Input Data Valid	t_{CHDV}		$10t_{CLK}$ -133	ns
39	Input Data Hold after Rising Clock Edge	t_{CHDIV}	0		ns

SERIAL PORT TIMING - MODE 0



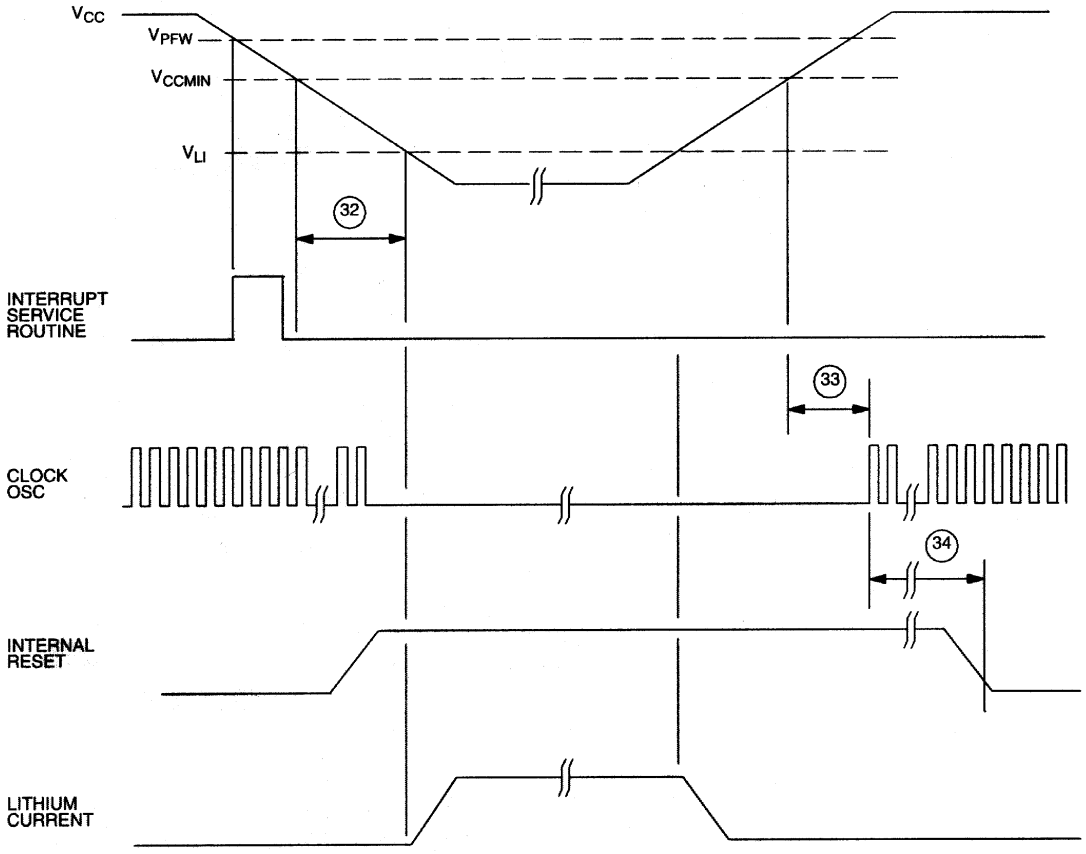
AC CHARACTERISTICS (cont'd)

POWER CYCLING TIMING

(t_A=0°C to70°C; V_{CC}=5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
32	Slew Rate from V_{CCmin} to V_{LImax}	t_F	40		µs
33	Crystal Startup Time	t_{CSU}		(note 5)	
34	Power-On Reset Delay	t_{POR}		21504	t_{CLK}

POWER CYCLE TIMING



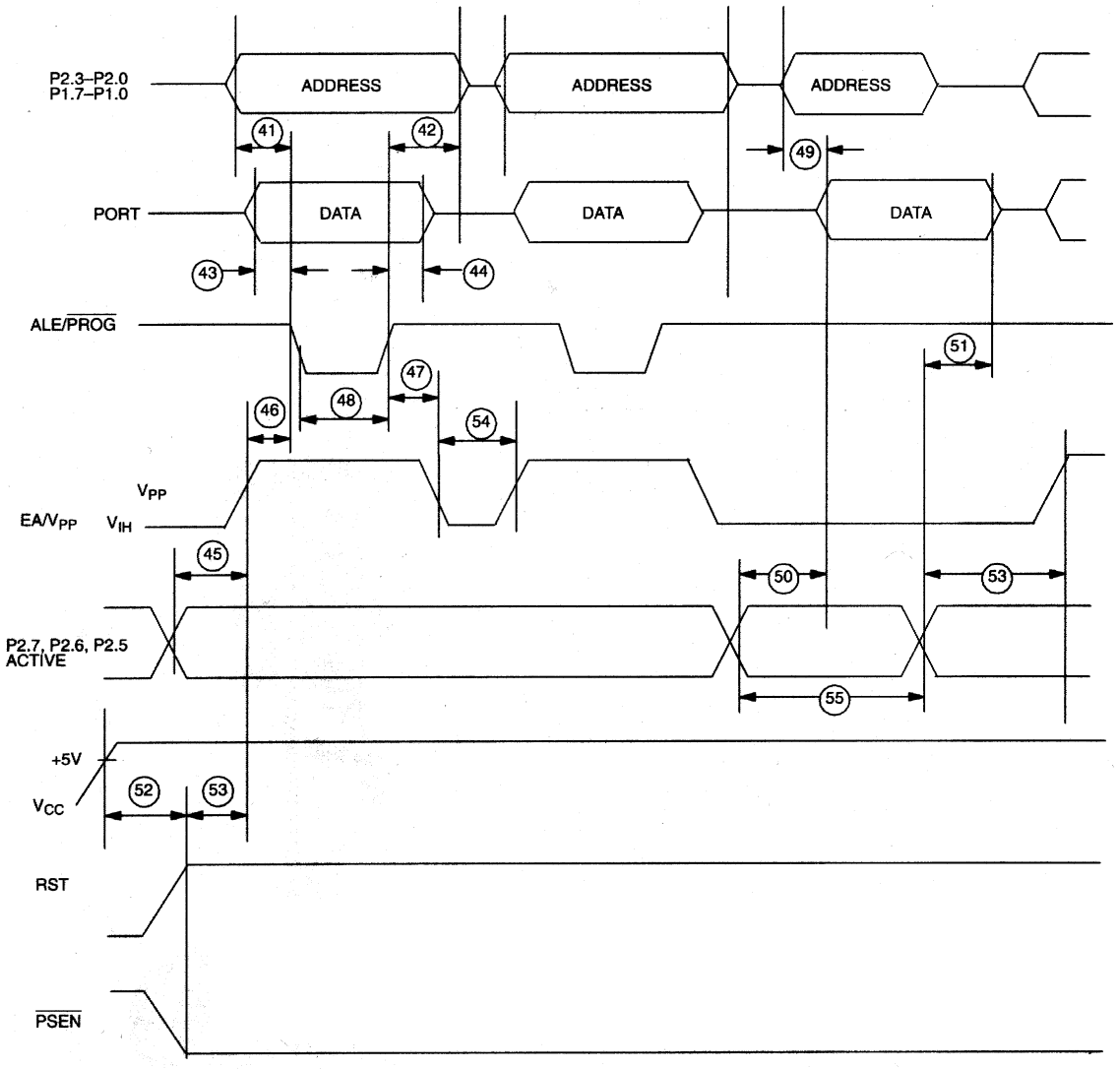
AC CHARACTERISTICS (cont'd)

PARALLEL PROGRAM LOAD TIMING (t_A=0°C to70°C; V_{CC}=5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
40	Oscillator Frequency	$1/t_{CLK}$	1.0	12.0	MHz
41	Address Setup to $\overline{PROG}$ Low	t_{AVPRL}	0		
42	Address Hold after $\overline{PROG}$ High	t_{PRHAV}	0		
43	Data Setup to $\overline{PROG}$ Low	t_{DVPRL}	0		
44	Data Hold after $\overline{PROG}$ High	t_{PRHDV}	0		
45	P2.7, 2.6, 2.5 Setup to V_{PP}	t_{P27HVP}	0		
46	V_{PP} Setup to $\overline{PROG}$ Low	t_{VPHPRL}	0		
47	V_{PP} Hold after $\overline{PROG}$ Low	t_{PRHVPL}	0		
48	$\overline{PROG}$ Width Low	t_{PRW}	2400		t_{CLK}
49	Data Output from Address Valid	t_{AVDV}		48 1800*	t_{CLK}
50	Data Output from P2.7 Low	t_{DVP27L}		48 1800*	t_{CLK}
51	Data Float after P2.7 High	t_{P27HDZ}	0	48 1800*	t_{CLK}
52	Delay to Reset/$\overline{PSEN}$ Active after Power On	t_{PORPV}	21504		t_{CLK}
53	Reset/$\overline{PSEN}$ Active (or Verify Inactive) to V_{PP} High	t_{RAVPH}	1200		t_{CLK}
54	V_{PP} Inactive (Between Program Cycles)	t_{VPPPC}	1200		t_{CLK}
55	Verify Active Time	t_{VFT}	48 2400*		t_{CLK}

* Second set of numbers refers to expanded memory programming up to 32k bytes.

PARALLEL PROGRAM LOAD TIMING



CAPACITANCE

(test frequency=1MHz; t_A=25°C)

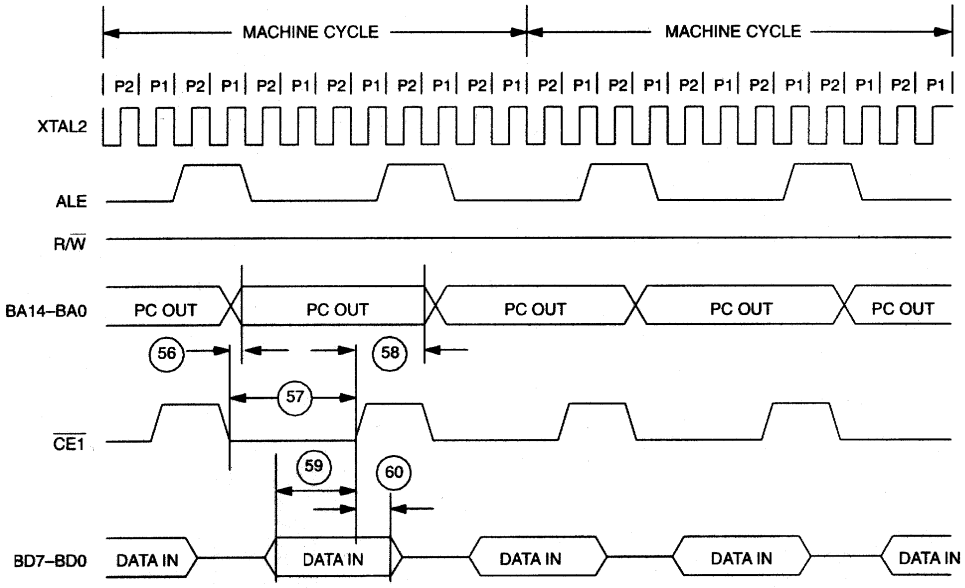
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Capacitance	C_O			10	pF	
Input Capacitance	C_I			10	pF	

BYTE-WIDE ADDRESS/DATA BUS TIMING

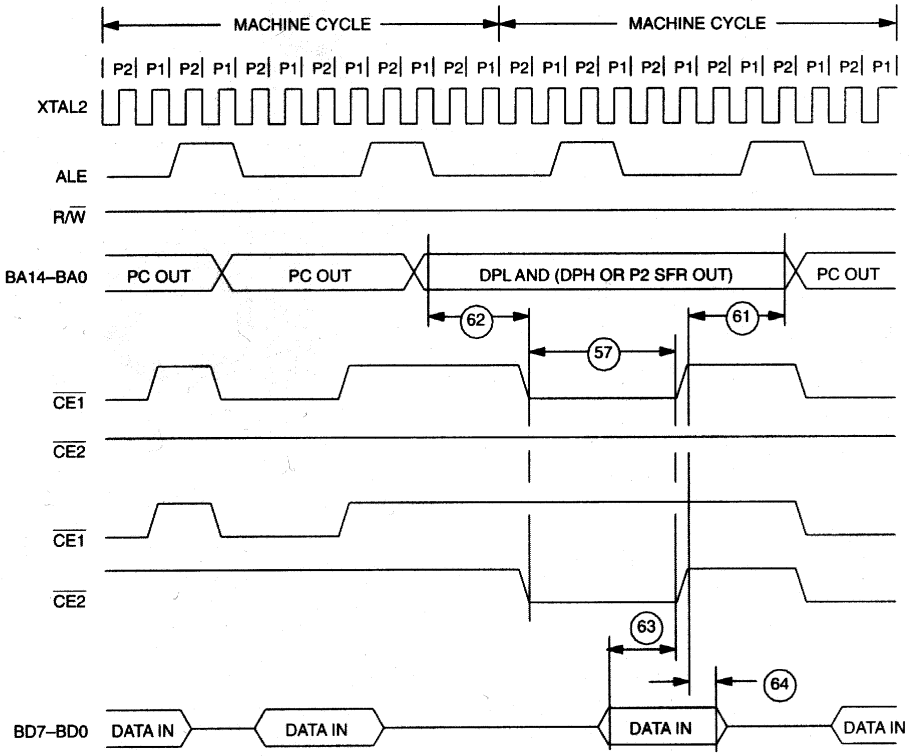
AC CHARACTERISTICS (t_A=0°C to70°C; V_{CC}=5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
56	Delay to Embedded Address Valid from $\overline{CE1}$ Low During Opcode Fetch	t_{CE1LPA}		20	ns
57	$\overline{CE1}$ or $\overline{CE2}$ Pulse Width	t_{CEPW}	$4t_{CLK}$-15		ns
58	Embedded Address Hold after $\overline{CE1}$ High During Opcode Fetch	t_{CE1HPA}	$2t_{CLK}$-20		ns
59	Embedded Data Setup to $\overline{CE1}$ High During Opcode Fetch	t_{OVCE1H}	$1t_{CLK}$+40		ns
60	Embedded Data Hold after $\overline{CE1}$ High During Opcode Fetch	t_{CE1HOV}	10		ns
61	Embedded Address Hold after $\overline{CE1}$ or $\overline{CE2}$ High During MOVX	t_{CEHDA}	$4t_{CLK}$-30		ns
62	Delay from Embedded Address Valid to $\overline{CE1}$ or $\overline{CE2}$ Low During MOVX	t_{CELDA}	$4t_{CLK}$-25		ns
63	Embedded Data Hold Setup to $\overline{CE1}$ or $\overline{CE2}$ High During MOVX (read)	t_{DACEH}	$1t_{CLK}$+40		ns
64	Embedded Data Hold after $\overline{CE1}$ or $\overline{CE2}$ High During MOVX (read)	t_{CEHDV}	10		ns
65	Embedded Address Valid to R/$\overline{W}$ Active During MOVX (write)	t_{AVRWL}	$3t_{CLK}$-35		ns
66	Delay from R/$\overline{W}$ Low to Valid Data Out During MOVX (write)	t_{RWLDV}	20		ns
67	Valid Data Out Hold Time from $\overline{CE1}$ or $\overline{CE2}$ High	t_{CEHDV}	$1t_{CLK}$-15		ns
68	Valid Data Out Hold Time from R/$\overline{W}$ High	t_{RWHDV}	0		ns
69	Write Pulse Width (R/$\overline{W}$ low time)	t_{RWLPW}	$6t_{CLK}$-20		ns

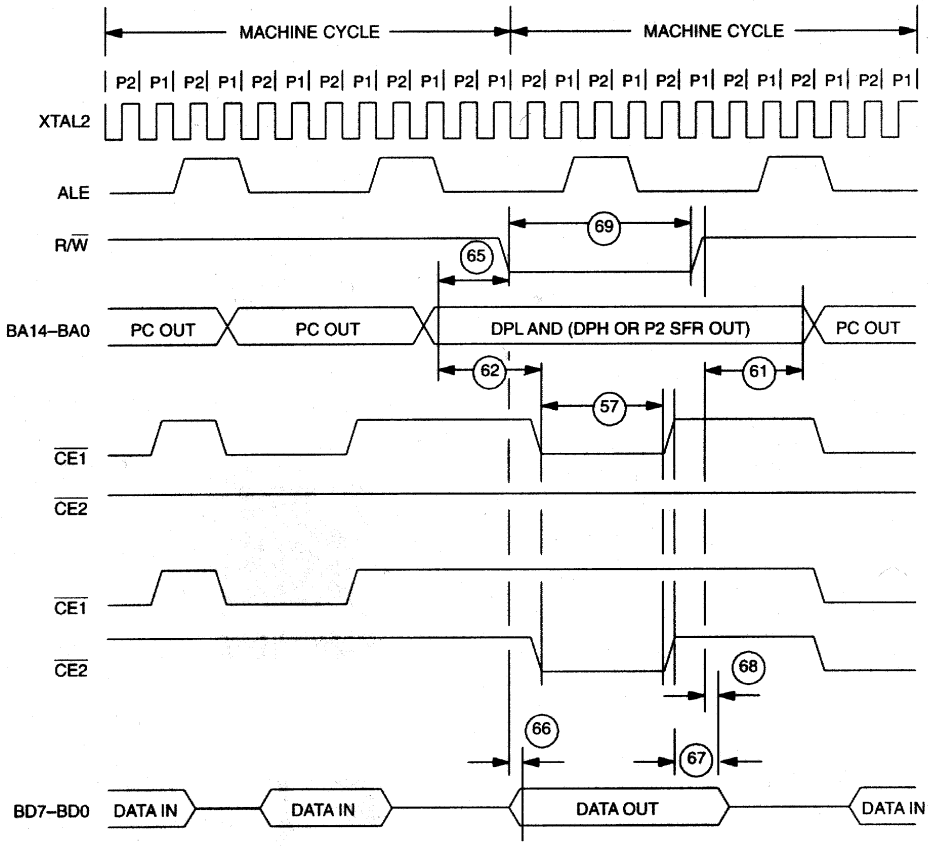
BYTE-WIDE ADDRESS/DATA BUS OPCODE FETCH CYCLE



BYTE-WIDE ADDRESS/DATA BUS OPCODE FETCH WITH DATA MEMORY READ



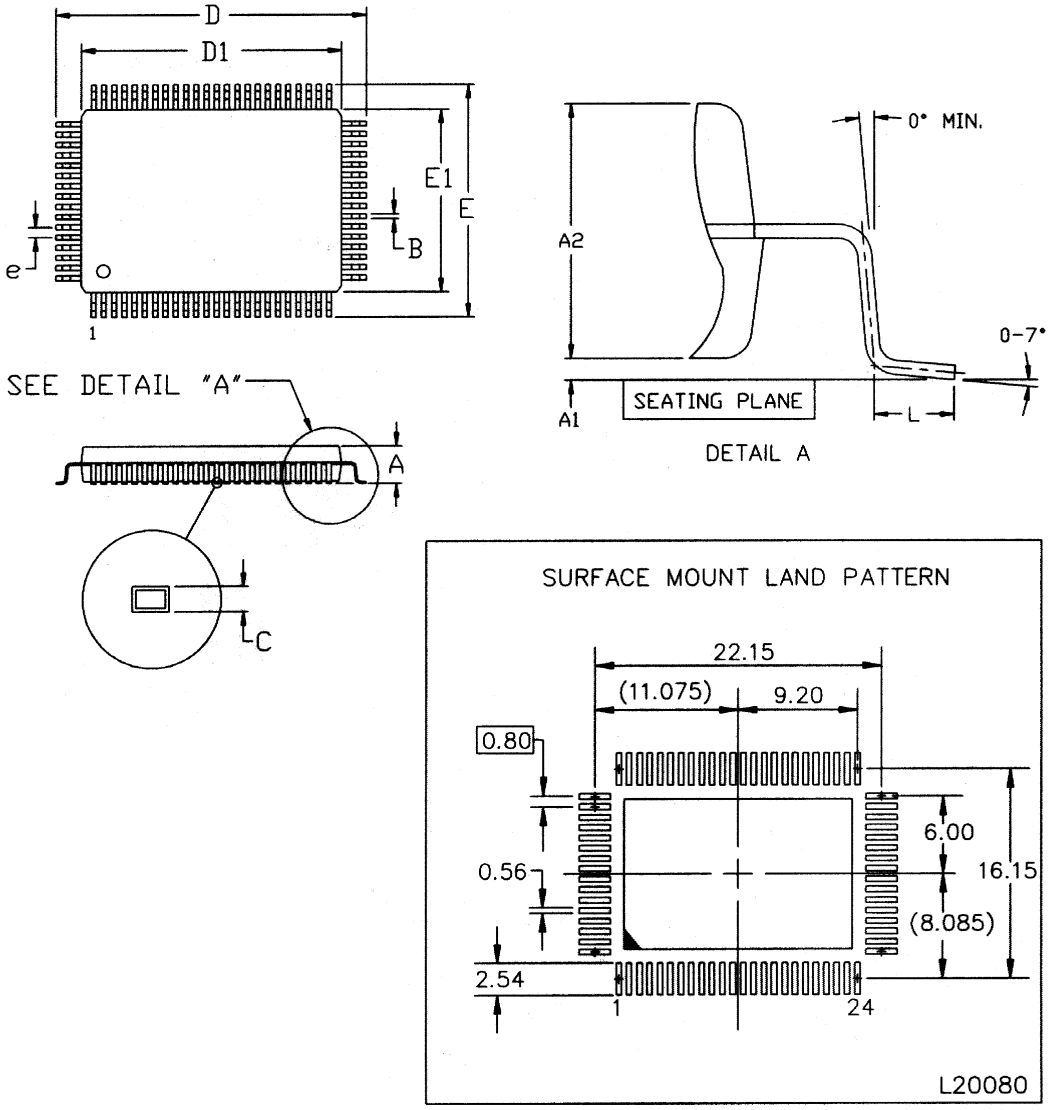
BYTE-WIDE ADDRESS/DATA BUS OPCODE FETCH WITH DATA MEMORY WRITE



NOTES:

1. All voltages are referenced to ground.
2. Maximum operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF}=10 ns, V_{IL}= 0.5V; XTAL2 disconnected; $\overline{EA}$ = RST = PORT0 = V_{CC}.
3. Idle mode I_{CC} is measured with all output pins disconnected; XTAL1 driven at 12 MHz with t_{CLKR}, t_{CLKF}=10 ns, V_{IL}= 0.5V; XTAL2 disconnected; $\overline{EA}$ = PORT0 = V_{CC}, RST = V_{SS}.
4. Stop mode I_{CC} is measured with all output pins disconnected; $\overline{EA}$ = PORT0 = V_{CC}; XTAL2 not connected; RST = V_{SS}.
5. Crystal start-up time is the time required to get the mass of the crystal into vibrational motion from the time that power is first applied to the circuit until the first clock pulse is produced by the on-chip oscillator. The user should check with the crystal vendor for the worst-case spec on this time.
6. Assumes V_{LI}=3.3V maximum.
7. I_{LI} is the current drawn from V_{LI} when V_{CC}=0V and V_{CCO} is disconnected.
8. I_{CCO}=10 µA.

DS5000FP CMOS MICROPROCESSOR



DIM	MILLIMETERS	
	MIN	MAX
A	-	3.15
A1	0.25	-
A2	2.55	2.87
B	0.30	0.50
C	0.13	0.23
D	23.70	24.10
D1	19.90	20.10
E	17.40	18.10
E1	13.90	14.10
e	0.80 BSC	
L	0.65	0.95

56-G4005-001

DATA SHEET REVISION SUMMARY

The following represent the key differences between 07/27/95 and 07/24/96/96 version of the DS5000FP data sheet. Please review this summary carefully.

1. Add V_{CCO2} Minimum Specification (PCN F62501).
2. Add embedded bus DC specifications.
3. Update mechanical specifications.