DALLAS SEMICONDUCTOR

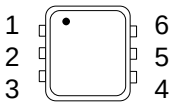
DS2417
1-Wire™ Time Chip With Interrupt

FEATURES

- Real-Time Clock with fully compatible 1-Wire MicroLAN interface
- Uses the same binary time/date representation as the DS2404 but with 1 second resolution
- Clock accuracy ± 2 minutes per month at 25°C
- Programmable interrupt output for system wakeup
- Communicates at 16.3k bits per second
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures absolute traceability because no two parts are alike
- 8-bit family code specifies device communication requirements to bus master
- Built-in multidrop controller ensures compatibility with other MicroLAN products
- Operates over a wide V_{DD} voltage range of 2.5V to 5.5V from -40°C to +85°C
- Low power, 200 nA typically with oscillator running
- Compact, low cost 6-pin TSOC surface mount package

PIN ASSIGNMENT

6-PIN TSOC PACKAGE



TOP VIEW

SIDE VIEW

See Mech. Drawings Section

PIN DESCRIPTION

Pin 1	GND
Pin 2	1-Wire
Pin 3	$\overline{INT}$
Pin 4	V_{DD}
Pin 5	X1
Pin 6	X2

ORDERING INFORMATION

DS2417P	6-pin TSOC package
DS2417V	Tape & Reel of DS2417P
DS2417X	Chip Scale Pkg., Tape & Reel

DESCRIPTION

The DS2417 1-Wire Time Chip with Interrupt offers a simple solution for storing and retrieving vital time information with minimal hardware. The DS2417 contains a unique lasered ROM and a real-time clock/calendar implemented as a binary counter. Only one pin is required for communication with the device. Utilizing a backup energy source, the data is nonvolatile and allows for stand-alone operation. The DS2417 features can be used to add functions such as calendar, time and date stamp, and logbook to any type of electronic device or embedded application that uses a microcontroller.

OVERVIEW

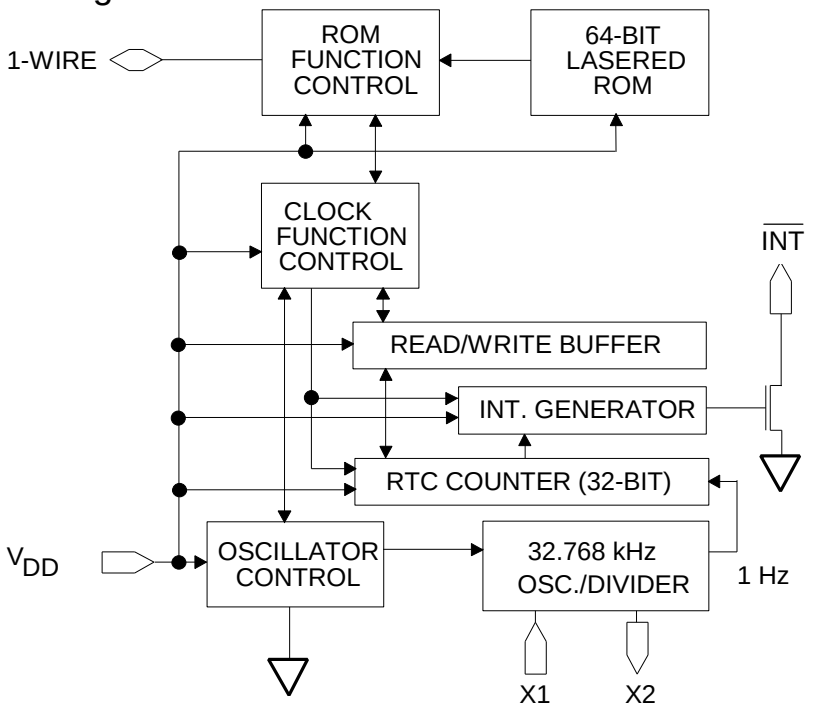
The DS2417 has two main data components: 1) 64-bit lasered ROM, and 2) real-time clock counter (Figure 1). The real-time clock utilizes an on-chip oscillator that is connected to an external 32.768 kHz crystal. The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of four ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM. The protocol for these ROM functions is described in Figure 7. After a ROM function command

is successfully executed, the real-time clock functions become accessible and the master may then provide one of the real-time clock function commands. The protocol for these commands is described in Figure 5. All data is read and written least significant bit first.

DETAILED PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	GND	**Ground Pin**
2	1-Wire	**Data input/output** Open drain.
3	$\overline{INT}$	**Interrupt pin** Open drain.
4	V_{DD}	**Power input pin**. 2.5V to 5.5V.
5, 6	X1, X2	**Crystal pins.** Connections for a standard 32.768 kHz quartz crystal, EPSON part number C-002RX or C-004R (be sure to request 6 pF load capacitance). **NOTE:** X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard-ringed with ground and that high frequency signals be kept away from the crystal area. See Figure 10 and Application Note 58 for details.

BLOCK DIAGRAM Figure 1

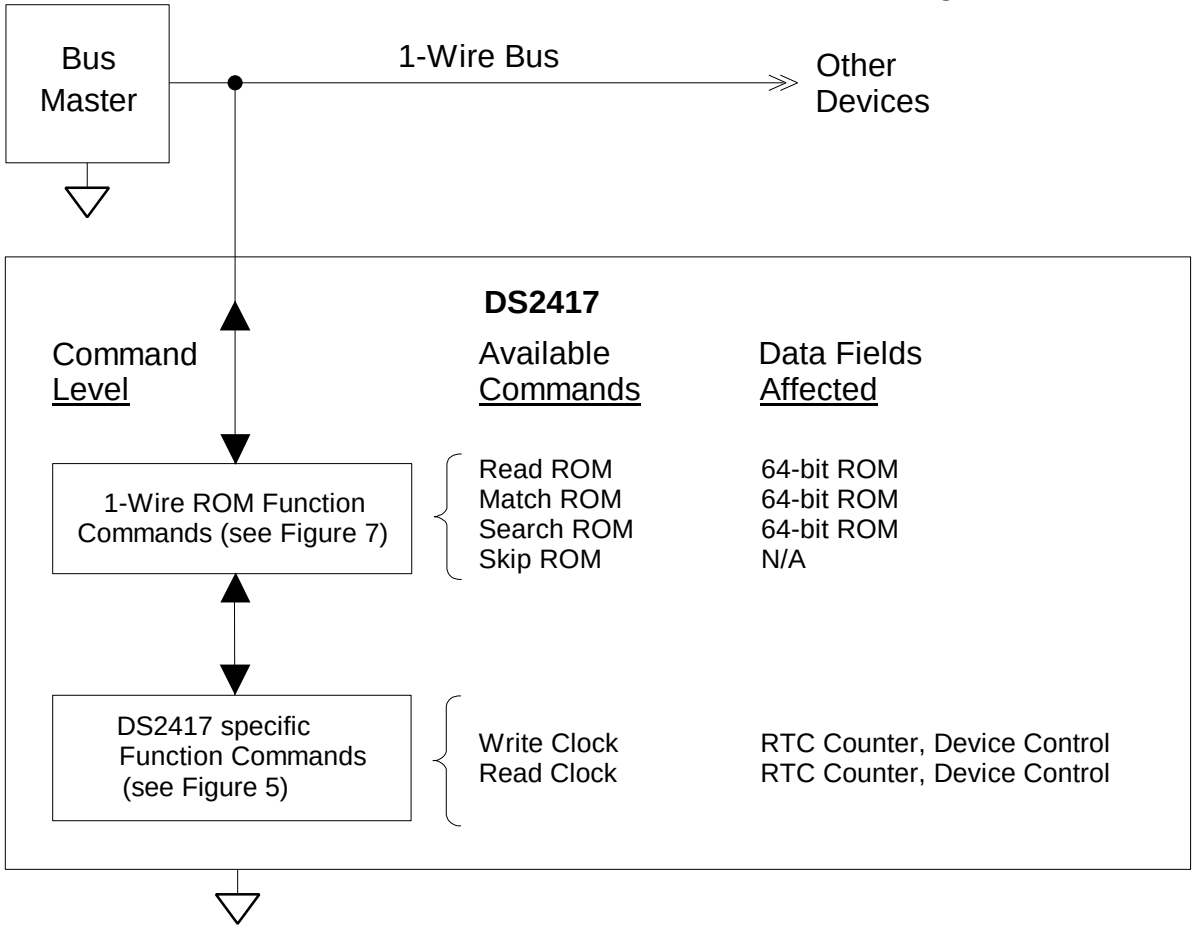


64-BIT LASERED ROM

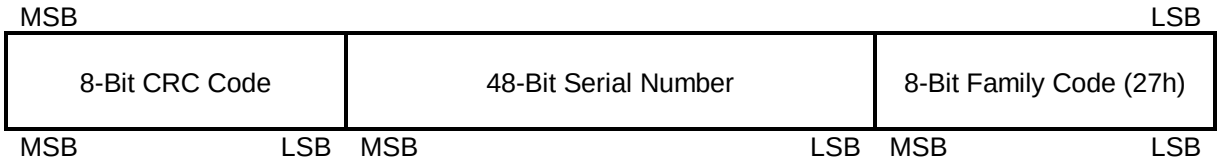
Each DS2417 contains a unique ROM code that is 64 bits long. The first eight bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 3.) The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas Semiconductor 1-Wire Cyclic Redundancy Check is available in the Book of DS19xx iButton Standards. The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros. The

64-bit ROM and ROM Function Control section allow the DS2417 to operate as a 1-Wire device and follow the 1-Wire protocol detailed in the section "1-Wire Bus System".

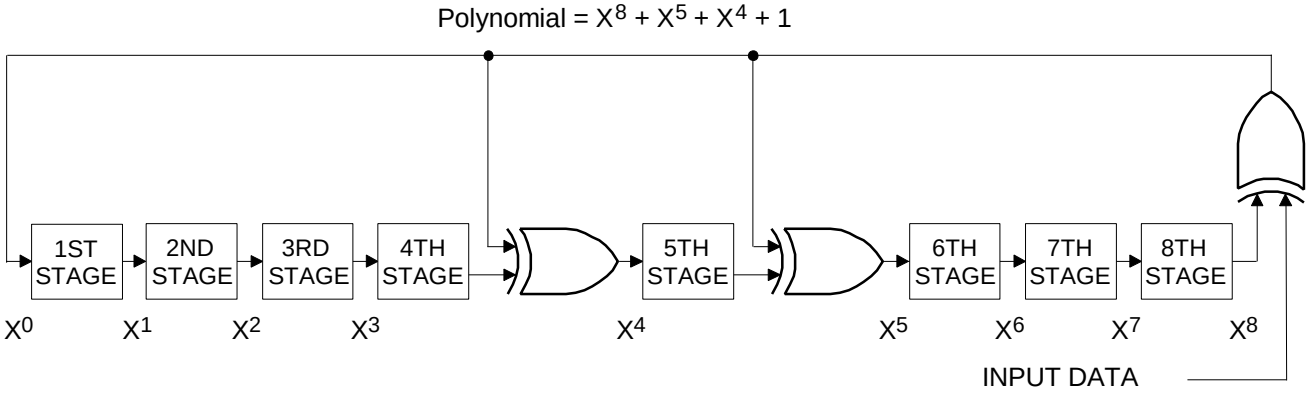
HIERARCHICAL STRUCTURE FOR 1-WIRE PROTOCOL Figure 2



64-BIT LASERED ROM Figure 3



1-WIRE CRC GENERATOR Figure 4



TIMEKEEPING

A 32.768 kHz crystal oscillator is used as the time base for the real-time clock counter. The oscillator can be turned on or off under software control. The oscillator must be on for the real time clock to function. The real-time clock counter is double buffered. This allows the master to read time without the data changing while it is being read. To accomplish this, a snapshot of the counter data is transferred to a read/write buffer, which the user accesses.

DEVICE CONTROL BYTE

The DS2417 can generate interrupt pulses to trigger activities that have to occur at regular intervals. The selection of this interval and the on/off control of the 32.768 kHz crystal oscillator are done through the device control byte. This byte can be read and written through the Clock Function commands.

Device Control Byte

7	6	5	4	3	2	1	0
IE	IS2	IS1	IS0	**OSC**	OSC	0	0

Bit 0 - 1 | 0 | No function

Bits 0 and 1 are hard-wired to read all 0's.

Bit 2 - 3 | OSC | Oscillator Enable/Disable

These bits control/report whether the 32.768 kHz crystal oscillator is running. If the oscillator is running, both OSC bits will read 1. If the oscillator is turned off these bits will all read 0. When writing the device control byte both occurrences of the OSC bit should have identical data. Otherwise the value in bit address 3 (bold) takes precedence.

Bit 4 - 6 | IS | Interval Select

These bits determine the time between interrupt pulses. The values available are shown below.

IS2	IS1	IS0	Interrupt Interval
0	0	0	1s
0	0	1	4s
0	1	0	32s = 0.53 min
0	1	1	64s = 1.07 min
1	0	0	2048s = 34.13 min
1	0	1	4096s = 68.27 min
1	1	0	65536s = 18.20 hours
1	1	1	131072s = 36.41 hours

Bit 7 | IE | Interrupt Enable

This bit controls whether the interrupt pulse will be generated at the selected interval. To enable interrupts this bit needs to be 1.

REAL-TIME CLOCK

The real-time clock is a 32-bit binary counter. It is incremented once per second. The real-time clock can accumulate 136 years of seconds before rolling over. Time/date is represented by the number of seconds since a reference point, which is determined by the user. For example, 12:00 a.m., January 1, 1970 could be a reference point.

CLOCK FUNCTION COMMANDS

The "Clock Function Flow Chart" (Figure 5) describes the protocols necessary for accessing the real-time clock. With only four bytes of real-time clock and one control byte the DS2417 does not provide random access. Reading and writing always starts with the device control byte followed by the least significant byte of the time data.

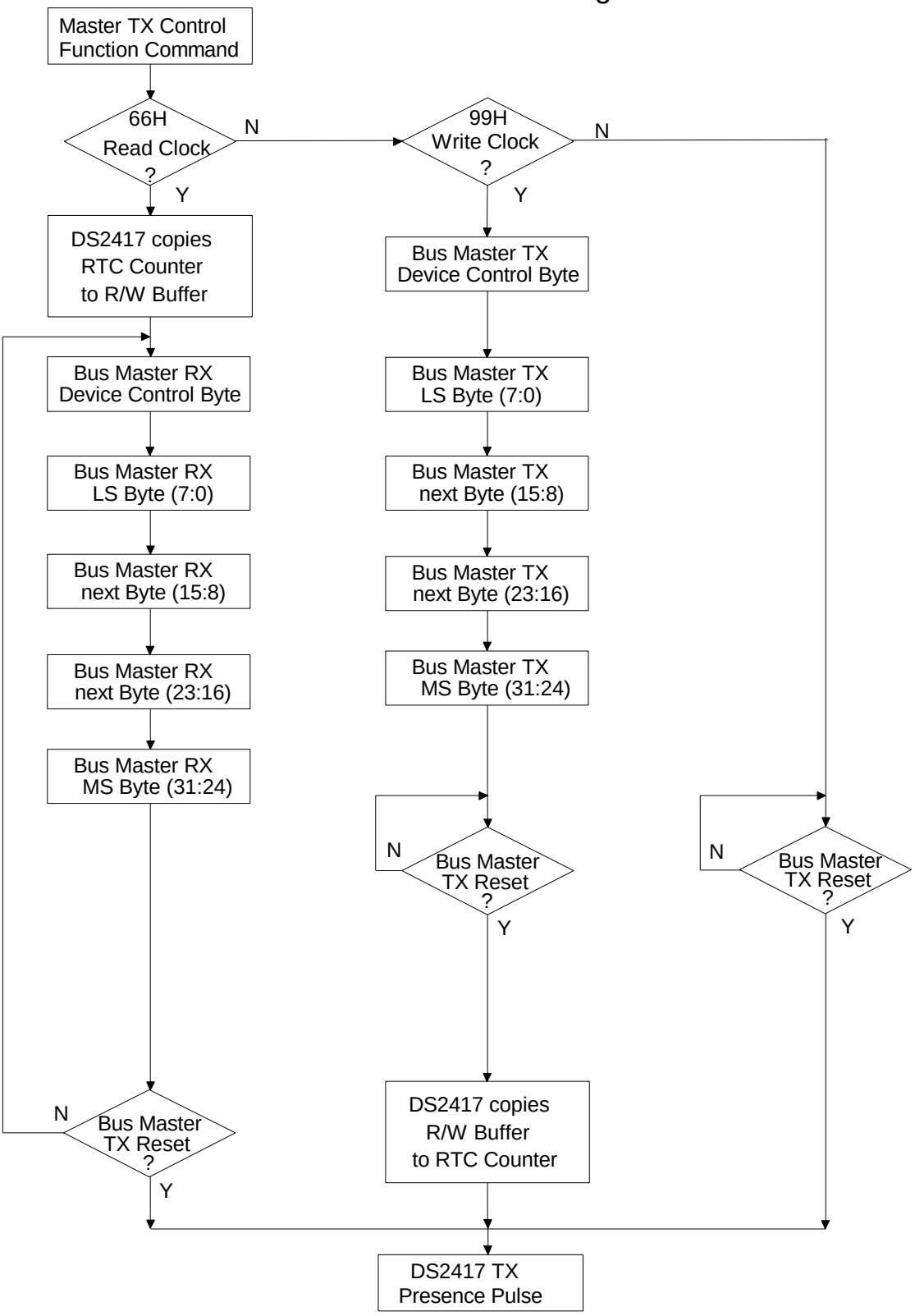
READ CLOCK [66h]

The read clock command is used to read the device control byte and the contents of the real-time clock counter. After having received the most significant bit of the command code the device copies the actual contents of the real-time clock counter to the read/write buffer. Now the bus master reads data beginning with the device control byte followed by the least significant byte through the most significant byte of the real-time clock. After this the bus master may continue reading from the DS2417. The data received will be the same as in the first pass through the command flow. The read clock command can be ended at any point by issuing a Reset Pulse.

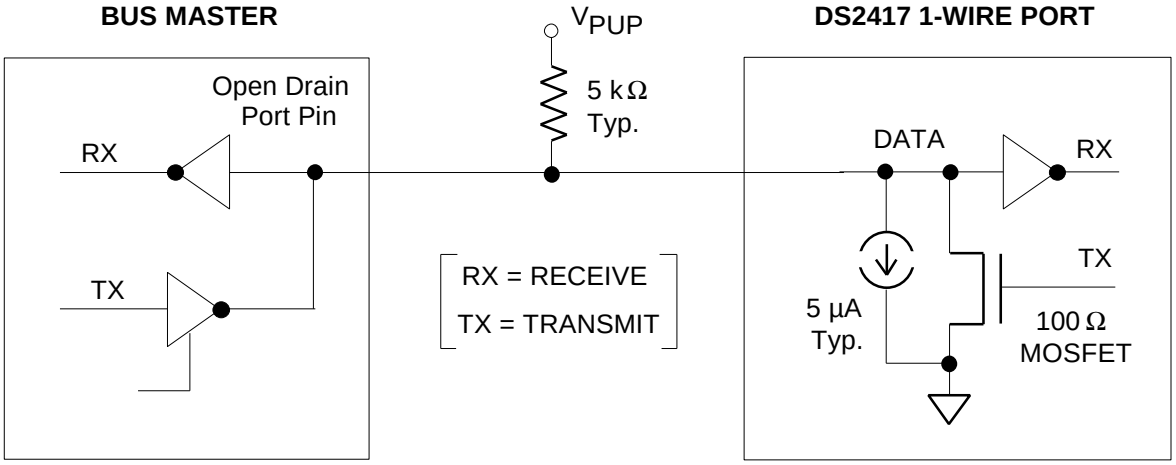
WRITE CLOCK [99h]

The write clock command is used to set the real-time clock counter and to write the device control byte. After issuing the command, the bus master writes first the device control byte, which becomes immediately effective. After this the bus master sends the least significant byte through the most significant byte to be written to the real-time clock counter. The new time data is copied from the read/write buffer to the real-time clock counter and becomes effective as the bus master generates a reset pulse. If enabled, an interrupt pulse will be generated either immediately or delayed, depending on the actual time and the selected interval duration (see Figure 11). If the oscillator is intentionally stopped the real-time clock counter behaves as a four-byte non-volatile memory.

CLOCK FUNCTION COMMAND FLOW CHART Figure 5



HARDWARE CONFIGURATION Figure 6



1-WIRE BUS SYSTEM

The 1-Wire bus is a system, which has a single bus master and one or more slaves. In all instances the DS2417 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). A 1-Wire protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx iButton Standards.

HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain or 3-state outputs. The 1-Wire input of the DS2417 is open drain with an internal circuit equivalent to that shown in Figure 6. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The 1-Wire bus has a maximum data rate of 16.3k bits per second and requires a pullup resistor of approximately 5kΩ.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120 µs, one or more of the devices on the bus may be reset. Since the DS2417 gets all its energy for operation through its V_{DD} pin it will NOT perform a power-on reset if the 1-Wire bus is low for an extended time period.

TRANSACTION SEQUENCE

The protocol for accessing the DS2417 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Clock Function Command

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS2417 is on the bus and is ready to operate. For more details, see the "1-Wire Signaling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands that the DS2417 supports. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 7):

Read ROM [33h]

This command allows the bus master to read the DS2417's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command should only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The resultant family code and 48-bit serial number read by the master will be invalid.

Match ROM [55h]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS2417 on a multidrop bus. Only the DS2417 that exactly matches the 64-bit ROM sequence will respond to the following clock function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

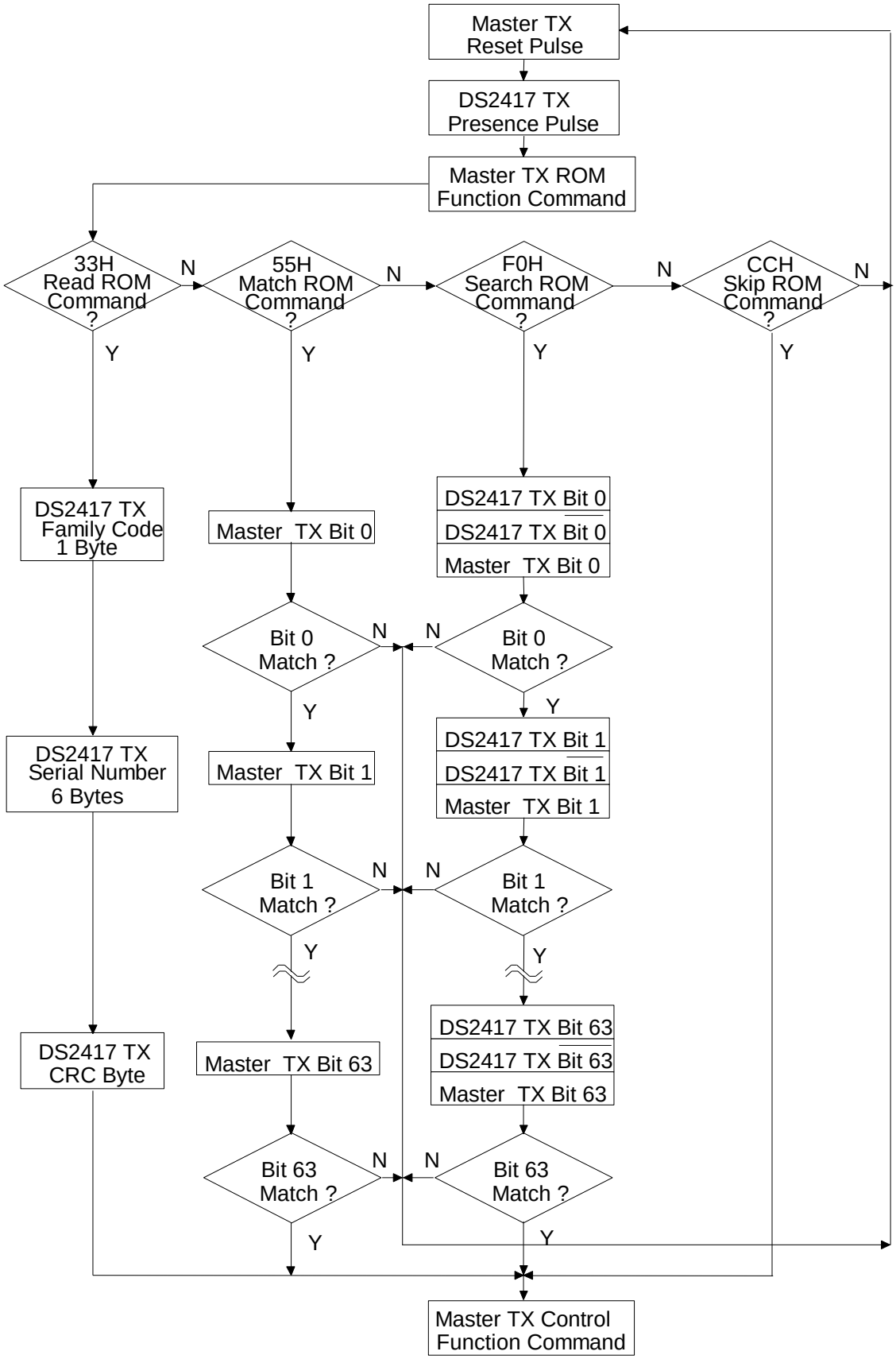
SEARCH ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The search ROM process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the 64-bit ROM code of one device. Additional passes will identify the ROM codes of the remaining devices. See Chapter 5 of the Book of DS19xx iButton Standards for a comprehensive discussion of a search ROM, including an actual example.

Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the clock functions without providing the 64-bit ROM code. If more than one slave is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired-AND result).

ROM FUNCTIONS FLOW CHART Figure 7



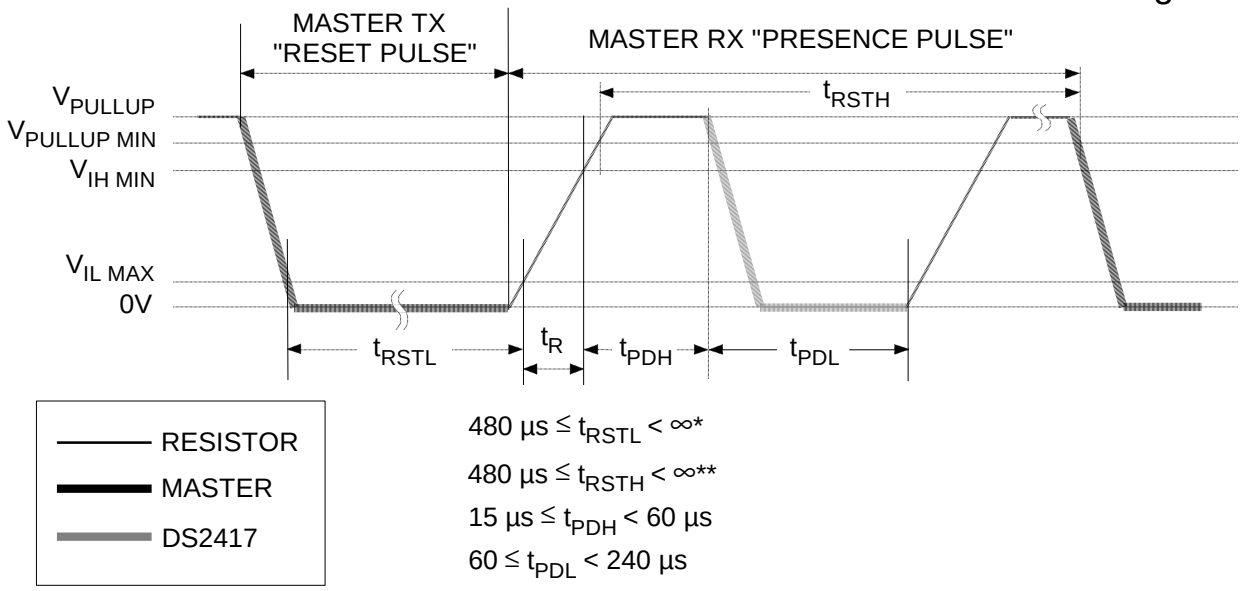
(SEE FIGURE 5)

1–WIRE SIGNALING

The DS2417 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1 and Read Data. Except for the presence pulse the bus master initiates all these signals.

The initialization sequence required to begin any communication with the DS2417 is shown in Figure 8. A reset pulse followed by a presence pulse indicates the DS2417 is ready to send or receive data. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480 µs). The bus master then releases the line and goes into receive mode (RX). The 1-Wire bus is pulled to a high state via the pullup resistor. After detecting the rising edge on the data line, the DS2417 waits (t_{PDH}, 15-60 µs) and then transmits the presence pulse (t_{PDL}, 60-240 µs).

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 8



* In order not to mask interrupt signaling by other devices on the 1-Wire bus t_{RSTL} + t_R should always be less than 960 µs.

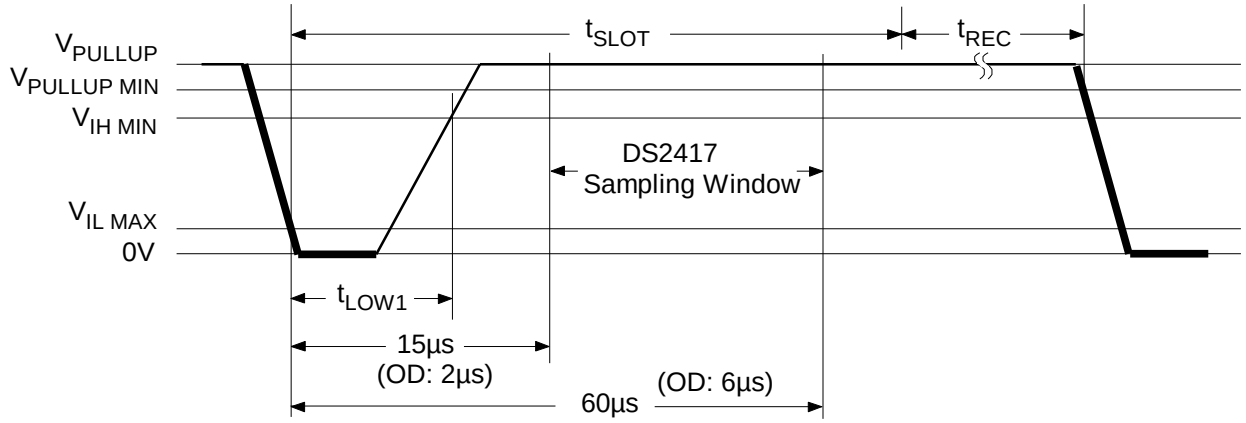
** Includes recovery time

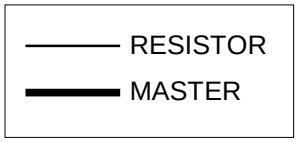
READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 9. The master initiates all time slots by driving the data line low. The falling edge of the data line synchronizes the DS2417 to the master by triggering an internal delay circuit. During write time slots, the delay circuit determines when the DS2417 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS2417 will hold the data line low. If the data bit is a "1", the DS2417 will not hold the data line low at all.

READ/WRITE TIMING DIAGRAM Figure 9

Write-one Time Slot



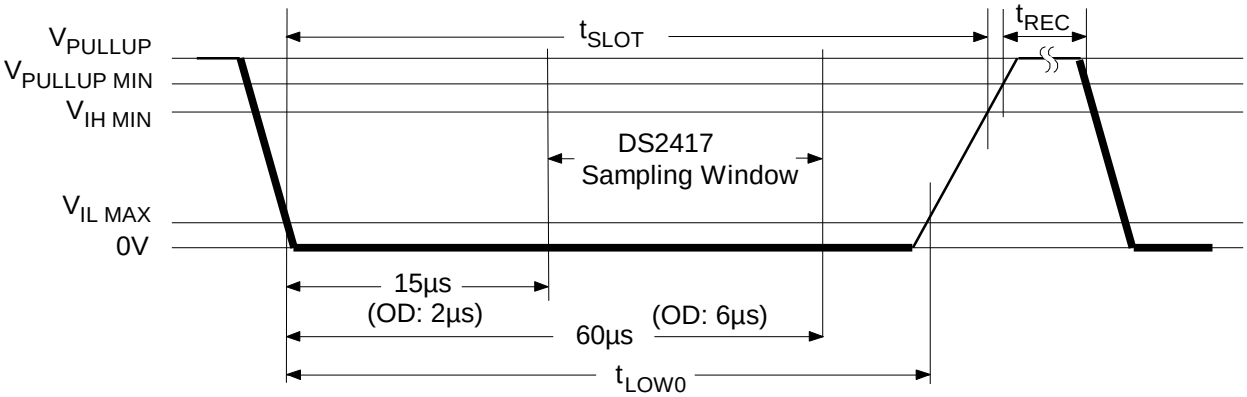


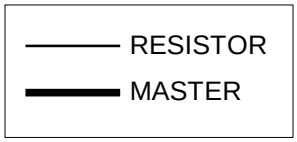
$60\ \mu s \le t_{SLOT} < 120\ \mu s$

$1\ \mu s \le t_{LOW1} < 15\ \mu s$

$1\ \mu s \le t_{REC} < \infty$

Write-zero Time Slot



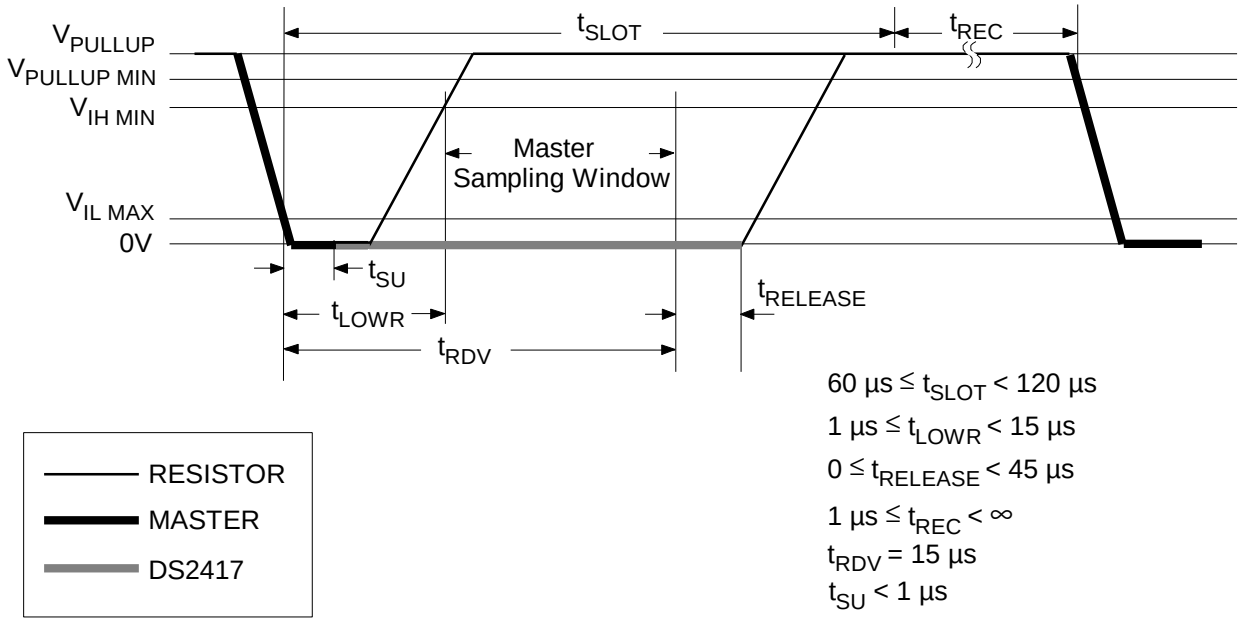


$60\ \mu s \le t_{LOW0} < t_{SLOT} < 120\ \mu s$

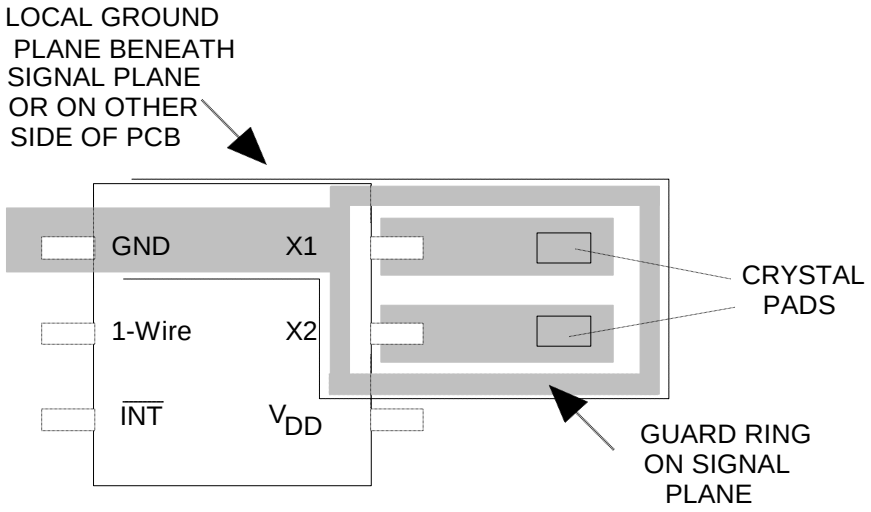
$1\ \mu s \le t_{REC} < \infty$

READ/WRITE TIMING DIAGRAM (continued) Figure 9

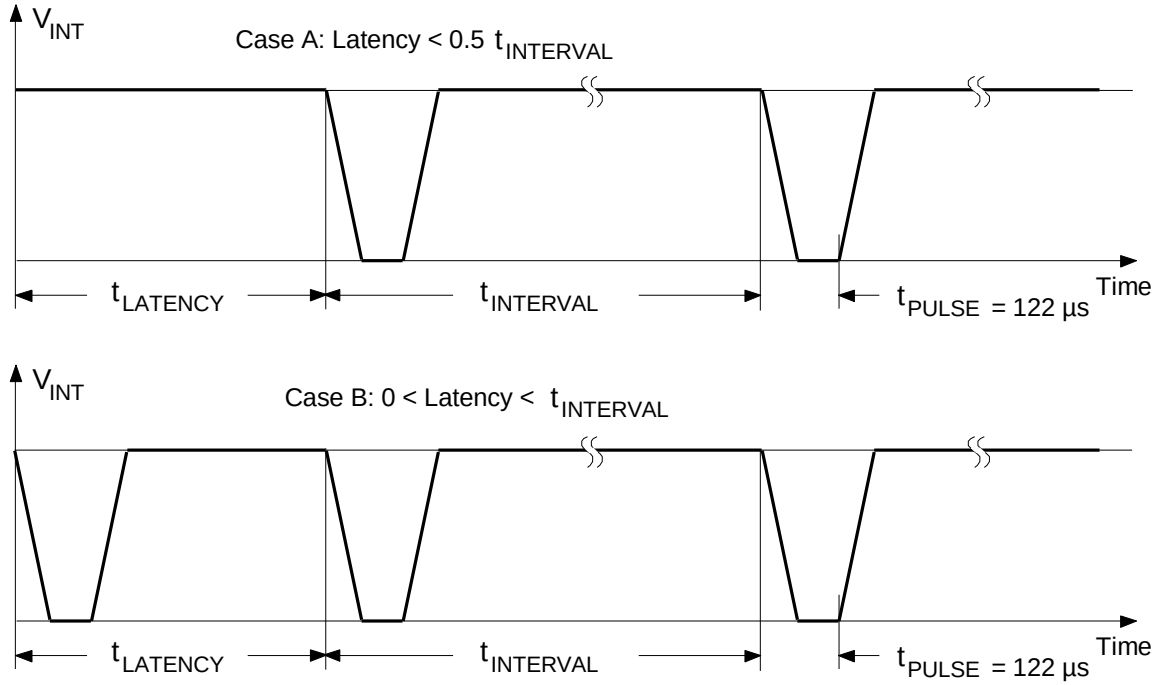
Read-data Time Slot



CRYSTAL PLACEMENT ON PCB Figure 10



INTERRUPT TIMING Figure 11



The latency depends on the selected interrupt interval (IS0 to IS2 settings) and the contents of the RTC counter at the time of writing the device control byte. In Case A, the flip-flop that determines the interval duration is reset and toggles before half of the interval time is over. In Case B, this flip-flop is set which generates an immediate interrupt pulse; the latency, therefore, can be up to one full interval duration.

If enabled, the interrupt pulse may also be triggered while reading from or writing to the control byte.

ABSOLUTE MAXIMUM RATINGS*

Voltage on 1-Wire to Ground	-0.5V to +7.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{PUP}=2.5V to 6.0V; V_{DD} = 2.5V to 5.5V, -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH1}	2.2		6.0	V	1,11
Logic 0	V_{IL1}	-0.3		TBD	V	1,6
Output Logic Low @ 4 mA	V_{OL1}			0.4	V	1
Output Logic High	V_{OH1}			V_{PUP}	V	1,3
Input Load Current	I_{L1}		5		µA	4
Interrupt Sink Current @ 0.4V	I_{INT3}	5			mA	9
Operating Current (Osc. On)	I_{DD3}			250	nA	2, 9
Quiescent Current (Osc. Off)	I_{DDQ3}			50	nA	2, 8, 9
Interrupt Sink Current @ 0.4V	I_{INT5}	10			mA	10
Operating Current (Osc. On)	I_{DD5}			450	nA	2, 10
Quiescent Current (Osc. Off)	I_{DDQ5}			100	nA	2, 8, 10

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance 1-Wire	C_{IN}			50	pF	

AC ELECTRICAL CHARACTERISTICS

(V_{PUP}=2.5V to 6.0V; V_{DD} = 2.5V to 5.5V, -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Low Time	t_{LOWR}	1		15	µs	
Read Data Valid	t_{RDV}	exactly 15			µs	12
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset High Time	t_{RSTH}	480			µs	
Reset Low Time	t_{RSTL}	480		960	µs	7
Presence Detect High	t_{PDH}	15		60	µs	
Presence Detect Low	t_{PDL}	60		240	µs	

NOTES:

1. All voltages are referenced to ground.

2. Measured with outputs open.

3. V_{PUP} = external pullup voltage.

4. Input load is to ground.

5. Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge.

6. Under certain low voltage conditions V_{IL1MAX} may have to be reduced to as much as 0.5V to always guarantee a presence pulse.

7. The reset low time (t_{RSTL}) should be restricted to a maximum of 960 µs, to allow interrupt signaling, otherwise, it could mask or conceal interrupt pulses.

8. When V_{DD} ramps up, the oscillator is always off.

9. At V_{DD} = 3V ± 10%

10. At V_{DD} = 5V ± 10%

11. V_{IH1} has to be V_{DD} – 0.3V or higher.

12. The master must read while the data is valid.