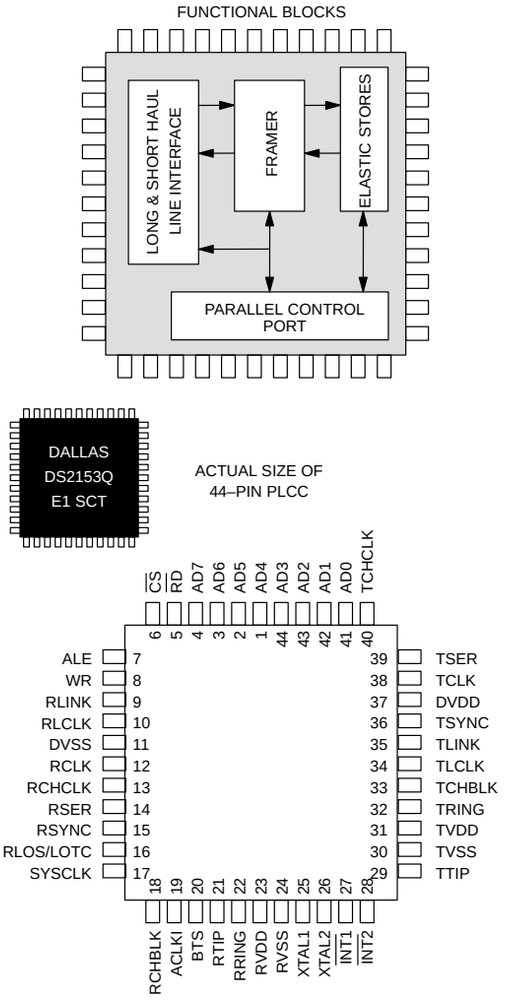
DALLAS SEMICONDUCTOR

DS2153Q
E1 Single–Chip Transceiver

FEATURES

- Complete E1(CEPT) PCM–30/ISDN–PRI transceiver functionality
- Onboard line interface for clock/data recovery and waveshaping
- 32–bit or 128–bit jitter attenuator
- Generates line build–outs for both 120 ohm and 75 ohm lines
- Frames to FAS, CAS, and CRC4 formats
- Dual onboard two–frame elastic store slip buffers that can connect to backplanes up to 8.192 MHz
- 8–bit parallel control port that can be used on either multiplexed or non–multiplexed buses
- Extracts and inserts CAS signaling
- Detects and generates Remote and AIS alarms
- Programmable output clocks for Fractional E1, H0, and H12 applications
- Fully independent transmit and receive functionality
- Full access to both Si and Sa bits
- Three separate loopbacks for testing
- Large counters for bipolar and code violations, CRC4 code word errors, FAS errors, and E bits
- Pin compatible with DS2151Q T1 Single–Chip Transceiver
- 5V supply; low power CMOS
- Industrial grade version (–40°C to +85°C) available (DS2153QN)

PIN ASSIGNMENT



DESCRIPTION

The DS2153Q T1 Single–Chip Transceiver (SCT) contains all of the necessary functions for connection to E1 lines. The onboard clock/data recovery circuitry coverts the AMI/HDB3 E1 waveforms to a NRZ serial stream. The DS2153 automatically adjusts to E1 22 AWG (0.6 mm) twisted–pair cables from 0 to 1.5 KM. The device can generate the necessary G.703 waveshapes for both 75 ohm and 120 ohm cables. The onboard jitter

attenuator (selectable to either 32 bits or 128 bits) can be placed in either the transmit or receive data paths. The framer locates the frame and multiframe boundaries and monitors the data stream for alarms. It is also used for extracting and inserting signaling data, Si, and Sa–bit information. The device contains a set of 71 8–bit internal registers which the user can access to control the operation of the unit. Quick access via the parallel control port allows a single micro to handle many E1 lines. The device fully meets all of the latest E1 specifications including ITU G.703, G.704, G.706, G.823, and I.431 as well as ETSI 300 011, 300 233, TBR 12 and TBR 13.

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1.0 INTRODUCTION

The analog AMI waveform off of the E1 line is transformer coupled into the RRING and RTIP pins of the DS2153Q. The device recovers clock and data from the analog signal and passes it through the jitter attenuation mux to the receive side framer where the digital serial stream is analyzed to locate the framing pattern. If needed, the receive side elastic store can be enabled in order to absorb the phase and frequency differences between the recovered E1 data stream and an asynchronous backplane clock which is provided at the SYSCLK input.

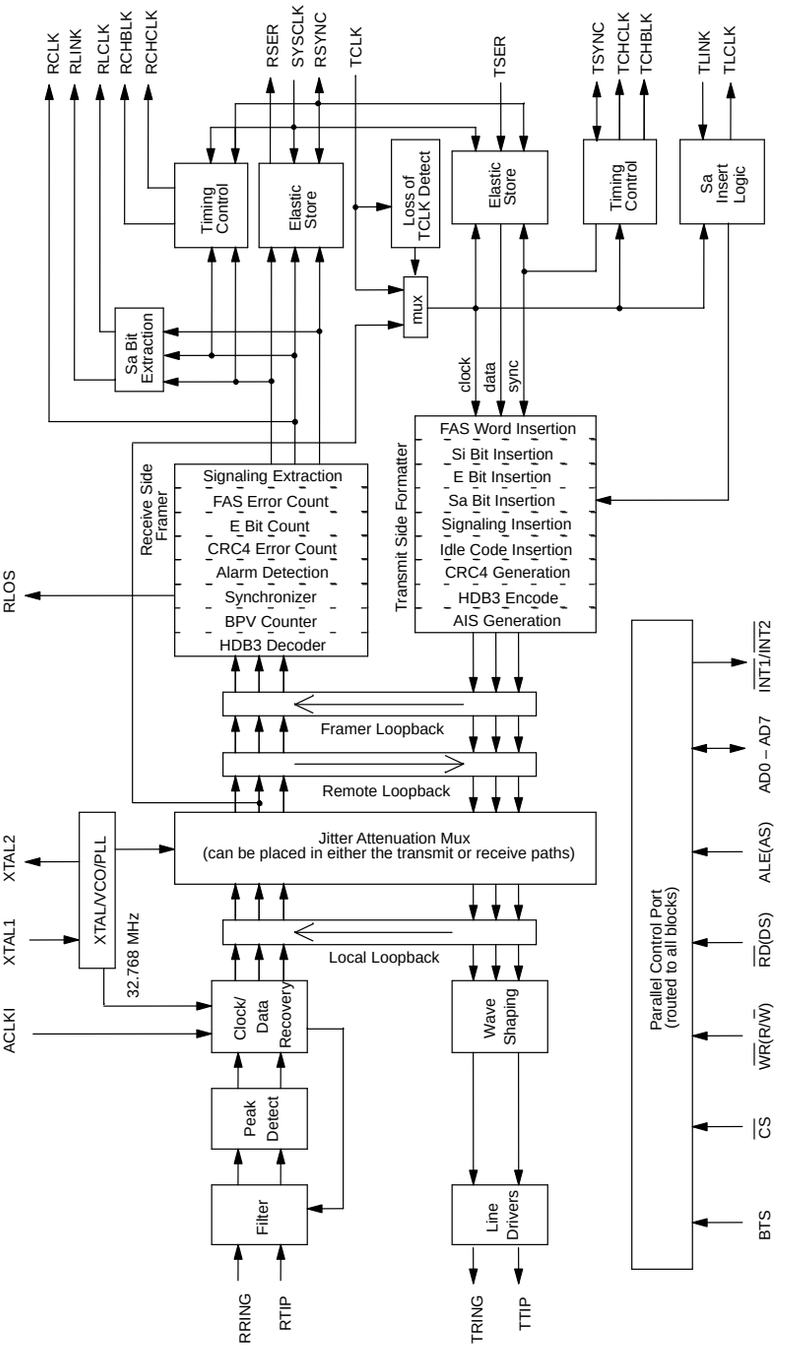
The transmit side of the DS2153Q is totally independent from the receive side in both the clock requirements and characteristics. The transmit formatter will provide the necessary data overhead for E1 transmission. Once the data stream has been prepared for transmission, it is sent via the jitter attenuation mux to the waveshaping and line driver functions. The DS2153Q will drive the E1 line from the TTIP and TRING pins via a coupling transformer.

Reader's Note

This data sheet assumes a particular nomenclature of the E1 operating environment. There are 32 8–bit timeslots in E1 systems which are numbered 0 to 31. Timeslot 0 is transmitted first and received first. These 32 timeslots are also referred to as channels with a numbering scheme of 1 to 32. Timeslot 0 is identical to channel 1, timeslot 1 is identical to channel 2, and so on. Each timeslot (or channel) is made up of eight bits which are numbered 1 to 8. Bit number 1 is the MSB and is transmitted first. Bit number 8 is the LSB and is transmitted last. Throughout this data sheet, the following abbreviations will be used:

FAS	Frame Alignment Signal
CAS	Channel Associated Signaling
MF	Multiframe
Si	International Bits
CRC4	Cyclical Redundancy Check
CCS	Common Channel Signaling
Sa	Additional bits
E–bit	CRC4 Error bits

DS2153Q BLOCK DIAGRAM Figure 1–1



PIN DESCRIPTION Table 1–1

PIN	SYMBOL	TYPE	DESCRIPTION
1 2 3 4	AD4 AD5 AD6 AD7	I/O	**Address/Data Bus**. A 8–bit multiplexed address/data bus.
5	$\overline{RD}$(DS)	I	**Read Input (Data Strobe)**.
6	$\overline{CS}$	I	**Chip Select**. Must be low to read or write the port.
7	ALE(AS)	I	**Address Latch Enable (Address Strobe)**. A positive going edge serves to demultiplex the bus.
8	$\overline{WR}$(R/$\overline{W}$)	I	**Write Input (Read/Write)**.
9	RLINK	O	**Receive Link Data**. Outputs the full receive data stream including the Sa bits. See Section 13 for timing details.
10	RLCLK	O	**Receive Link Clock**. 4 KHz to 20 KHz demand clock for the RLINK output; controlled by RCR2. See Section 13 for timing details.
11	DVSS	–	**Digital Signal Ground**. 0.0 volts. Should be tied to local ground plane.
12	RCLK	O	**Receive Clock**. Recovered 2.048 MHz clock.
13	RCHCLK	O	**Receive Channel Clock**. 256 KHz clock which pulses high during the LSB of each channel. Useful for parallel to serial conversion of channel data. See Section 13 for timing details.
14	RSER	O	**Receive Serial Data**. Received NRZ serial data, updated on rising edges of RCLK or SYSCLK.
15	RSYNC	I/O	**Receive Sync**. An extracted pulse, one RCLK wide, is output at this pin which identifies either frame (RCR1.6=0) or multiframe boundaries (RCR1.6=1). If the elastic store is enabled via the RCR2.1, then this pin can be enabled to be an input via RCR1.5 at which a frame boundary pulse is applied. See Section 13 for timing details.
16	RLOS/LOTC	O	**Receive Loss of Sync/Loss of Transmit Clock**. A dual function output. If TCR2.0=0, will toggle high when the synchronizer is searching for the E1 frame and multiframe; if TCR2.0=1, will toggle high if the TCLK pin has not toggled for 5 µs.
17	SYSCLK	I	**System Clock**. 1.544 MHz or 2.048 MHz clock. Only used when the elastic store functions are enabled via RCR2.1. Should be tied low in applications that do not use the elastic store. If tied high for at least 100 µs, will force all output pins (including the parallel port) to 3–state.
18	RCHBLK	O	**Receive Channel Block**. A user programmable output that can be forced high or low during any of the 32 E1 channels. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all E1 channels are used such as Fractional E1, 384 Kbps service (H0), 1920 Kbps (H12), or ISDN–PRI. Also useful for locating individual channels in drop–and–insert applications. See Section 13 for timing details.
19	ACLKI	I	**Alternate Clock Input**. Upon a receive carrier loss, the clock applied at this pin (normally 2.048 MHz) will be routed to the RCLK pin. If no clock is routed to this pin, then it should be tied to DVSS VIA A 1KΩ resistor.

PIN	SYMBOL	TYPE	DESCRIPTION
20	BTS	I	**Bus Type Select**. Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the $\overline{RD}$(DS), ALE(AS), and $\overline{WR}$(R/$\overline{W}$) pins. If BTS=1, then these pins assume the function listed in parenthesis ().
21 22	RTIP RRING	–	**Receive Tip and Ring**. Analog inputs for clock recovery circuitry; connects to a 1:1 transformer (see Section 12 for details).
23	RVDD	–	**Receive Analog Positive Supply**. 5.0 volts. Should be tied to DVDD and TVDD pins.
24	RVSS	–	**Receive Signal Ground**. 0.0 volts. Should be tied to local ground plane.
25 26	XTAL1 XTAL2	–	**Crystal Connections**. A pullable 8.192 MHz crystal must be applied to these pins. See Section 12 for crystal specifications.
27	$\overline{INT1}$	O	**Receive Alarm Interrupt 1**. Flags host controller during alarm conditions defined in Status Register 1. Active low, open drain output.
28	$\overline{INT2}$	O	**Receive Alarm Interrupt 2**. Flags host controller during conditions defined in Status Register 2. Active low, open drain output.
29	TTIP	–	**Transmit Tip**. Analog line driver output; connects to a step–up transformer (see Section 12 for details).
30	TVSS	–	**Transmit Signal Ground**. 0.0 volts. Should be tied to local ground plane.
31	TVDD	–	**Transmit Analog Positive Supply**. 5.0 volts. Should be tied to DVDD and RVDD pins.
32	TRING	–	**Transmit Ring**. Analog line driver outputs; connects to a step–up transformer (see Section 12 for details).
33	TCHBLK	O	**Transmit Channel Block**. A user programmable output that can be forced high or low during any of the 32 E1 channels. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all E1 channels are used such as Fractional E1, 384 Kbps service (H0), 1920 Kbps (H12), or ISDN–PRI. Also useful for locating individual channels in drop–and–insert applications. See Section 13 for timing details.
34	TLCLK	O	**Transmit Link Clock**. 4 KHz to 20 KHz demand clock for the TLINK input; controlled by TCR2. See Section 13 for timing details.
35	TLINK	I	**Transmit Link Data**. If enabled, this pin will be sampled on the falling edge of TCLK to insert the Sa bits See Section 13 for timing details.
36	TSYNC	I/O	**Transmit Sync**. A pulse at this pin will establish either frame or multiframe boundaries for the DS2153Q. Via TCR1.1, the DS2153Q can be programmed to output either a frame or multiframe pulse at this pin. See Section 13 for timing details.
37	DVDD	–	**Digital Positive Supply**. 5.0 volts. Should be tied to RVDD and TVDD pins.
38	TCLK	I	**Transmit Clock**. 2.048 MHz primary clock. Needed for proper operation of the parallel control port.
39	TSER	I	**Transmit Serial Data**. Transmit NRZ serial data, sampled on the falling edge of TCLK.

PIN	SYMBOL	TYPE	DESCRIPTION
40	TCHCLK	O	**Transmit Channel Clock**. 256 KHz clock which pulses high during the LSB of each channel. Useful for parallel to serial conversion of channel data. See Section 13 for timing details.
41 42 43 44	AD0 AD1 AD2 AD3	I/O	**Address/Data Bus**. A 8–bit multiplexed address/data bus.

DS2153Q REGISTER MAP

ADDRESS	R/W	REGISTER NAME	ADDRESS	R/W	REGISTER NAME
00	R	BPV or Code Violation Count 1	20	R/W	Transmit Align Frame
01	R	BPV or Code Violation Count 2	21	R/W	Transmit Non–Align Frame
02	R	CRC4 Count 1/FAS Error Count 1	22	R/W	Transmit Channel Blocking 1
03	R	CRC4 Error Count 2	23	R/W	Transmit Channel Blocking 2
04	R	E–Bit Count 1/FAS Error Count 2	24	R/W	Transmit Channel Blocking 3
05	R	E–Bit Count 2	25	R/W	Transmit Channel Blocking 4
06	R	Status 1	26	R/W	Transmit Idle 1
07	R	Status 2	27	R/W	Transmit Idle 2
08	R/W	Receive Information	28	R/W	Transmit Idle 3
10	R/W	Receive Control 1	29	R/W	Transmit Idle 4
11	R/W	Receive Control 2	2A	R/W	Transmit Idle Definition
12	R/W	Transmit Control 1	2B	R/W	Receive Channel Blocking 1
13	R/W	Transmit Control 2	2C	R/W	Receive Channel Blocking 2
14	R/W	Common Control 1	2D	R/W	Receive Channel Blocking 3
15	R/W	Test 1	2E	R/W	Receive Channel Blocking 4
16	R/W	Interrupt Mask 1	2F	R	Receive Align Frame
17	R/W	Interrupt Mask 2			
18	R/W	Line Interface Control			
19	R/W	Test 2			
1A	R/W	Common Control 2			
1B	R/W	Common Control 3			
1E	R	Synchronizer Status			
1F	R	Receive Non–Align Frame			

ADDRESS	R/W	REGISTER NAME	ADDRESS	R/W	REGISTER NAME
30	R	Receive Signaling 1	40	R/W	Transmit Signaling 1
31	R	Receive Signaling 2	41	R/W	Transmit Signaling 2
32	R	Receive Signaling 3	42	R/W	Transmit Signaling 3
33	R	Receive Signaling 4	43	R/W	Transmit Signaling 4
34	R	Receive Signaling 5	44	R/W	Transmit Signaling 5
35	R	Receive Signaling 6	45	R/W	Transmit Signaling 6
36	R	Receive Signaling 7	46	R/W	Transmit Signaling 7
37	R	Receive Signaling 8	47	R/W	Transmit Signaling 8
38	R	Receive Signaling 9	48	R/W	Transmit Signaling 9
39	R	Receive Signaling 10	49	R/W	Transmit Signaling 10
3A	R	Receive Signaling 11	4A	R/W	Transmit Signaling 11
3B	R	Receive Signaling 12	4B	R/W	Transmit Signaling 12
3C	R	Receive Signaling 13	4C	R/W	Transmit Signaling 13
3D	R	Receive Signaling 14	4D	R/W	Transmit Signaling 14
3E	R	Receive Signaling 15	4E	R/W	Transmit Signaling 15
3F	R	Receive Signaling 16	4F	R/W	Transmit Signaling 16

Note: the Test Registers 1 and 2 are used only by the factory; these registers must be cleared (set to all zeros) on power–up initialization to insure proper operation.

2.0 PARALLEL PORT

The DS2153Q is controlled via a multiplexed bidirectional address/data bus by an external microcontroller or microprocessor. The DS2153Q can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in the AC Electrical Characteristics for more details. The multiplexed bus on the DS2153Q saves pins because the address information and data information share the same signal paths. The addresses are presented to the pins in the first portion of the bus cycle and data will be transferred on the pins during second portion of the bus cycle. Addresses must be valid prior to the falling edge of ALE(AS), at which time the DS2153Q latches the address from the AD0 to AD7 pins. Valid write data must be present and held stable during the later portion of the DS $\overline{WR}$ pulses. In a read cycle, the DS2153Q outputs a byte of data during the latter portion of the DS or $\overline{RD}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ transitions high in Intel timing or as DS transitions low in Motorola timing.

3.0 CONTROL AND TEST REGISTERS

The operation of the DS2153Q is configured via a set of seven registers. Typically, the control registers are only accessed when the system is first powered up. Once the DS2153Q has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Register (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), and three Common Control Registers (CCR1, CCR2 and CCR3). Each of the seven registers are described in this section.

The Test Registers at addresses 15 and 19 hex are used by the factory in testing the DS2153Q. On power–up, the Test Registers should be set to 00 hex in order for the DS2153Q to operate properly.

RCR1: RECEIVE CONTROL REGISTER 1 (Address=10 Hex)

(MSB)							(LSB)
RSMF	RSM	RSIO	–	–	FRC	SYNCE	RESYNC

SYMBOL	POSITION	NAME AND DESCRIPTION
RSMF	RCR1.7	**RSYNC Multiframe Function**. Only used if the RSYNC pin is programmed in the multiframe mode (RCR1.6=1). 0=RSYNC outputs CAS multiframe boundaries 1=RSYNC outputs CRC4 multiframe boundaries
RSM	RCR1.6	**RSYNC Mode Select**. 0=frame mode (see the timing in Section 13) 1=multiframe mode (see the timing in Section 13)
RSIO	RCR1.5	**RSYNC I/O Select**. 0=RSYNC is an output (depends on RCR1.6) 1=RSYNC is an input (only valid if elastic store enabled) (note: this bit must be set to zero when RCR2.1=0)
–	RCR1.4	**Not Assigned**. Should be set to zero when written.
–	RCR1.3	**Not Assigned**. Should be set to zero when written.
FRC	RCR1.2	**Frame Resync Criteria**. 0=resync if FAS received in error 3 consecutive times 1=resync if FAS or bit 2 of non–FAS is received in error 3 consecutive times
SYNCE	RCR1.1	**Sync Enable**. 0=auto resync enabled 1=auto resync disabled
RESYNC	RCR1.0	**Resync**. When toggled from low to high, a resync is initiated. Must be cleared and set again for a subsequent resync.

SYNC/RESYNC CRITERIA Table 3–1

FRAME OR MULTIFRAME LEVEL	SYNC CRITERIA	RESYNC CRITERIA	ITU SPEC.
FAS	FAS present in frames N and N + 2, and FAS not present in frame N + 1.	Three consecutive incorrect FAS received. Alternate (RCR1.2=1) the above criteria is met or three consecutive incorrect bit 2 of non–FAS received.	G.706 4.1.1 4.1.2
CRC4	Two valid MF alignment words found within 8 ms.	915 or more CRC4 code words out of 1000 received in error.	G.706 4.2 4.3.2
CAS	Valid MF alignment word found and previous time slot 16 contains code other than all zeros.	Two consecutive MF alignment words received in error.	G.732 5.2

RCR2: RECEIVE CONTROL REGISTER 2 (Address=11 Hex)

(MSB)							(LSB)
Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	RSCLKM	RESE	–

SYMBOL	POSITION	NAME AND DESCRIPTION
Sa8S	RCR2.7	**Sa8 Bit Select**. Set to one to report the Sa8 bit at the RLINK pin; set to zero to not report the Sa8 bit.
Sa7S	RCR2.6	**Sa7 Bit Select**. Set to one to report the Sa7 bit at the RLINK pin; set to zero to not report the Sa7 bit.
Sa6S	RCR2.5	**Sa6 Bit Select**. Set to one to report the Sa6 bit at the RLINK pin; set to zero to not report the Sa6 bit.
Sa5S	RCR2.4	**Sa5 Bit Select**. Set to one to report the Sa5 bit at the RLINK pin; set to zero to not report the Sa5 bit.
Sa4S	RCR2.3	**Sa4 Bit Select**. Set to one to report the Sa4 bit at the RLINK pin; set to zero to not report the Sa4 bit.
RSCLKM	RCR2.2	**Receive Side SYSCLK Mode Select**. 0=if SYSCLK is 1.544 MHz 1=if SYSCLK is 2.048 MHz
RESE	RCR2.1	**Receive Side Elastic Store Enable**. 0=elastic store is bypassed 1=elastic store is enabled
–	RCR2.0	**Not Assigned**. Should be set to zero when written.

TCR1: TRANSMIT CONTROL REGISTER 1 (Address=12 Hex)

(MSB)							(LSB)
–	TFPT	T16S	TUA1	TSiS	TSA1	TSM	TSIO

SYMBOL	POSITION	NAME AND DESCRIPTION
–	TCR1.7	**Not Assigned**. Should be set to zero when written to.
TFPT	TCR1.6	**Transmit Timeslot 0 Pass Through**. 0=FAS bits/Sa bits/Remote Alarm sourced internally from the TAF and TNAF registers 1=FAS bits/Sa bits/Remote Alarm sourced from TSER
T16S	TCR1.5	**Transmit Timeslot 16 Data Select**. 0=sample timeslot 16 at TSER pin 1=source timeslot 16 from TS1 to TS16 registers
TUA1	TCR1.4	**Transmit Unframed All Ones**. 0=transmit data normally 1=transmit an unframed all one's code at TPOS and TNEG
TSiS	TCR1.3	**Transmit International Bit Select**. 0=sample Si bits at TSER pin 1=source Si bits from TAF and TNAF registers (in this mode, TCR1.6 must be set to 0)

TSA1	TCR1.2	**Transmit Signaling All Ones**. 0=normal operation 1=force timeslot 16 in every frame to all ones
TSM	TCR1.1	**TSYNC Mode Select**. 0=frame mode (see the timing in Section 13) 1=CAS and CRC4 multiframe mode (see the timing in Section 13)
TSIO	TCR1.0	**TSYNC I/O Select**. 0=TSYNC is an input 1=TSYNC is an output

Note: See Figure 13–9 for more details about how the Transmit Control Registers affect the operation of the DS2153Q.

TCR2: TRANSMIT CONTROL REGISTER 2 (Address=13 Hex)

(MSB)							(LSB)
Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	–	AEBE	P16F

SYMBOL	POSITION	NAME AND DESCRIPTION
Sa8S	TCR2.7	**Sa8 Bit Select**. Set to one to source the Sa8 bit from the TLINK pin; set to zero to not source the Sa8 bit.
Sa7S	TCR2.6	**Sa7 Bit Select**. Set to one to source the Sa7 bit from the TLINK pin; set to zero to not source the Sa7 bit.
Sa6S	TCR2.5	**Sa6 Bit Select**. Set to one to source the Sa6 bit from the TLINK pin; set to zero to not source the Sa6 bit.
Sa5S	TCR2.4	**Sa5 Bit Select**. Set to one to source the Sa5 bit from the TLINK pin; set to zero to not source the Sa5 bit.
Sa4S	TCR2.3	**Sa4 Bit Select**. Set to one to source the Sa4 bit from the TLINK pin; set to zero to not source the Sa4 bit.
–	TCR2.2	**Not Assigned**. Should be set to zero when written.
AEBE	TCR2.1	**Automatic E–Bit Enable**. 0=E–bits not automatically set in the transmit direction 1=E–bits automatically set in the transmit direction
P16F	TCR2.0	**Function of Pin 16**. 0=Receive Loss of Sync (RLOS) 1=Loss of Transmit Clock (LOTC)

CCR1: COMMON CONTROL REGISTER 1 (Address=14 Hex)

(MSB)							(LSB)
FLB	THDB3	TG802	TCRC4	RSM	RHDB3	RG802	RCRC4

SYMBOL	POSITION	NAME AND DESCRIPTION
FLB	CCR1.7	**Framer Loopback**. 0=loopback disabled 1=loopback enabled

THDB3	CCR1.6	**Transmit HDB3 Enable**. 0=HDB3 disabled 1=HDB3 enabled
TG802	CCR1.5	**Transmit G.802 Enable**. See Section 13 for details. 0=do not force TCHBLK high during bit 1 of timeslot 26 1=force TCHBLK high during bit 1 of timeslot 26
TCRC4	CCR1.4	**Transmit CRC4 Enable**. 0=CRC4 disabled 1=CRC4 enabled
RSM	CCR1.3	**Receive Signaling Mode Select**. 0=CAS signaling mode 1=CCS signaling mode
RHDB3	CCR1.2	R**eceive HDB3 Enable**. 0=HDB3 disabled 1=HDB3 enabled
RG802	CCR1.1	**Receive G.802 Enable**. See Section 13 for details. 0=do not force RCHBLK high during bit 1 of timeslot 26 1=force RCHBLK high during bit 1 of timeslot 26
RCRC4	CCR1.0	**Receive CRC4 Enable**. 0=CRC4 disabled 1=CRC4 enabled

FRAMER LOOPBACK

When CCR1.7 is set to a one, the DS2153Q will enter a Framer LoopBack (FLB) mode. This loopback is useful in testing and debugging applications. In FLB, the DS2153Q will loop data from the transmit side back to the receive side. When FLB is enabled, the following will occur:

1. data will be transmitted as normal at TTIP and TRING
2. data off the E1 line at RTIP and RRING will be ignored
3. the RCLK output will be replaced with the TCLK input.

CCR2: COMMON CONTROL REGISTER 2 (Address=1A Hex)

(MSB)							**(LSB)**
ECUS	VCRFS	AAIS	ARA	RSERC	LOTCMC	RLB	LLB

SYMBOL	POSITION	NAME AND DESCRIPTION
ECUS	CCR2.7	**Error Counter Update Select**. 0=update error counters once a second 1=update error counters every 62.5 ms (500 frames)
VCRFS	CCR2.6	**VCR Function Select**. 0=count BiPolar Violations (BPVs) 1=count Code Violations (CVs)
AAIS	CCR2.5	**Automatic AIS Generation**. 0=disabled 1=enabled
ARA	CCR2.4	**Automatic Remote Alarm Generation**. 0=disabled 1=enabled

RSERC	CCR2.3	**RSER Control**. 0=allow RSER to output data as received under all conditions 1=force RSER to one under loss of frame alignment conditions
LOTCMC	CCR2.2	**Loss of Transmit Clock Mux Control**. Determines whether the transmit side formatter should switch to the ever present RCLK if the TCLK should fail to transition (see Figure 1.1). 0=do not switch to RCLK if TCLK stops 1=switch to RCLK if TCLK stops
RLB	CCR2.1	**Remote Loopback**. 0=loopback disabled 1=loopback enabled
LLB	CCR2.0	**Local Loopback**. 0=loopback disabled 1=loopback enabled

REMOTE LOOPBACK

When CCR2.1 is set to a one, the DS2153Q will be forced into Remote LoopBack (RLB). In this loopback, data recovered off of the E1 line from the RTIP and RRING pins will be transmitted back onto the E1 line (with any BPV's that might have occurred intact) via the TTIP and TRING pins. Data will continue to pass through the receive side of the DS2153Q as it would normally and the data at the TSER pin will be ignored. Data in this loopback will pass through the jitter attenuator. Please see Figure 1.1 for more details.

LOCAL LOOPBACK

When CCR2.0 is set to a one, the DS2153Q will be forced into Local LoopBack (LLB). In this loopback, data will continue to be transmitted as normal through the transmit side of the SCT. Data being received at RTIP and RRING will be replaced with the data being transmitted. Data in this loopback will pass through the jitter attenuator. Please see Figure 1.1 for more details.

AUTOMATIC ALARM GENERATION

When either CCR2.4 or CCR2.5 is set to one, the DS2153Q monitors the receive side to determine if any of the following conditions are present: loss of receive frame synchronization, AIS alarm (all ones) reception, or loss of receive carrier (or signal). If any one (or more) of the above conditions is present, then the DS2151Q will either force an AIS alarm (if CCR2.5=1) or a Remote Alarm (CCR2.4=1) to be transmitted via the TTIP and TRING pins. It is an illegal state to have both CCR2.4 and CCR2.5 set to one at the same time.

CCR3: COMMON CONTROL REGISTER 3 (Address=1B Hex)

(MSB)							(LSB)
TESE	TCBFS	TIRFS	ESR	LIRST	–	TSCLKM	–

SYMBOL	POSITION	NAME AND DESCRIPTION
TESE	CCR3.7	**Transmit Elastic Store Enable.** 0 = elastic store is disabled 1 = elastic store is enabled
TCBFS	CCR3.6	**Transmit Channel Blocking Registers (TCBR) Function Select**. 0=TCBRs define the operation of the TCHBLK output pin 1=TCBRs define which signaling bits are to be inserted
TIRFS	CCR3.5	**Transmit Idle Registers (TIR) Function Select**. 0=TIRs define in which channels to insert idle code 1=TIRs define in which channels to insert data from RSER
ESR	CCR3.4	**Elastic Stores Reset**. Setting this bit from a one to a zero will force the elastic stores to a known depth. Should be toggled after SYSCLK has been

		applied and is stable. Must be set and cleared again for a subsequent reset. Do not leave this bit set high.
LIRST	CCR3.3	**Line Interface Reset**. Setting this bit from a zero to a one will initiate an internal reset that affects the slicer, AGC, clock recovery state machine, and jitter attenuator. Normally this bit is only toggled on power–up. Must be cleared and set again for a subsequent reset.
–	CCR3.2	**Not Assigned**. Should be set to zero when written.
TSCLKM	CCR3.1	**Transmit Backplane Clock Select.** Must be set like RCR2.2. 0 = 1.544 MHz 1 = 2.048 MHz
–	CCR3.0	**Not Assigned**. Should be set to zero when written.

POWER–UP SEQUENCE

On power–up, after the supplies are stable, the DS2153Q should be configured for operation by writing to all of the internal registers (this includes the Test Registers) since the contents of the internal registers cannot be predicted on power–up. Next, the LIRST bit should be toggled from zero to one to reset the line interface circuitry (it will take the DS2153Q about 40 ms to recover from the LIRST bit being toggled). Finally, after the SYSCLK input is stable, the ESR bit should be toggled from a zero to a one and back to zero (this step can be skipped if the elastic store is not being used).

4.0 STATUS AND INFORMATION REGISTERS

There is a set of four registers that contain information on the current real time status of the DS2153Q, Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Register (RIR), and Synchronizer Status Register (SSR). When a particular event has occurred (or is occurring), the appropriate bit in one of these four registers will be set to a one. All of the bits in these registers operate in a latched fashion (except for the SSR). This means that if an event occurs and a bit is set to a one in any of the registers, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again or if the alarm is still present.

The user will always precede a read of the SR1, SR2, and RIR registers with a write. The byte written to the register will inform the DS2153Q which bits the user wishes to read and have cleared. The user will write a byte to one of these three registers, with a one in the bit positions he or she wishes to read and a zero in the bit positions he or she does not wish to obtain the latest information on. When a one is written to a bit location, the read register will be updated with current value and it will be cleared. When a zero is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that bit does indeed clear. This second write step is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. This write–read–write scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS2153Q with higher–order software languages.

The SSR register operates differently than the other three. It is a read only register and it reports the status of the synchronizer in real time. This register is not latched and it is not necessary to precede a read of this registers with a write.

The SR1 and SR2 registers have the unique ability to initiate a hardware interrupt via the $\overline{INT1}$ and $\overline{INT2}$ pins respectively. Each of the alarms and events in the SR1 and SR2 can be either masked or unmasked from the interrupt pins via the Interrupt Mask Register 1 (IMR1) and Interrupt Mask Register 2 (IMR2) respectively.

RIR: RECEIVE INFORMATION REGISTER (Address=08 Hex)

(MSB)							(LSB)
TESF	TESE	JALT	RESF	RESE	CRCRC	FASRC	CASRC

SYMBOL	POSITION	NAME AND DESCRIPTION
TESF	RIR.7	**Transmit Elastic Store Full.** Set when the elastic store fills and a frame is deleted.
TESE	RIR.6	**Transmit Elastic Store Empty.** Set when the elastic store empties and a frame is repeated.
JALT	RIR.5	**Jitter Attenuator Limit Trip**. Set when the jitter attenuator FIFO reaches to within 4–bits of it's limit; useful for debugging jitter attenuation operation.
RESF	RIR.4	**Elastic Store Full**. Set when the elastic store buffer fills and a frame is deleted.
RESE	RIR.3	**Elastic Store Empty**. Set when the elastic store buffer empties and a frame is repeated.
CRCRC	RIR.2	**CRC Resync Criteria Met.** Set when 915/1000 code words are received in error.
FASRC	RIR.1	**FAS Resync Criteria Met**. Set when three consecutive FAS words are received in error.
CASRC	RIR.0	**CAS Resync Criteria Met**. Set when two consecutive CAS MF alignment words are received in error.

SSR: SYNCHRONIZER STATUS REGISTER (Address=1E Hex)

(MSB)							(LSB)
CSC5	CSC4	CSC3	CSC2	CSC0	FASSA	CASSA	CRC4SA

SYMBOL	POSITION	NAME AND DESCRIPTION
CSC5	SSR.7	**CRC4 Sync Counter Bit 5**. MSB of the 6–bit counter.
CSC4	SSR.6	**CRC4 Sync Counter Bit 4**.
CSC3	SSR.5	**CRC4 Sync Counter Bit 3**.
CSC2	SSR.4	**CRC4 Sync Counter Bit 2**.
CSC0	SSR.3	**CRC4 Sync Counter Bit 0**. LSB of the 6–bit counter. The next to LSB bit is not accessible. This bit will toggle each time the CRC4 MF search times out at 8 ms.
FASSA	SSR.2	**FAS Sync Active**. Set while the synchronizer is searching for alignment at the FAS level.
CASSA	SSR.1	**CAS MF Sync Active**. Set while the synchronizer is searching for the CAS MF alignment word.
CRC4SA	SSR.0	**CRC4 MF Sync Active**. Set while the synchronizer is searching for the CRC4 MF alignment word.

CRC4 SYNC COUNTER

The CRC4 Sync Counter increments each time the 8 ms CRC4 multiframe search times out. The counter is cleared when the DS2153Q has successfully obtained synchronization at the CRC4 level. The counter can also be cleared by disabling the CRC4 mode (CCR1.0=0). This counter is useful for determining the amount of time the DS2153Q has been searching for synchronization at the CRC4 level. Annex B of CCITT G.706 suggests that if synchronization at the CRC4 level cannot be obtained within 400 ms, then the search should be abandoned and proper action taken. The CRC4 Sync Counter will rollover.

SR1: STATUS REGISTER 1 (Address=06 Hex)

(MSB) **(LSB)**

RSA1	RDMA	RSA0	RSLIP	RUA1	RRA	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
RSA1	SR1.7	**Receive Signaling All Ones**. Set when the contents of timeslot 16 contains less than three zeros over 16 consecutive frames. This alarm is not disabled in the CCS signaling mode.
RDMA	SR1.6	**Receive Distant MF Alarm**. Set when bit 6 of timeslot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode.
RSA0	SR1.5	**Receive Signaling All Zeros**. Set when over a full MF, timeslot 16 contains all zeros.
RSLIP	SR1.4	**Receive Elastic Store Slip Occurrence**. Set when the elastic store has either repeated or deleted a frame of data.
RUA1	SR1.3	**Receive Unframed All Ones**. Set when an unframed all ones code is received at RTIP and RRING.
RRA	SR1.2	**Receive Remote Alarm**. Set when a remote alarm is received at RTIP and RRING.
RCL	SR1.1	**Receive Carrier Loss**. Set when 255 consecutive zeros have been detected at RTIP and RRING.
RLOS	SR1.0	**Receive Loss of Sync**. Set when the device is not synchronized to the receive E1 stream.

ALARM CRITERIA Table 4–1

ALARM	SET CRITERIA	CLEAR CRITERIA	CCITT SPEC.
RSA1 (receive signaling all ones)	over 16 consecutive frames (one full MF) timeslot 16 contains less than 3 zeros	over 16 consecutive frames (one full MF) timeslot 16 contains 3 or more zeros	G.732 4.2
RSA0 (receive signaling all zeros)	over 16 consecutive frames (one full MF) timeslot 16 contains all zeros	over 16 consecutive frames (one full MF) timeslot 16 contains at least a single one	G.732 5.2
RDMA (receive distant multiframe alarm)	bit 6 in timeslot 16 of frame 0 set to one for two consecutive MF	bit 6 in timeslot 16 of frame 0 set to zero for a two consecutive MF	O.162 2.1.5
RUA1 (receive unframed all ones)	less than 3 zeros in two frames (512 bits)	more than 2 zeros in two frames (512 bits)	O.162 1.6.1.2
RRA (receive remote alarm)	bit 3 of non–align frame set to one for 3 consecutive occasions	bit 3 of non–align frame set to zero for 3 consecutive occasions	O.162 2.1.4
RCL (receive carrier loss)	255 consecutive zeros received	in 255–bit times, at least 32 ones are received	G.775

SR2: STATUS REGISTER 2 (Address=07 Hex)

(MSB)							**(LSB)**
RMF	RAF	TMF	SEC	TAF	LOTC	RCMF	TSLIP

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	SR2.7	**Receive CAS Multiframe**. Set every 2 ms (regardless if CAS signaling is enabled or not) on receive multiframe boundaries. Used to alert the host that signaling data is available.
RAF	SR2.6	**Receive Align Frame**. Set every 250 µs at the beginning of align frames. Used to alert the host that Si and Sa bits are available in the RAF and RNAF registers.
TMF	SR2.5	**Transmit Multiframe**. Set every 2 ms (regardless if CRC4 is enabled) on transmit multiframe boundaries. Used to alert the host that signaling data needs to be updated.
SEC	SR2.4	**One Second Timer**. Set on increments of one second based on RCLK. If CCR2.7=1, then this bit will be set every 62.5 ms instead of once a second.
TAF	SR2.3	**Transmit Align Frame**. Set every 250 µs at the beginning of align frames. Used to alert the host that the TAF and TNAF registers need to be updated.
LOTC	SR2.2	**Loss of Transmit Clock**. Set when the TCLK pin has not transitioned for one channel time (or 3.9 µs). Will force pin 16 high if enabled via TCR2.0. Based on RCLK.
RCMF	SR2.1	**Receive CRC4 Multiframe**. Set on CRC4 multiframe boundaries; will continue to be set every 2 ms on an arbitrary boundary if CRC4 is disabled.
TSLIP	SR2.0	**Transmit Elastic Store Slip.** Set when the elastic store has either repeated or deleted a frame of data.

IMR1: INTERRUPT MASK REGISTER 1 (Address=16 Hex)

(MSB)							**(LSB)**
RSA1	RDMA	RSA0	RSLIP	RUA1	RRA	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
RSA1	IMR1.7	**Receive Signaling All Ones**. 0=interrupt masked 1=interrupt enabled
RDMA	IMR1.6	**Receive Distant MF Alarm**. 0=interrupt masked 1=interrupt enabled
RSA0	IMR1.5	**Receive Signaling All Zeros**. 0=interrupt masked 1=interrupt enabled
RSLIP	IMR1.4	**Receive Elastic Store Slip Occurrence**. 0=interrupt masked 1=interrupt enabled
RUA1	IMR1.3	**Receive Unframed All Ones**. 0=interrupt masked 1=interrupt enabled
RRA	IMR1.2	**Receive Remote Alarm**. 0=interrupt masked 1=interrupt enabled
RCL	IMR1.1	**Receive Carrier Loss**. 0=interrupt masked 1=interrupt enabled
RLOS	IMR1.0	**Receive Loss of Sync**. 0=interrupt masked 1=interrupt enabled

IMR2: INTERRUPT MASK REGISTER 2 (Address=17 Hex)

(MSB)							(LSB)
RMF	RAF	TMF	SEC	TAF	LOTC	RCMF	TSLIP

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	IMR2.7	**Receive CAS Multiframe**. 0=interrupt masked 1=interrupt enabled
RAF	IMR2.6	**Receive Align Frame**. 0=interrupt masked 1=interrupt enabled
TMF	IMR2.5	**Transmit Multiframe**. 0=interrupt masked 1=interrupt enabled
SEC	IMR2.4	**One Second Timer**. 0=interrupt masked 1=interrupt enabled
TAF	IMR2.3	**Transmit Align Frame**. 0=interrupt masked 1=interrupt enabled
LOTC	IMR2.2	**Loss Of Transmit Clock**. 0=interrupt masked 1=interrupt enabled
RCMF	IMR2.1	**Receive CRC4 Multiframe**. 0=interrupt masked 1=interrupt enabled
TSLIP	IMR2.0	**Transmit Side Elastic Store Slip.** 0 = interrupt masked 1 = interrupt enabled

5.0 ERROR COUNT REGISTERS

There are a set of four counters in the DS2153Q that record bipolar or code violations, errors in the CRC4 SMF code words, E bits as reported by the far end, and word errors in the FAS. Each of these four counters are automatically updated on either one second boundaries (CCR2.7=0) or every 62.5 ms (CCR2.7=1) as determined by the timer in Status Register 2 (SR2.4). Hence, these registers contain performance data from either the previous second or the previous 62.5 ms. The user can use the interrupt from the timer to determine when to read these registers. The user has a full second (or 62.5 ms) to read the counters before the data is lost.

5.1 BPV or Code Violation Counter

Violation Count Register 1 (VCR1) is the most significant word and VCR2 is the least significant word of a 16–bit counter that records either BiPolar Violations (BPVs) or Code Violations (CVs). If CCR2.6=0, then the VCR counts bipolar violations. Bipolar violations are defined as consecutive marks of the same polarity. In this mode, if the HDB3 mode is set for the receive side via CCR1.2, then HDB3 code words are not counted as BPVs. If CCR2.6=1, then the VCR counts code violations as defined in CCITT O.161. Code violations are defined as consecutive bipolar violations of the same polarity. In most applications, the DS2153Q should be programmed to count BPVs when receiving AMI code and to count CVs when receiving HDB3 code. This counter increments at all times and is not disabled by loss of sync conditions. The counter saturates at 65,535 and will not rollover. The bit error rate on a E1 line would have to be greater than 10**–2 before the VCR would saturate.

VCR1: UPPER BIPOLAR VIOLATION COUNT REGISTER 1 (Address=00 Hex)
VCR2: LOWER BIPOLAR VIOLATION COUNT REGISTER 2 (Address=01 Hex)

(MSB)							(LSB)	
V15	V14	V13	V12	V11	V10	V9	V8	VCR1
V7	V6	V5	V4	V3	V2	V1	V0	VCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
V15	VCR1.7	MSB of the 16–bit bipolar or code violation count
V0	VCR2.0	LSB of the 16–bit bipolar or code violation count

5.2 CRC4 Error Counter

CRC4 Count Register 1 (CRCCR1) is the most significant word and CRCCR2 is the least significant word of a 10–bit counter that records word errors in the Cyclic Redundancy Check 4 (CRC4). Since the maximum CRC4 count in a one second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

CRCCR1: CRC4 COUNT REGISTER 1 (Address=02 Hex)
CRCCR2: CRC4 COUNT REGISTER 2 (Address=03 Hex)

(MSB)							(LSB)	
(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	CRC9	CRC8	CRCCR1
CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0	CRCCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC9	CRCCR1.1	MSB of the 10–bit CRC4 error count
CRC0	CRCCR2.0	LSB of the 10–bit CRC4 error count

NOTES:

1. The upper six bits of CRCCR1 at address 02 are the most significant bits of the 12–bit FAS error counter.

5.3 E–Bit Counter

E–bit Count Register 1 (EBCR1) is the most significant word and EBCR2 is the least significant word of a 10–bit counter that records Far End Block Errors (FEBE) as reported in the first bit of frames 13 and 15 on E1 lines running with CRC4 multiframe. These count registers will increment once each time the received E–bit is set to zero. Since the maximum E–bit count in a one second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

EBCR1: E–BIT COUNT REGISTER 1 (Address=04 Hex)
EBCR2: E–BIT COUNT REGISTER 2 (Address=05 Hex)

(MSB)							(LSB)	
(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	EB9	EB8	EBCR1
EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0	EBCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
EB9	EBCR1.1	MSB of the 10–bit E–Bit count
EB0	EBCR2.0	LSB of the 10–bit E–Bit count

NOTES:

1. The upper six bits of EBCR1 at address 04 are the least significant bits of the 12–bit FAS error counter.

5.4 FAS Bit Error Counter

FAS Count Register 1 (FASCR1) is the most significant word and FASCR2 is the least significant word of a 12–bit counter that records word errors in the Frame Alignment Signal in timeslot 0. This counter is disabled during loss of synchronization conditions, (RLOS = 1). Since the maximum FAS word error count in a one second period is 4000, this counter cannot saturate.

FASCR1: FAS BIT COUNT REGISTER 1 (Address=02 Hex)
FASCR2: FAS BIT COUNT REGISTER 2 (Address=04 Hex)

(MSB)							(LSB)	
FAS11	FAS10	FAS9	FAS8	FAS7	FAS6	(note 2)	(note 2)	FASCR1
FAS5	FAS4	FAS3	FAS2	FAS1	FAS0	(note 1)	(note 1)	FASCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
FAS11	FASCR1.7	MSB of the 12–bit FAS error count
FAS0	FASCR2.2	LSB of the 12–bit FAS error count

NOTES:

1. The lower two bits of FASCR1 at address 02 are the most significant bits of the 10–bit CRC4 error counter.
2. The lower two bits of FASCR2 at address 04 are the most significant bits of the 10–bit E–Bit counter.

6.0 Sa DATA LINK CONTROL AND OPERATION

The DS2153Q provides for access to the proposed E1 performance monitor data link in the Sa bit positions. The device allows access to the Sa bits either via a set of two internal registers (RNAF and TNAF) or via two external pins (RLINK and TLINK).

On the receive side, the Sa bits are always reported in the internal RNAF register (see Section 11 for more details). All five Sa bits are always output at the RLINK pin. See Section 13 for detailed timing. Via RCR2, the user can control the RLCLK pin to pulse during any combination of Sa bits. This allows the user to create a clock that can be used to capture the needed Sa bits.

On the transmit side, the individual Sa bits can be either sourced from the internal TNAF register (TCR1.6=0) or from the external TLINK pin. Via TCR2, the DS2153Q can be programmed to source any combination of the additional bits from the TLINK pin. If the user wishes to pass the Sa bits through the DS2153Q without them

being altered, then the device should be set up to source all five Sa bits via the TLINK pin and the TLINK pin should be tied to the TSER pin. Please see the timing diagrams and the transmit data flow diagram in Section 13 for examples.

7.0 SIGNALING OPERATION

The Channel Associated Signaling (CAS) bits embedded in the E1 stream can be extracted from the receive stream and inserted into the transmit stream by the DS2153Q. Each of the 30 channels has four signaling bits (A/B/C/D) associated with it. The numbers in parenthesis () are the channel associated with a particular signaling bit. The channel numbers have been assigned as described in the ITU documents. For example, channel 1 is associated with timeslot 1 and channel 30 is associated with timeslot 31. There is a set of 16 registers for the receive side (RS1 to RS16) and 16 registers on the transmit side (TS1 to TS16). The signaling registers are detailed below.

RS1 TO RS16: RECEIVE SIGNALING REGISTERS (Address=30 to 3F Hex)

(MSB)							**(LSB)**	
0	**0**	**0**	**0**	**X**	**Y**	**X**	**X**	RS1 (30)
A(1)	B(1)	C(1)	D(1)	A(16)	B(16)	C(16)	D(16)	RS2 (31)
A(2)	B(2)	C(2)	D(2)	A(17)	B(17)	C(17)	D(17)	RS3 (32)
A(3)	B(3)	C(3)	D(3)	A(18)	B(18)	C(18)	D(18)	RS4 (33)
A(4)	B(4)	C(4)	D(4)	A(19)	B(19)	C(19)	D(19)	RS5 (34)
A(5)	B(5)	C(5)	D(5)	A(20)	B(20)	C(20)	D(20)	RS6 (35)
A(6)	B(6)	C(6)	D(6)	A(21)	B(21)	C(21)	D(21)	RS7 (36)
A(7)	B(7)	C(7)	D(7)	A(22)	B(22)	C(22)	D(22)	RS8 (37)
A(8)	B(8)	C(8)	D(8)	A(23)	B(23)	C(23)	D(23)	RS9 (38)
A(9)	B(9)	C(9)	D(9)	A(24)	B(24)	C(24)	D(24)	RS10 (39)
A(10)	B(10)	C(10)	D(10)	A(25)	B(25)	C(25)	D(25)	RS11 (3A)
A(11)	B(11)	C(11)	D(11)	A(26)	B(26)	C(26)	D(26)	RS12 (3B)
A(12)	B(12)	C(12)	D(12)	A(27)	B(27)	C(27)	D(27)	RS13 (3C)
A(13)	B(13)	C(13)	D(13)	A(28)	B(28)	C(28)	D(28)	RS14 (3D)
A(14)	B(14)	C(14)	D(14)	A(29)	B(29)	C(29)	D(29)	RS15 (3E)
A(15)	B(15)	C(15)	D(15)	A(30)	B(30)	C(30)	D(30)	RS16 (3F)

SYMBOL	POSITION	NAME AND DESCRIPTION
X	RS1.0/1/3	Spare Bits
Y	RS1.2	Remote Alarm Bit (integrated and reported in SR1.6)
A(1)	RS2.7	Signaling Bit A for Channel 1
D(30)	RS16.0	Signaling Bit D for Channel 30

Each Receive Signaling Register (RS1 to RS16) reports the incoming signaling from two timeslots. The bits in the Receive Signaling Registers are updated on multiframe boundaries so the user can utilize the Receive Multiframe Interrupt in the Receive Status Register 2 (SR2.7) to know when to retrieve the signaling bits. The user has a full 2 ms to retrieve the signaling bits before the data is lost. The RS registers are updated under all conditions. Their validity should be qualified by checking for synchronization at the CAS level. In CCS signal-

ing mode, RS1 to RS16 can also be used to extract signaling information. Via the SR2.7 bit, the user will be informed when the signaling registers have been loaded with data. The user has 2 ms to retrieve the data before it is lost.

TS1 TO TS16: TRANSMIT SIGNALING REGISTERS (Address=40 to 4F Hex)

(MSB)							(LSB)	
0	**0**	**0**	**0**	**X**	**Y**	**X**	**X**	TS1 (40)
A(1)	B(1)	C(1)	D(1)	A(31)	B(16)	C(16)	D(16)	TS2 (41)
A(2)	B(2)	C(2)	D(2)	A(32)	B(17)	C(17)	D(17)	TS3 (42)
A(3)	B(3)	C(3)	D(3)	A(33)	B(18)	C(18)	D(18)	TS4 (43)
A(4)	B(4)	C(4)	D(4)	A(34)	B(19)	C(19)	D(19)	TS5 (44)
A(5)	B(5)	C(5)	D(5)	A(35)	B(20)	C(20)	D(20)	TS6 (45)
A(6)	B(6)	C(6)	D(6)	A(36)	B(21)	C(21)	D(21)	TS7 (46)
A(7)	B(7)	C(7)	D(7)	A(37)	B(22)	C(22)	D(22)	TS8 (47)
A(8)	B(8)	C(8)	D(8)	A(38)	B(23)	C(23)	D(23)	TS9 (48)
A(9)	B(9)	C(9)	D(9)	A(39)	B(24)	C(24)	D(24)	TS10 (49)
A(10)	B(10)	C(10)	D(10)	A(40)	B(25)	C(25)	D(25)	TS11 (4A)
A(11)	B(11)	C(11)	D(11)	A(41)	B(26)	C(26)	D(26)	TS12 (4B)
A(12)	B(12)	C(12)	D(12)	A(42)	B(27)	C(27)	D(27)	TS13 (4C)
A(13)	B(13)	C(13)	D(13)	A(43)	B(28)	C(28)	D(28)	TS14 (4D)
A(14)	B(14)	C(14)	D(14)	A(44)	B(29)	C(29)	D(29)	TS15 (4E)
A(15)	B(15)	C(15)	D(15)	A(45)	B(30)	C(30)	D(30)	TS16 (4F)

SYMBOL	POSITION	NAME AND DESCRIPTION
X	TS1.0/1/3	Spare Bits
Y	TS1.2	Remote Alarm Bit
A(1)	TS2.7	Signaling Bit A for Channel 1
D(30)	TS16.0	Signaling Bit D for Channel 30

Each Transmit Signaling Register (TS1 to TS16) contains the CAS bits for two timeslots that will be inserted into the outgoing stream if enabled to do so via TCR1.5. On multiframe boundaries, the DS2153Q will load the values present in the Transmit Signaling Register into an outgoing signaling shift register that is internal to the device. The user can utilize the Transmit Multiframe bit in Status Register 2 (SR2.5) to know when to update the signaling bits. The bit will be set every 2 ms and the user has 2 ms to update the TSR's before the old data will be retransmitted.

The TS1 register is special because it contains the CAS multiframe alignment word in its upper nibble. The upper nibble must always be set to 0000 or else the terminal at the far end will lose multiframe synchronization. If the user wishes to transmit a multiframe alarm to the far end, then the TS1.2 bit should be set to a one. If no alarm is to be transmitted, then the TS1.2 bit should be cleared. The three remaining bits in TS1 are the spare bits. If they are not used, they should be set to one. In CCS signaling mode, TS1 to TS16 can also be used to insert signaling information. Via the SR2.5 bit, the user will be informed when the signaling registers need to be

loaded with data. The user has 2 ms to load the data before the old data will be retransmitted. Via the CCR3.6 bit, the user has the option to use the Transmit Channel Blocking Registers (TCBRs) to determine on a channel by channel basis, which signaling bits are to be inserted via the TSRs (the corresponding bit in the TCBRs=1) and which are to be sourced from the TSER pin (the corresponding bit in the TCBRs=0). See the Transmit Data Flow diagram in Section 13 for more details.

8.0 TRANSMIT IDLE REGISTERS

There is a set of five registers in the DS2153Q that can be used to custom tailor the data that is to be transmitted onto the E1 line, on a channel by channel basis. Each of the 32 E1 channels can be forced to have a user defined idle code inserted into them.

TIR1/TIR2/TIR3/TIR4: TRANSMIT IDLE REGISTERS (Address=26 to 29 Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1 (26)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2 (27)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3 (28)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TIR4 (29)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	TIR4.7	**Transmit Idle Registers**. 0=do not insert the Idle Code into this channel 1=insert the Idle Code into this channel
CH1	TIR1.0	

NOTE:
If CCR3.5=1, then a zero in the TIRs implies that channel data is to be sourced from TSER and a one implies that channel data is to be sourced from the RSER pin.

TIDR: TRANSMIT IDLE DEFINITION REGISTER (Address=2A Hex)

(MSB)							(LSB)
TIDR7	TIDR6	TIDR5	TIDR4	TIDR3	TIDR2	TIDR1	TIDR0

SYMBOL	POSITION	NAME AND DESCRIPTION
TIDR7	TIDR.7	MSB of the Idle Code
TIDR0	TIDR.0	LSB of the Idle Code

Each of the bit positions in the Transmit Idle Registers (TIR1/TIR2/TIR3/TIR4) represent a timeslot in the outgoing frame. When these bits are set to a one, the corresponding channel will transmit the Idle Code contained in the Transmit Idle Definition Register (TIDR). In the TIDR, the MSB is transmitted first. Via the CCR3.5 bit, the user has the option to use the TIRs to determine on a channel by channel basis, if data from the RSER pin should be substituted for data from the TSER pin. In this mode, if the corresponding bit in the TIRs is set to one, then data will be sourced from the RSER pin. If the corresponding bit in the TIRs is set to zero, then data for that channel will sourced from the TSER pin. See the Transmit Data Flow diagram in Section 13 for more details.

9.0 CLOCK BLOCKING REGISTERS

The Receive Channel Blocking Registers (RCBR1/RCBR2/RCBR3/RCBR4) and the Transmit Channel Blocking Registers (TCBR1/TCBR2/TCBR3/TCBR4) control the RCHBLK and TCHBLK pins respectively. The RCHBLK and TCHCLK pins are user programmable outputs that can be forced either high or low during individual channels. These outputs can be used to block clocks to a USART or LAPD controller in ISDN–PRI applications. When the appropriate bits are set to a one, the RCHBLK and TCHCLK pins will be held high during the entire corresponding channel time. See the timing in Section 13 for an example. The TCBRs have alternate mode of use. Via the CCR3.6 bit, the user has the option to use the TCBRs to determine on a channel by channel basis, which signaling bits are to be inserted via the TSRs (the corresponding bit in the TCBRs=1) and which are to be sourced from the TSER pin (the corresponding bit in the TCBR=0). See the Transmit Data Flow diagram in Section 13 for more details.

RCBR1/RCBR2/RCBR3/RCBR4: RECEIVE CHANNEL BLOCKING REGISTERS

(Address=2B to 2E Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCBR1 (2B)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCBR2 (2C)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCBR3 (2D)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	RCBR4 (2E)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	RCBR4.7	**Receive Channel Blocking Registers**. 0=force the RCHBLK pin to remain low during this channel time
CH1	RCBR1.0	1=force the RCHBLK pin high during this channel time

TCBR1/TCBR2/TCBR3/TCBR4: TRANSMIT CHANNEL BLOCKING REGISTERS

(Address=22 to 25 Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCBR1 (22)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCBR2 (23)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCBR3 (24)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TCBR4 (25)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	TCBR4.7	**Transmit Channel Blocking Registers**. 0=force the TCHBLK pin to remain low during this channel time
CH1	TCBR1.0	1=force the TCHBLK pin high during this channel time

NOTE:

If CCR3.6=1, then a zero in the TCBRs implies that signaling data is to be sourced from TSER and a one implies that signaling data for that channel is to be sourced from the Transmit Signaling (TS) registers. See definition below.

TCBR1/TCBR2/TCBR3/TCBR4: DEFINITION WHEN CCR3.6 = 1

(MSB)							(LSB)	
CH20	CH4	CH19	CH3	CH18	CH2	CH17*	CH1*	TCBR1
CH24	CH8	CH23	CH7	CH22	CH6	CH21	CH5	TCBR2
CH28	CH12	CH27	CH11	CH26	CH10	CH25	CH9	TCBR3
CH32	CH16	CH31	CH15	CH30	CH14	CH29	CH13	TCBR4

* = CH1 and CH17 should be set to one to allow the internal TS1 register to create the CAS Multiframe Alignment Word and Spare/Remote Alarm bits.

10.0 ELASTIC STORE OPERATION

The DS2153Q has an onboard two frame (512 bits) elastic store. This elastic store can be enabled via RCR2.1. If the elastic store is enabled (RCR2.1=1), then the user must provide either a 1.544 MHz (RCR2.2=0) or 2.048 MHz (RCR2.2=1) clock at the SYSCLK pin. If the elastic store is enabled, then the user has the option of either providing a frame sync at the RSYNC pin (RCR1.5=1) or having the RSYNC pin provide a pulse on frame or multiframe boundaries (RCR1.5=0). If the user wishes to obtain pulses at the frame boundary, then RCR1.6 must be set to zero and if the user wishes to have pulses occur at the multiframe boundary, then RCR1.6 must be set to one. If the user selects to apply a 1.544 MHz clock to the SYSCLK pin, then every fourth channel will be deleted and the F–bit position inserted (forced to one). Hence channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be deleted. Also, in 1.544 MHz applications, the RCHBLK output will not be active in channels 25 through 32 (or in other words, RCBR4 is not active). See Section 13 for more details. If the 512–bit elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data (256 bits) will be repeated at RSER and the SR1.4 and RIR.3 bits will be set to a one. If the buffer fills, then a full frame of data will be deleted and the SR1.4 and RIR.4 bits will be set to a one.

11.0 ADDITIONAL (Sa) AND INTERNATIONAL (Si) BIT OPERATION

The DS2153Q provides for access to both the Additional (Sa) and International (Si) bits. On the receive side, the RAF and RNAF registers will always report the data as it received in the Additional and International bit locations. The RAF and RNAF registers are updated with the setting of the Receive Align Frame bit in Status Register 2 (SR2.6). The host can use the SR2.6 bit to know when to read the RAF and RNAF registers. It has 250 µs to retrieve the data before it is lost.

On the transmit side, data is sampled from the TAF and TNAF registers with the setting of the Transmit Align Frame bit in Status Register 2 (SR2.3). The host can use the SR2.3 bit to know when to update the TAF and TNAF registers. It has 250 µs to update the data or else the old data will be retransmitted. Data in the Si bit position will be overwritten if either the DS2153Q is programmed: (1) to source the Si bits from the TSER pin, (2) in the CRC4 mode, or (3) have automatic E–bit insertion enabled. Data in the Sa bit position will be overwritten if any of the TCR2.3 to TCR2.7 bits are set to one. Please see the register descriptions for TCR1 and TCR2 and the Transmit Data Flow diagram in Section 13 for more details.

RAF: RECEIVE ALIGN FRAME REGISTER (Address=2F Hex)

(MSB)							(LSB)
Si	0	0	1	1	0	1	1

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	RAF.7	International Bit.
0	RAF.6	Frame Alignment Signal Bit.
0	RAF.5	Frame Alignment Signal Bit.
1	RAF.4	Frame Alignment Signal Bit.
1	RAF.3	Frame Alignment Signal Bit.
0	RAF.2	Frame Alignment Signal Bit.
1	RAF.1	Frame Alignment Signal Bit.
1	RAF.0	Frame Alignment Signal Bit.

RNAF: RECEIVE NON–ALIGN FRAME REGISTER (Address=1F Hex)

(MSB)							(LSB)
Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	RNAF.7	International Bit.
1	RNAF.6	Frame Non–Alignment Signal Bit.
A	RNAF.5	Remote Alarm.
Sa4	RNAF.4	Additional Bit 4.
Sa5	RNAF.3	Additional Bit 5.
Sa6	RNAF.2	Additional Bit 6.
Sa7	RNAF.1	Additional Bit 7.
Sa8	RNAF.0	Additional Bit 8.

TAF: TRANSMIT ALIGN FRAME REGISTER (Address=20 Hex)

(MSB)							(LSB)
Si	0	0	1	1	0	1	1

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	TAF.7	International Bit.
0	TAF.6	Frame Alignment Signal Bit.
0	TAF.5	Frame Alignment Signal Bit.
1	TAF.4	Frame Alignment Signal Bit.

1	TAF.3	Frame Alignment Signal Bit.
0	TAF.2	Frame Alignment Signal Bit.
1	TAF.1	Frame Alignment Signal Bit.
1	TAF.0	Frame Alignment Signal Bit.

TNAF: TRANSMIT NON–ALIGN FRAME REGISTER (Address=21 Hex)

(MSB)							(LSB)
Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	TNAF.7	International Bit.
1	TNAF.6	Frame Non–Alignment Signal Bit.
A	TNAF.5	Remote Alarm.
Sa4	TNAF.4	Additional Bit 4.
Sa5	TNAF.3	Additional Bit 5.
Sa6	TNAF.2	Additional Bit 6.
Sa7	TNAF.1	Additional Bit 7.
Sa8	TNAF.0	Additional Bit 8.

12.0 LINE INTERFACE FUNCTIONS

The line interface function in the DS2153Q contains three sections; (1) the receiver which handles clock and data recovery, (2) the transmitter which waveshapes and drives the E1 line, and (3) the jitter attenuator. Each of the these three sections is controlled by the Line Interface Control Register (LICR) which is described below.

LICR: LINE INTERFACE CONTROL REGISTER (Address=18 Hex)

(MSB)							(LSB)	
L2	L1	L0	EGL	JAS	JABDS	DJA	TPD	LICR

SYMBOL	POSITION	NAME AND DESCRIPTION
LB2	LICR.7	**Line Build Out Bit 2**. Transmit waveshape setting; see Table 12.2.
LB1	LICR.6	**Line Build Out Bit 1**. Transmit waveshape setting; see Table 12.2.
LB0	LICR.5	**Line Build Out Bit 0**. Transmit waveshape setting; see Table 12.2.
EGL	LICR.4	**Receive Equalizer Gain Limit**. 0 = –12 dB 1 = –30 dB
JAS	LICR.3	**Jitter Attenuator Select**. 0=place the jitter attenuator on the receive side 1=place the jitter attenuator on the transmit side
JABDS	LICR.2	**Jitter Attenuator Buffer Depth Select** . 0=128 bits 1=32 bits (use for delay sensitive applications)

DJA	LICR.1	**Disable Jitter Attenuator**. 0=jitter attenuator enabled 1=jitter attenuator disabled
TPD	LICR.0	**Transmit Power Down**. 0=normal transmitter operation 1=powers down the transmitter and 3–states the TTIP and TRING pins

12.1 Receive Clock and Data Recovery

The DS2153Q contains a digital clock recovery system. See the DS2153Q Block Diagram in Section 1 and Figure 12.1 for more details. The DS2153Q couples to the receive E1 shielded twisted pair or COAX via a 1:1 transformer. See Table 12.3 for transformer details. The DS2153Q automatically adjusts to the E1 signal being received at the RTIP and RRING pins and can handle E1 twisted pair cables of 0.6 mm (22 AWG) from 0 to 1.5 KM in length. The crystal attached at the XTAL1 and XTAL2 pins is multiplied by four via an internal PLL and fed to the clock recovery system. The clock recovery system uses both edges of the clock from the PLL circuit to form a 32 times oversampler which is used to recover the clock and data. This oversampling technique offers outstanding jitter tolerance (see Figure 12.2).

Normally, the clock that is output at the RCLK pin is the recovered clock from the E1 AMI/HDB3 waveform presented at the RTIP and RRING inputs. When no AMI signal is present at RTIP and RRING, a Receive Carrier Loss (RCL) condition will occur and the RCLK can be sourced from either the ACLKI pin or from the crystal attached to the XTAL1 and XTAL2 pins. The DS2153Q will sense the ACLKI pin to determine if a clock is present. If no clock is applied to the ACLKI pin, then it should be tied to RVSS to prevent the device from falsely sensing a clock. See Table 12.1. If the jitter attenuator is either placed in the transmit path or is disabled, the RCLK output can exhibit short high cycles of the clock. This is due to the highly oversampled digital clock recovery circuitry. If the jitter attenuator is placed in the receive path (as is the case in most applications), the jitter attenuator restores the RCLK to being close to 50% duty cycle. Please see the Receive AC Timing Characteristics in Section 14 for more details.

SOURCE OF RCLK UPON RCL Table 12–1

ACLKI PRESENT?	RECEIVE SIDE JITTER ATTENUATOR	TRANSMIT SIDE JITTER ATTENUATOR
yes	ACLKI via the jitter attenuator	ACLKI
no	centered crystal	TCLK via the jitter attenuator

12.2 Transmit Waveshaping and Line Driving

The DS2153Q uses a set of laser–trimmed delay lines along with a precision Digital–to–Analog Converter (DAC) to create the waveforms that are transmitted onto the E1 line. The waveforms created by the DS2153Q meet the ITU specifications. See Figure 12.3. The user will select which waveform is to be generated by properly programming the L2/L1/L0 bits in the Line Interface Control Register (LICR). The DS2153Q can set set up in a number of various configurations depending on the application. See Table 12.2 and Figure 12.1.

LINE BUILD OUT SELECT IN LICR Table 12–2

L2	L1	L0	APPLICATION	TRANSFORMER	RETURN LOSS	Rt
0	0	0	75 ohm normal	1:1.15 step–up	NM	0 ohms
0	0	1	120 ohm normal	1:1.15 step–up	NM	0 ohms
0	1	0	75 ohm normal with protection resistors	1:1.15 step–up	NM	8.2 ohms
0	1	1	120 ohm normal with protection resistors	1:1.15 step–up	NM	8.2 ohms
1	0	0	75 ohm with high return loss	1:1.15 step–up	21 dB	27 ohms
1	1	0	75 ohm with high return loss	1:1.36 step–up	21 dB	18 ohms
1	0	0	120 ohm with high return loss	1:1.36 step–up	21 dB	27 ohms

NM=Not Meaningful

Due to the nature of the design of the transmitter in the DS2153Q, very little jitter (less then 0.00 5UIpp broadband from 10 Hz to 100 KHz) is added to the jitter present on TCLK. Also, the waveforms that they create are independent of the duty cycle of TCLK. The transmitter in the DS2153Q couples to the E1 transmit shielded twisted pair or COAX via a 1:1.15 or 1:1.36 step up transformer as shown in Figure 12.1. In order for the devices to create the proper waveforms, this transformer used must meet the specifications listed in Table 12.3.

TRANSFORMER SPECIFICATIONS Table 12–3

SPECIFICATION	RECOMMENDED VALUE
Turns Ratio	1:1 (receive) and 1:1.15 or 1:1.36 (transmit) ±5%
Primary Inductance	600 µH minimum
Leakage Inductance	1.0 µH maximum
Interwinding Capacitance	60 pF maximum
DC Resistance	1.2 ohms maximum

12.3 Jitter Attenuator

The DS2153Q contains an onboard jitter attenuator that can be set to a depth of either 32 or 128 bits via the JABDS bit in the Line Interface Control Register (LICR). The 128–bit mode is used in applications where large excursions of wander are expected. The 32–bit mode is used in delay sensitive applications. The characteristics of the attenuation are shown in Figure 12.4. The jitter attenuator can be placed in either the receive path or the transmit path by appropriately setting or clearing the JAS bit in the LICR. Also, the jitter attenuator can be disabled (in effect, removed) by setting the DJA bit in the LICR. In order for the jitter attenuator to operate properly, a crystal with the specifications listed in Table 12.4 below must be connected to the XTAL1 and XTAL2 pins.

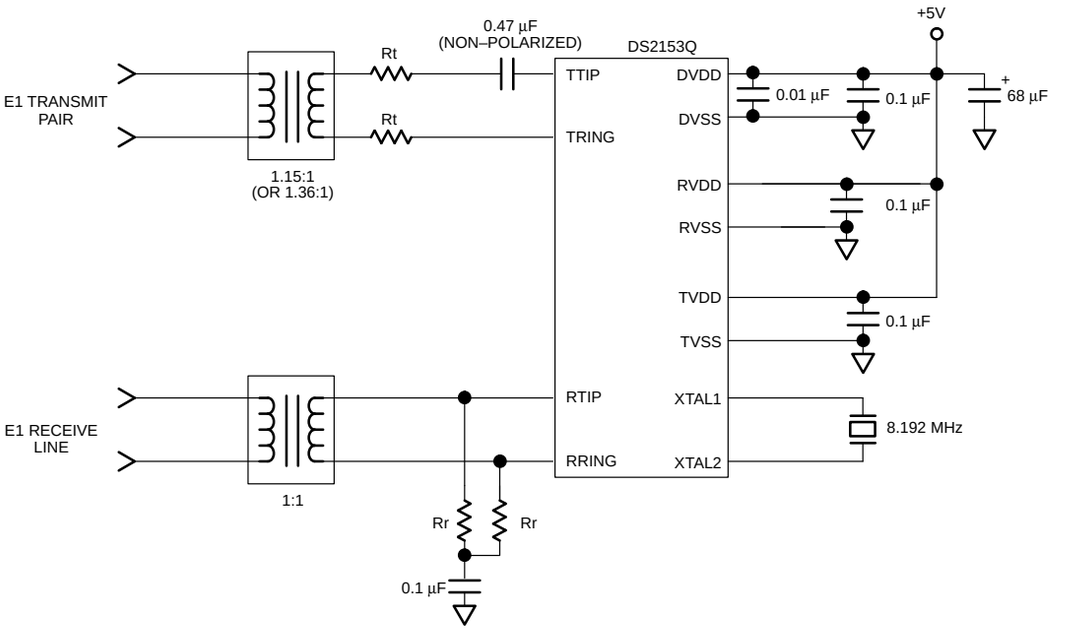
The jitter attenuator divides the clock provided by the 8.192 MHz crystal at the XTAL1 and XTAL2 pins by to create an output clock that contains very little jitter. Onboard circuitry will pull the crystal (by switching in or out load capacitance) to keep it long term averaged to the same frequency as the incoming E1 signal. If the incoming jitter exceeds either 120 UIpp (buffer depth is 128–bits) or 28 UIpp (buffer depth is 32–bits), then the

DS2153Q will divide the attached crystal by either 3.5 or 4.5 instead of the normal 4 to keep the buffer from overflowing. When the device divides by either 3.5 or 4.5, it also sets the Jitter Attenuator Limit Trip (JALT) bit in the Receive Information Register (RIR.5).

CRYSTAL SELECTION GUIDELINES Table 12–4

PARAMETER	SPECIFICATION
Parallel Resonant Frequency	8.192 MHz
Mode	Fundamental
Load Capacitance	18 pF to 20 pF (18.5 pF nominal)
Tolerance	±50 ppm
Pullability	CL=10 pF, delta frequency=+175 to +250 ppm CL=45 pF, delta frequency=–175 to –250 ppm
Effective Series Resistance	30 ohms maximum
Crystal Cut	AT

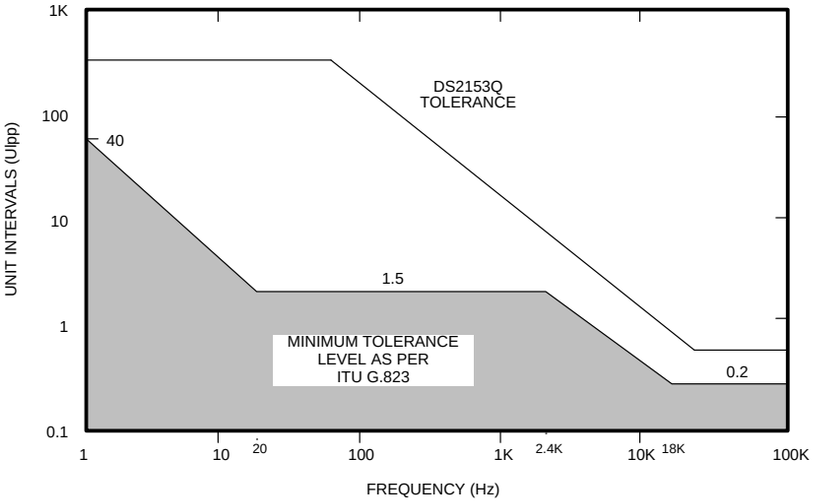
DS2153Q EXTERNAL ANALOG CONNECTIONS Figure 12–1



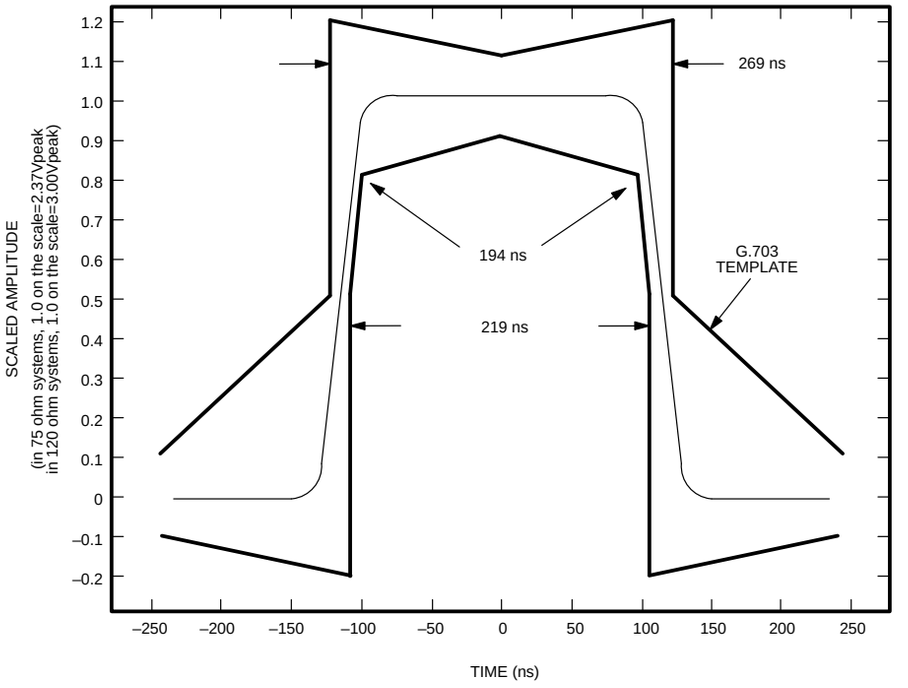
NOTES:

1. All resistor values are ±1%.
2. The Rt resistors are used to increase the transmitter return loss or to protect the device from over–voltage.
3. The Rr resistors are used to terminate the receive E1 line.
4. For 75 ohm termination, Rr=37.5 ohms/for 120 ohm termination Rr=60 ohms.
5. See the separate Application Note for details on how to construct a protected interface.

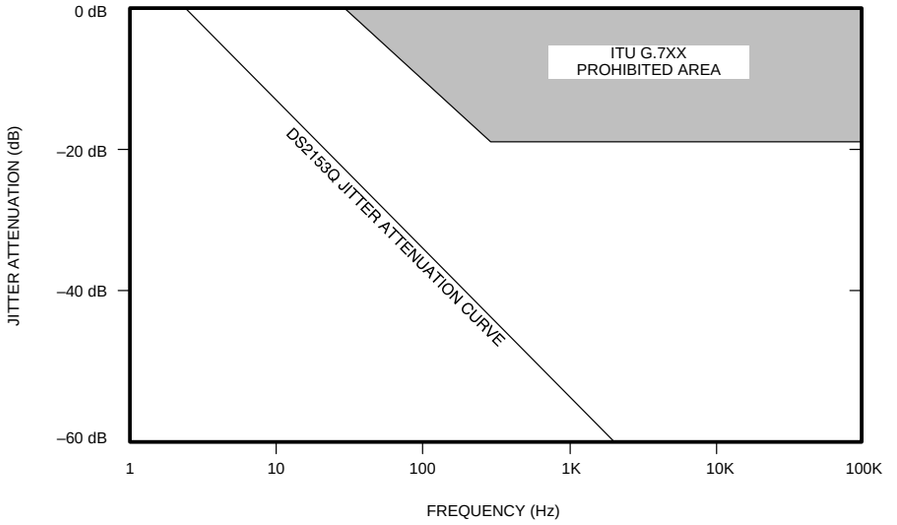
DS2153Q JITTER TOLERANCE Figure 12–2



DS2153Q TRANSMIT WAVEFORM TEMPLATE Figure 12–3

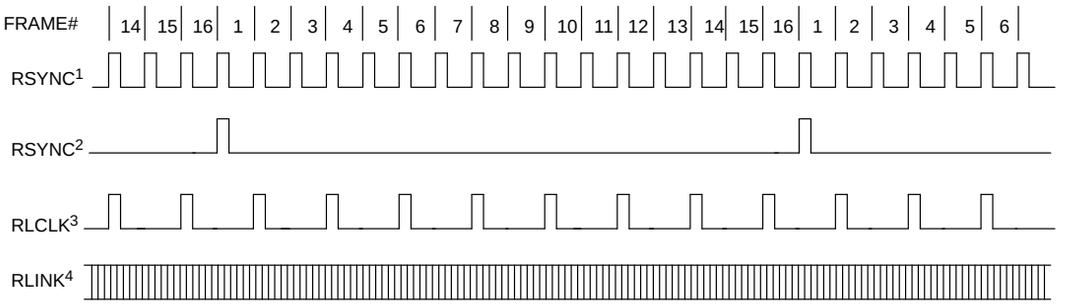


DS2153Q JITTER ATTENUATION Figure 12–4



13.0 TIMING DIAGRAMS/SYNCHRONIZATION FLOWCHART/TRANSMIT DATA FLOW DIAGRAM

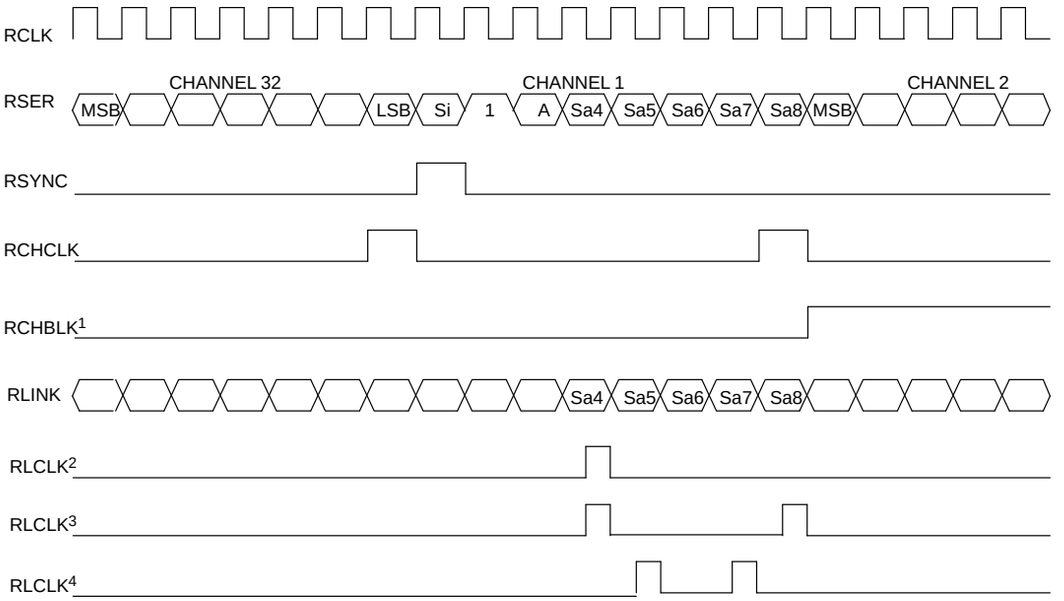
RECEIVE SIDE TIMING Figure 13–1



NOTES:

1. RSYNC in the frame mode (RCR1.6=0).
2. RSYNC in the multiframe mode (RCR1.6=1).
3. RLCLK is programmed to output just the Sa4 bit.
4. RLINK will always output all five Sa bits as well as the rest of the receive data stream.
5. This diagram assumes the CAS MF begins with the FAS word.

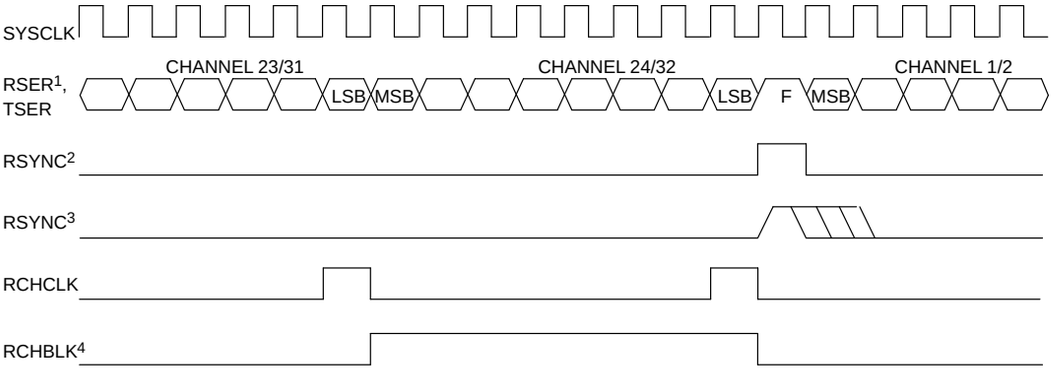
RECEIVE SIDE BOUNDARY TIMING (WITH ELASTIC STORES DISABLED) Figure 13–2



NOTES:

1. RCHBLK is programmed to block channel 2.
2. RLINK is programmed to output the Sa4 bits.
3. RLINK is programmed to output the SA4 and SA8 bits.
4. RLINK is programmed to output the Sa5 and Sa7 bits.
5. Shown is a non–align frame boundary.

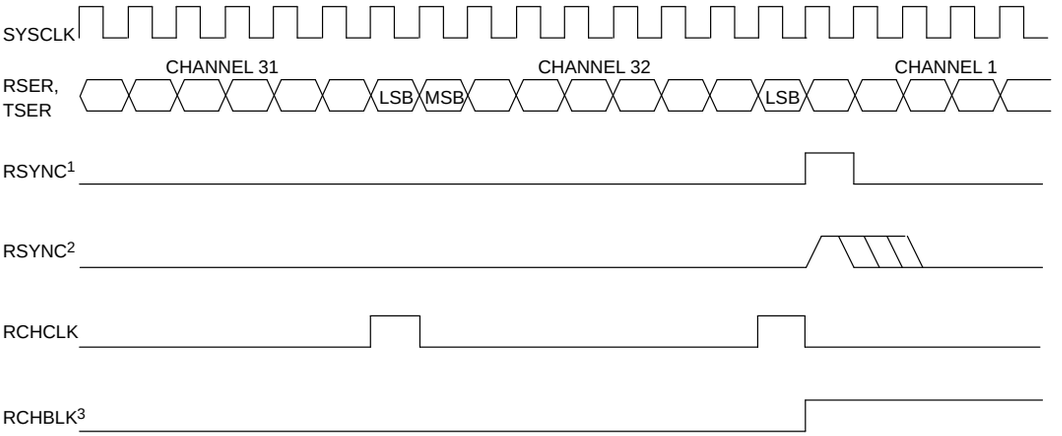
1.544 MHz BOUNDARY TIMING WITH ELASTIC STORE(S) ENABLED Figure 13–3



NOTES:

1. Data from the E1 channels 1, 5, 9, 13, 17, 21, 25, and 29 is dropped (channel 2 from the E1 link is mapped to channel 1 of the T1 link, etc.) and the F–bit position is added (forced to one).
2. RSYNC is in the output mode (RCR1.5=0).
3. RSYNC is in the input mode (RCR1.5=1).
4. RCHBLK is programmed to block channel 24.

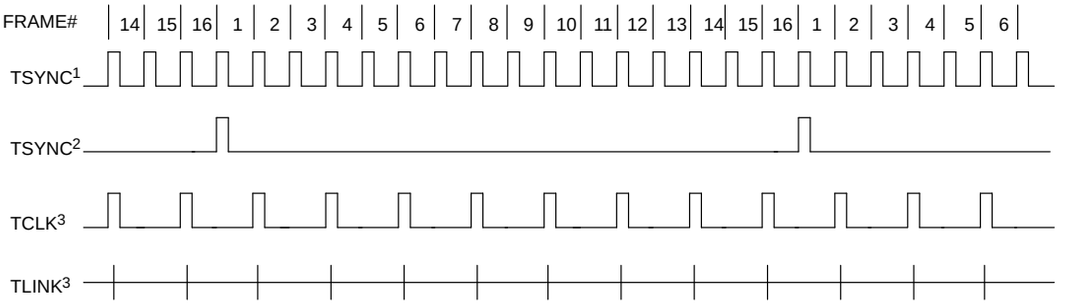
2.048 MHz BOUNDARY TIMING WITH ELASTIC STORE(S) ENABLED Figure 13–4



NOTES:

1. RSYNC is in the output mode (RCR1.5=0).
2. RSYNC is in the input mode (RCR1.5=1).
3. RCHBLK is programmed to block channel 1.

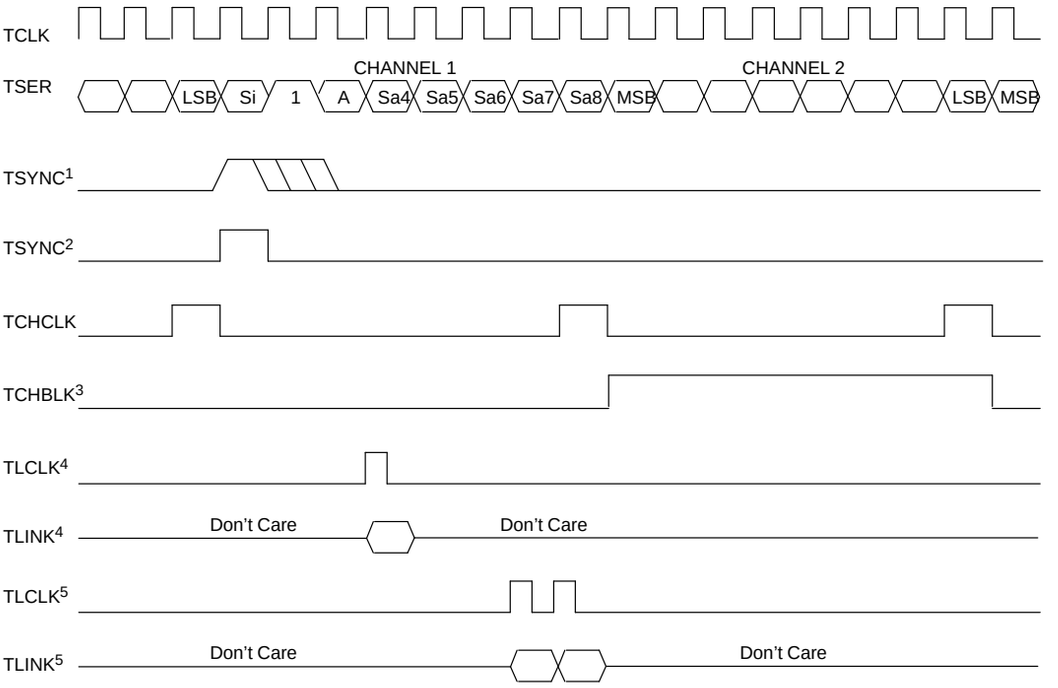
TRANSMIT SIDE TIMING Figure 13–5



NOTES:

1. TSYNC in the frame mode (TCR1.1=0).
2. TSYNC in the multiframe mode (TCR1.1=1).
3. TLINK is programmed to source only the Sa4 bit.
4. This diagram assembles both the CAS MF and the CRC4 begin with the align frame.

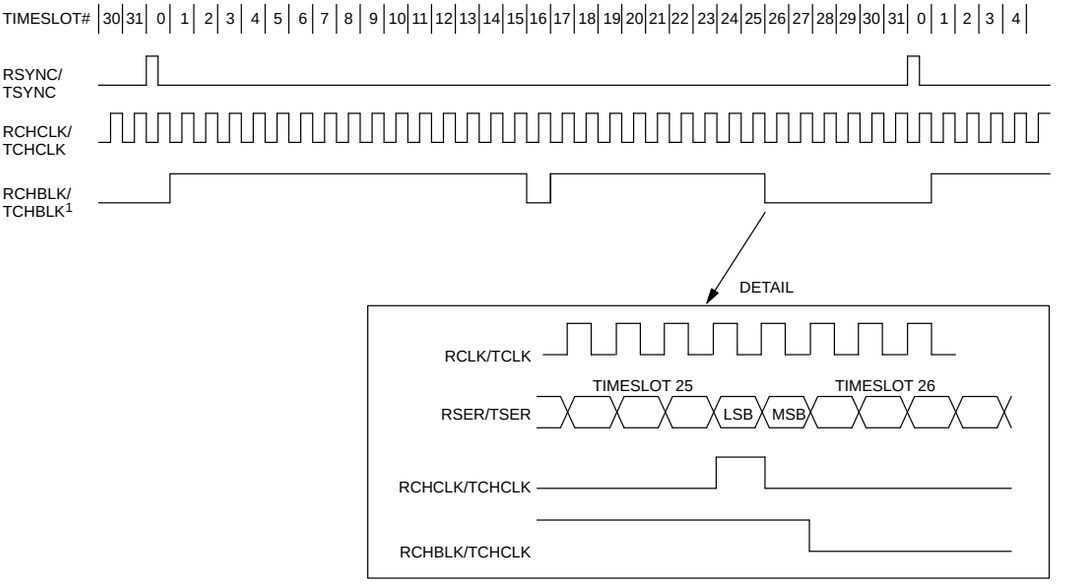
TRANSMIT SIDE BOUNDARY TIMING Figure 13–6



NOTES:

1. TSYNC is in the input mode (TCR1.0=0).
2. TSYNC is in the output mode (TCR1.0=1).
3. TCHBLK is programmed to block channel 2.
4. TLINK is programmed to source the Sa4 bits.
5. TLINK is programmed to source the Sa7 and Sa8 bits.
6. Shown is a non–align frame boundary.
7. See Figures 13.3 and 13.4 for details on timing with the transmit side elastic store enabled.

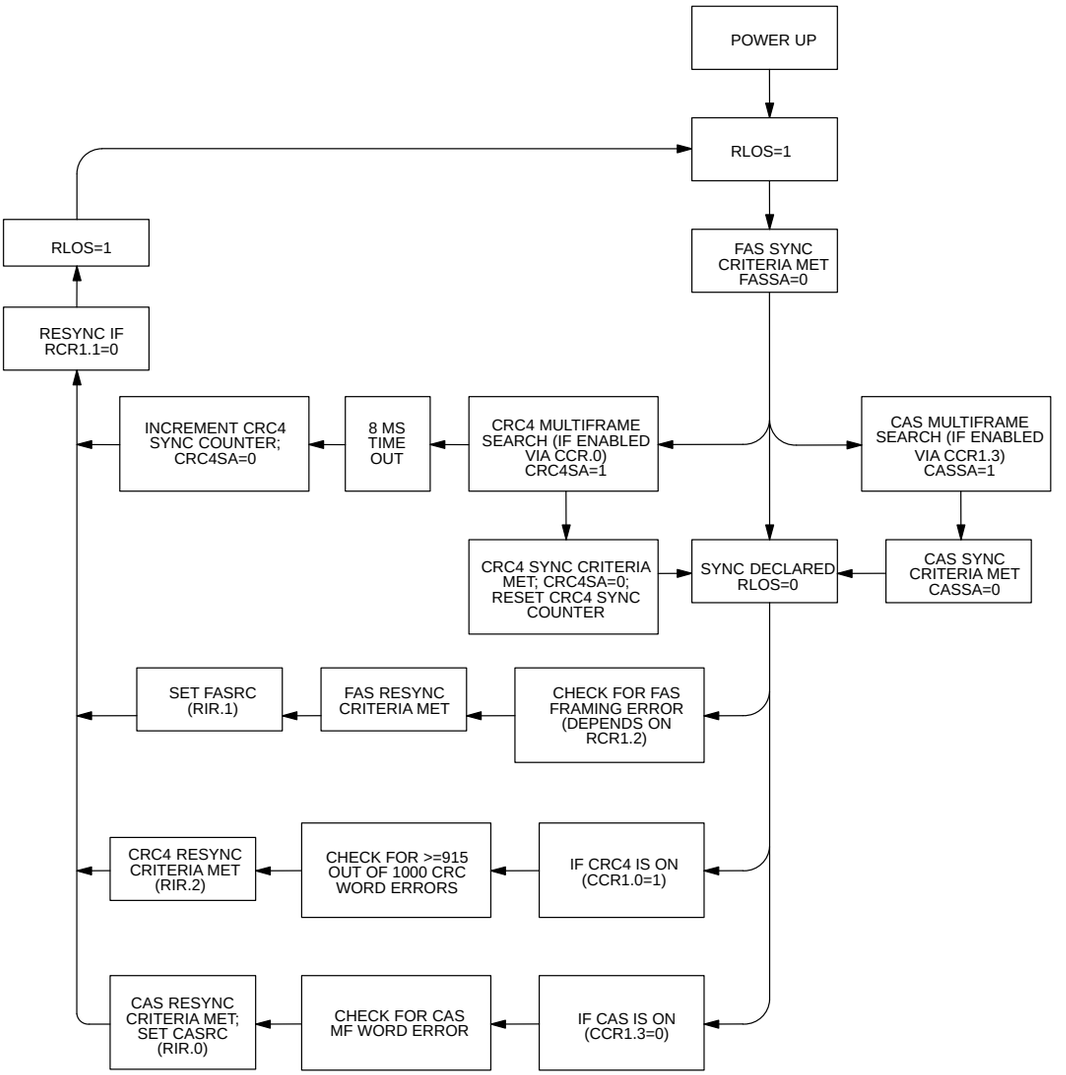
G.802 TIMING Figure 13–7



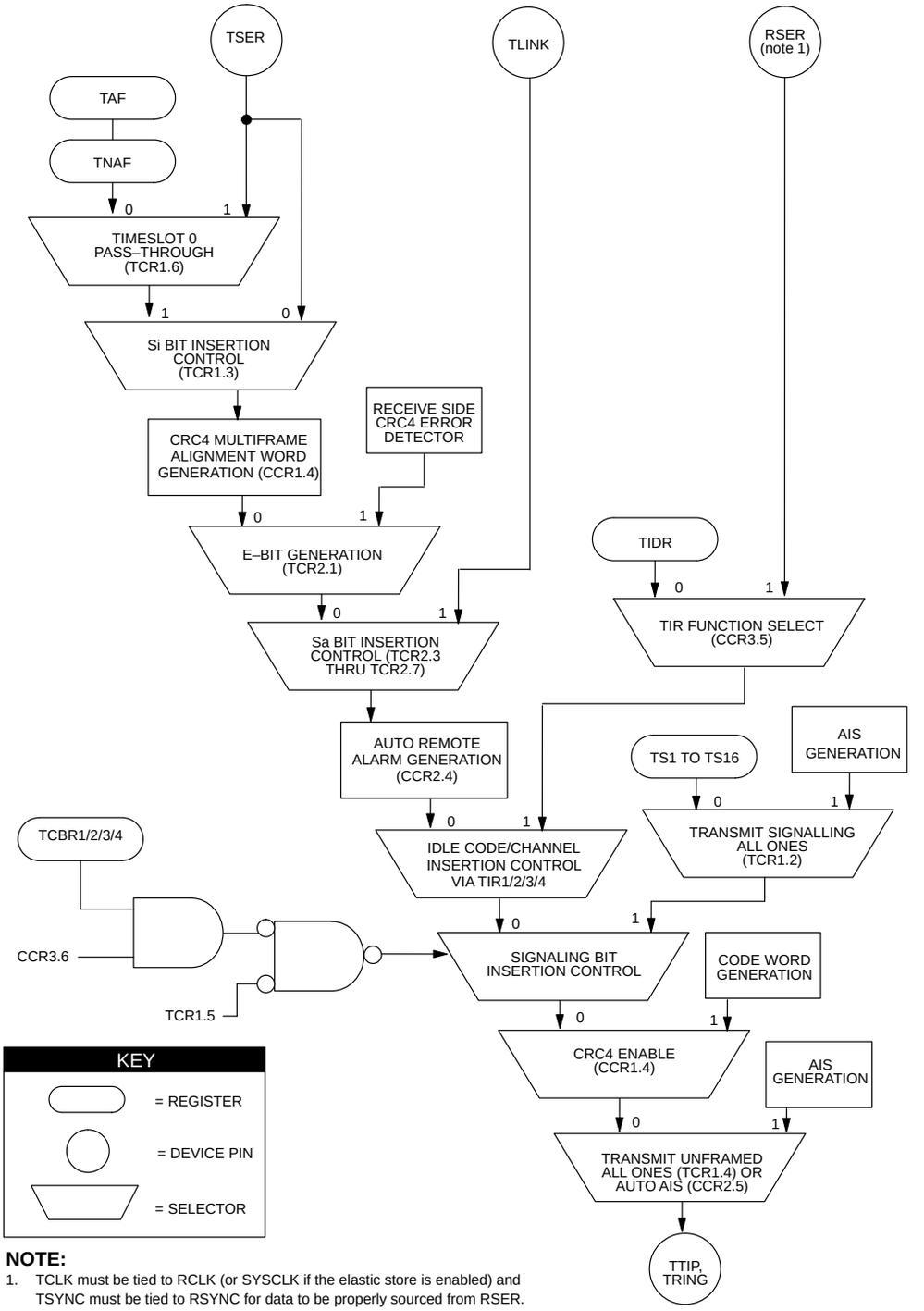
NOTE:

1. RCHBLK or TCHBLK is programmed to pulse high during timeslots 1 to 15, 17 to 25, and during bit 1 of timeslot 26.

DS2153Q SYNCHRONIZATION FLOWCHART Figure 13–8



DS2153Q TRANSMIT DATA FLOW Figure 13–9



NOTE:

1. TCLK must be tied to RCLK (or SYSCLK if the elastic store is enabled) and TSYNC must be tied to RSYNC for data to be properly sourced from RSER.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +7.0V
Operating Temperature	0°C to 70°C (–40°C to +85°C for DS2153QN)
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATION CONDITIONS

(0°C to 70°C)
(–40°C to +85°C for DS2153QN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{DD} +0.3	V	
Logic 0	V_{IL}	–0.3		+0.8	V	
Supply for DS2153Q	V_{DD}	4.75		5.25	V	1
Supply for DS2153QN	V_{DD}	4.80		5.25	V	1

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

DC CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V ± 5%)
(–40°C to +85°C; V_{DD}=5V +5%/–4% for DS2153QN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current @ 5V	I_{DD}		60		mA	2
Input Leakage	I_{IL}	–1.0		+1.0	µA	3
Output Leakage	I_{LO}			1.0	µA	4
Output Current (2.4V)	I_{OH}	–1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

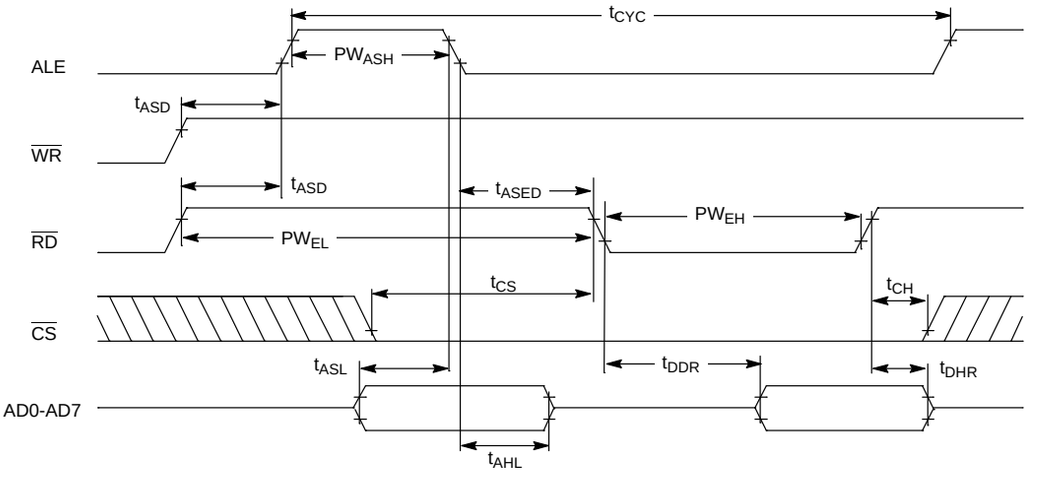
1. Applies to RVDD, TVDD, and DVDD.
2. TCLK=2.048 MHz.
3. $0.0V < V_{IN} < V_{DD}$.
4. Applies to $\overline{INT1}$ and $\overline{INT2}$ when 3–stated.

AC CHARACTERISTICS – PARALLEL PORT

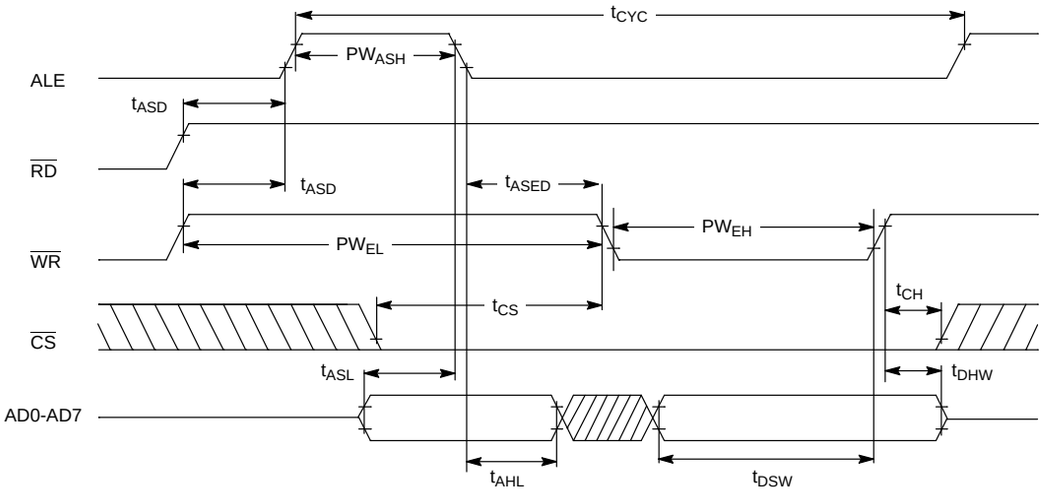
(0°C to 70°C; V_{DD}=5V ± 5%)
(–40°C to +85°C; V_{DD}=5V +5%/–4% for DS2153QN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	250			ns	
Pulse Width, DS Low or $\overline{RD}$ High	PW_{EL}	150			ns	
Pulse Width, DS High or $\overline{RD}$ Low	PW_{EH}	100			ns	
Input Rise/Fall Times	t_R, t_F			30	ns	
R/$\overline{W}$ Hold Time	t_{RWH}	10			ns	
R/$\overline{W}$ Setup Time Before DS High	t_{RWS}	50			ns	
$\overline{CS}$ Setup Time Before DS, $\overline{WR}$ or $\overline{RD}$ active	t_{CS}	20			ns	
$\overline{CS}$ Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		50	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid to AS or ALE fall	t_{ASL}	20			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time DS, $\overline{WR}$ or $\overline{RD}$ to AS or ALE Rise	t_{ASD}	25			ns	
Pulse Width AS or ALE High	PW_{ASH}	40			ns	
Delay Time, AS or ALE to DS, $\overline{WR}$ or $\overline{RD}$	t_{ASED}	20			ns	
Output Data Delay Time from DS or $\overline{RD}$	t_{DDR}	20		100	ns	
Data Setup Time	t_{DSW}	80			ns	

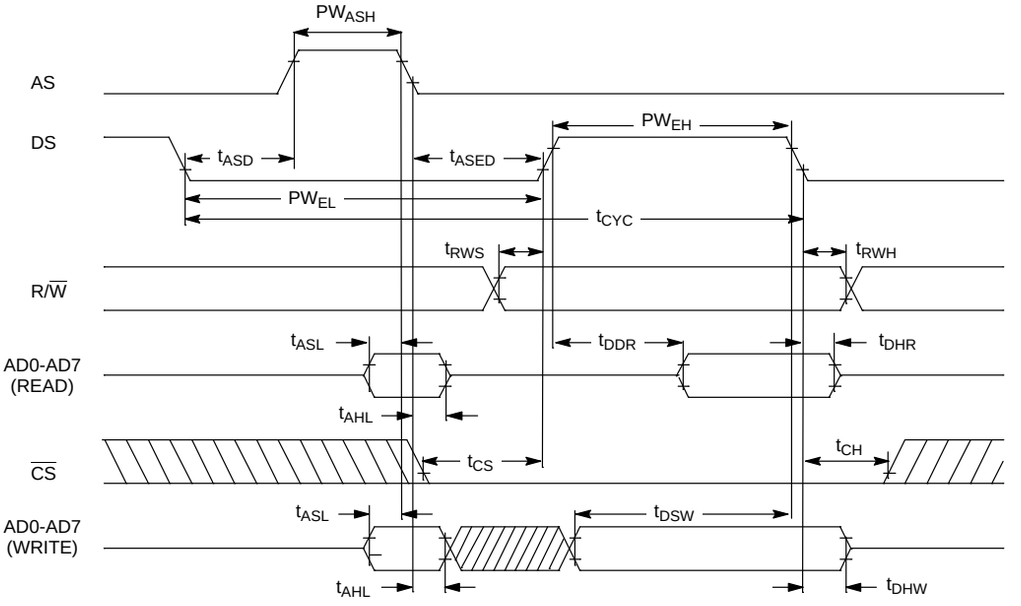
INTEL READ BUS AC TIMING Figure 14–1



INTEL WRITE BUS AC TIMING Figure 14–2



MOTOROLA BUS AC TIMING Figure 14–3



AC CHARACTERISTICS – RECEIVE SIDE

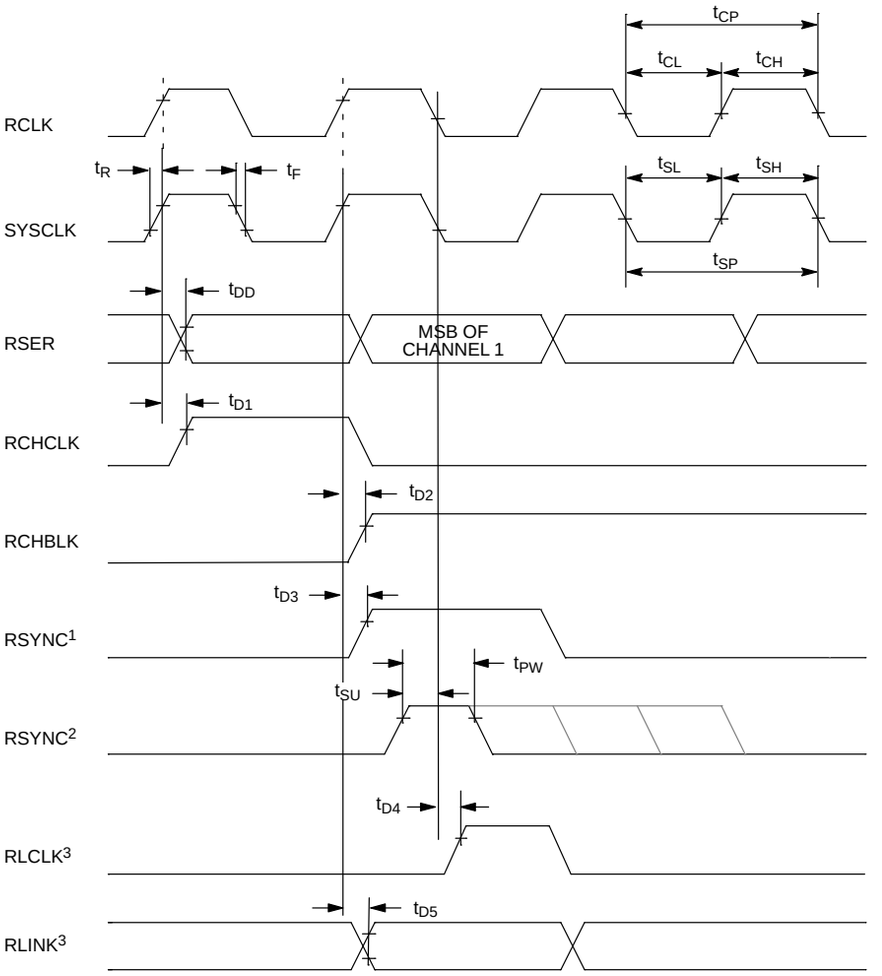
(0°C to 70°C; V_{DD}=5V ± 5%)
(–40°C to +85°C; V_{DD}=5V +5%/–4% for DS2153QN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
ALCKI/RCLK Period	t_{CP}		488		ns	
RCLK Pulse Width	t_{CH} t_{CL}	180 180	244 244		ns ns	1
RCLK Pulse Width	t_{CH} t_{CL}	90 200	244 244		ns ns	2
SYSCLK Period	t_{SP} t_{SP}		648 488		ns ns	3 4
SYSCLK Pulse Width	t_{SH} t_{SL}	50 50			ns	
RSYNC Set Up to SYSCLK Falling	t_{SU}	25		t_{SH}–5	ns	
RSYNC Pulse Width	t_{PW}	50			ns	
SYSCLK Rise/Fall Times	t_R, t_F			25	ns	
Delay RCLK or SYSCLK to RSER Valid	t_{DD}			70	ns	
Delay RCLK or SYSCLK to RCHCLK	t_{D1}			50	ns	
Delay RCLK or SYSCLK to RCHBLK	t_{D2}			50	ns	
Delay RCLK or SYSCLK to RSYNC	t_{D3}			50	ns	
Delay RCLK to RLCLK	t_{D4}			50	ns	
Delay RCLK to RLINK Valid	t_{D5}			50	ns	

NOTES:

1. Jitter attenuator enabled in the receive side path.
2. Jitter attenuator disabled or enabled in the transmit path.
3. SYSCLK=1.544 MHz.
4. SYSCLK=2.048 MHz.

RECEIVE SIDE AC TIMING Figure 14–4



NOTES:

1. RSYNC is in the output mode (RCR1.5=0).
2. RSYNC is in the input mode (RCR1.5=1).
3. RLCLK and RLINK only have a timing relationship to RCLK; no timing relationship between RLCLK/RLINK and RSYNC is implied.
4. RCLK can exhibit a short high time if the jitter attenuator is either disabled or in the transmit path.

AC CHARACTERISTICS – TRANSMIT SIDE

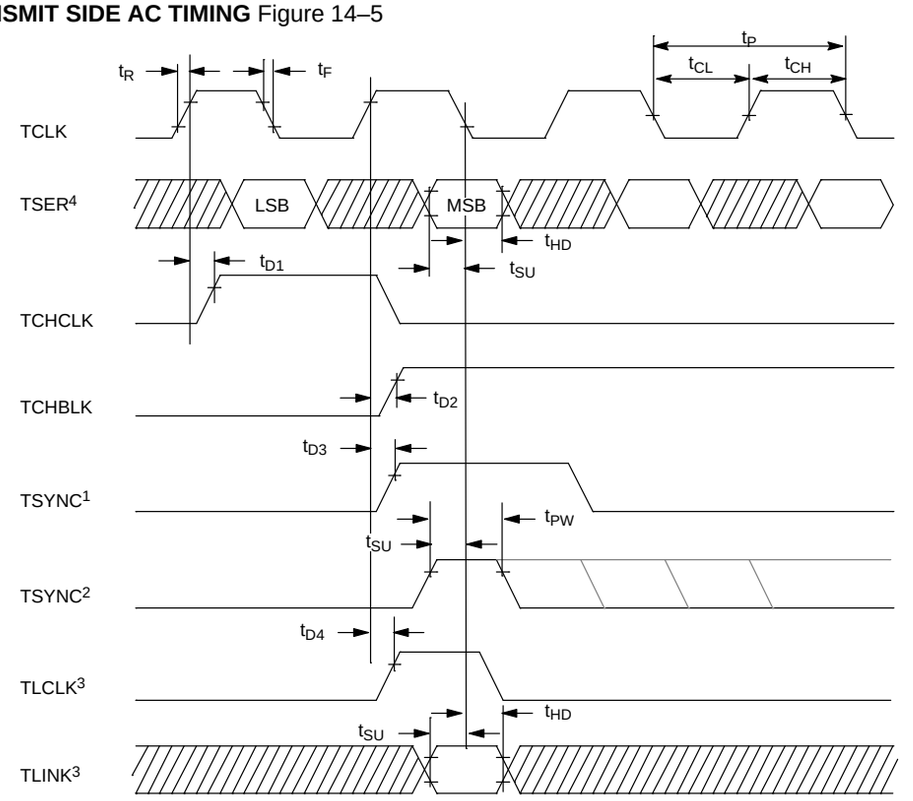
(0°C to 70°C; V_{DD}=5V ± 5%)
(–40°C to +85°C; V_{DD}=5V +5%/–4% for DS2153QN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_P		488		ns	
TCLK Pulse Width	t_{CH} t_{CL}	75 75			ns ns	
TSER, TLINK Set Up to TCLK Falling	t_{SU}	25			ns	1
TSER, TLINK Hold from TCLK Falling	t_{HD}	25			ns	1
TSYNC Setup to TCLK Falling	t_{HD}	25		t_{CH}–5	ns	
TSYNC Pulse Width	t_{PW}	25			ns	
TCLK Rise/Fall Times	t_R, t_F			25	ns	
Delay TCLK to TCHCLK	t_{D1}			50	ns	
Delay TCLK to TCHBLK	t_{D2}			50	ns	
Delay TCLK to TSYNC	t_{D3}			50	ns	
Delay TCLK to TLCLK	t_{D4}			50	ns	

NOTES:

1. If the transmit side elastic store is enabled,then TSER is sampled on the falling edge of SYSCLK and the parameters t_{SU} and t_{HD} still apply.

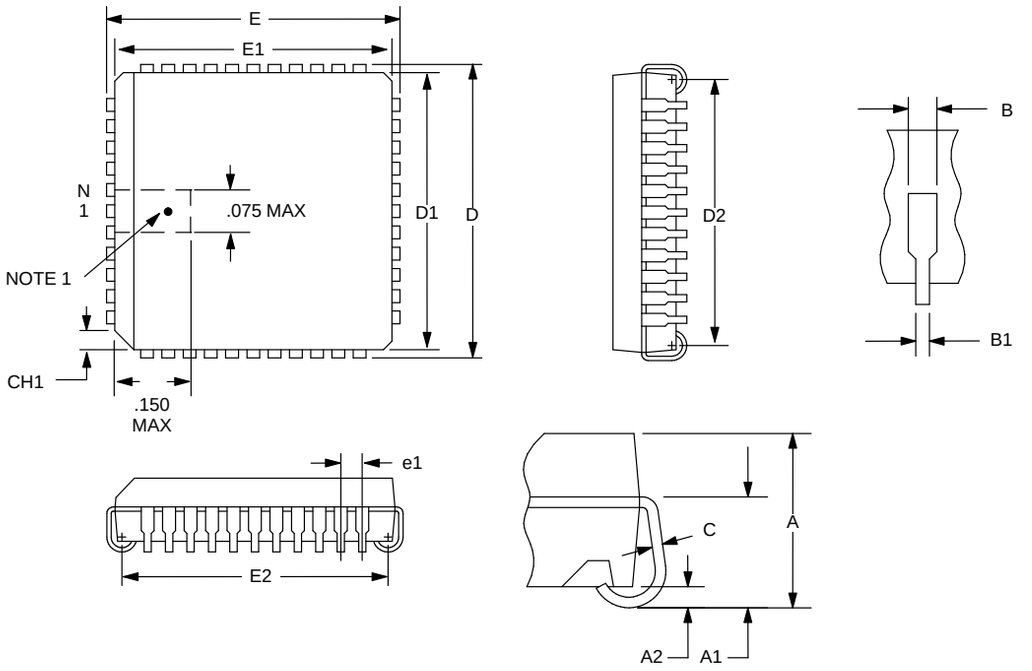
TRANSMIT SIDE AC TIMING Figure 14–5



NOTES:

1. TSYNC is in the output mode (TCR1.0=1).
2. TSYNC is in the input mode (TCR1.0=0).
3. No timing relationship between TSYNC and TLCLK/TLINK is implied.
4. TSER is sampled on the falling edge of SYSCLK if the transmit side elastic store is enabled.

DS2153Q E1 SINGLE–CHIP TRANSCEIVER 44–PIN PLCC



NOTE1: PIN 1 IDENTIFIER TO BE LOCATED IN ZONE INDICATED.

DIM	INCHES	
	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	–
B	0.026	0.033
B1	0.013	0.021
C	0.009	0.012
CH1	0.042	0.048
D	0.685	0.695
D1	0.650	0.656
D2	0.590	0.630
E	0.685	0.695
E1	0.650	0.656
E2	0.590	0.630
e1	0.050 BSC	
N	44	–