DS2120A
Ultra3 LVD SCSI Terminator

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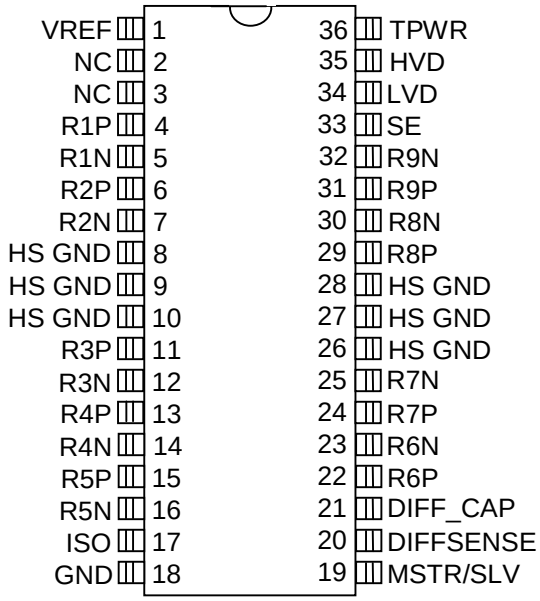
FEATURES

- Fully compliant with Ultra2, Ultra3, and Ultra 160 *LVD-only* SCSI
- Provides Low Voltage Differential termination for 9 signal line pairs
- Auto-selection of LVD termination
- 5% tolerance on LVD termination resistance
- Low power down capacitance of 3 pF
- Onboard thermal shutdown circuitry
- SCSI bus hot plug compatible

PIN ASSIGNMENT



DS2120AB 36-Pin SSOP

DESCRIPTION

The DS2120A Ultra3 LVD SCSI Terminator is a Low Voltage Differential (LVD) terminator. If the device is connected in an LVD-only bus, the DS2120A will use LVD termination. If any single-ended (SE) or high-voltage differential (HVD) devices are connected to the bus, the DS2120A will isolate itself from the SCSI bus. This is accomplished automatically inside the part by sensing the voltage on the SCSI bus DIFFSENS line.

For the LVD termination, the DS2120A integrates two current sources with nine precision resistor strings. Three DS2120A terminators are needed for a wide SCSI bus.

REFERENCE DOCUMENTS

Small Computer Systems Interface (SCSI-3) SCSI Parallel Interface (SPI) Project: 0855-M, 1995
Small Computer Systems Interface (SCSI-3) SCSI Parallel Interface 2 (SPI-2) Project: 1142-M, 1998
Small Computer Systems Interface (SCSI-3) SCSI Parallel Interface 3 (SPI-3) Project: 1302-D, 1999
Small Computer Systems Interface (SCSI-3) SCSI Parallel Interface 4 (SPI-4) Project: 1365-D, *xxxx*

Available from:
American National Standards Institute (ANSI) Phone: (212) 642-4900
Global Engineering Documents 15 Inverness Way East; Englewood, CO 80112 Phone: (800) 854-7179

FUNCTIONAL DESCRIPTION

The DS2120A combines LVD termination with DIFFSENSE sourcing and detection.

A bandgap reference is fed into two amplifiers, which creates a 1.25V reference voltage.

The DIFFSENSE circuitry decodes trinary logic. There will be one of three voltages on the SCSI control line called DIFFSENS. Two comparators and a NAND gate determine if the voltage is below 0.6V, above 2.15V, or in between. That indicates the mode of the bus to be HVD, SE, or LVD, respectively.

The DS2120A's DIFF_CAP pin monitors the DIFFSENS line to determine the proper operating mode of the device; this mode is indicated by the SE/LVD/HVD outputs. The DIFFSENSE pin can also drive the SCSI DIFFSENS line (when MSTR/SLV = 1) to determine the SCSI bus operating mode. The DS2120A switches to the termination mode that is appropriate for the bus based on the value of the DIFFSENS voltage. These modes are:

LVD mode LVD termination is provided by a precision laser trimmed resistor string with two current sources. This configuration yields a 105Ω differential and 150Ω common mode impedance. A fail-safe bias of 112 mV is maintained when no drivers are connected to the SCSI bus.

SE mode The DS2120A identifies that there is a SE (single-ended) device on the SCSI bus and isolates the termination pins from the bus.

HVD Isolation Mode The DS2120A identifies that there is an HVD (high voltage differential) device on the SCSI bus and isolates the termination pins from the bus.

When ISO is pulled high, the termination pins are isolated from the SCSI bus, and the bus mode indicators (SE/LVD/HVD) as well as Vref remains active. During thermal shutdown, the termination pins are isolated from the SCSI bus and Vref becomes high impedance. The DIFFSENSE driver is shut down during either of these two events.

To ensure proper operation, the TPWR pin should be connected to the SCSI bus TERMPWR line. As with all analog circuitry, the TERMPWR and VDD lines should be bypassed locally. A 2.2 µF capacitor and a 0.01 µF high frequency capacitor is recommended between TPWR and ground and placed as close as possible to the DS2120A. The DS2120A should be placed as close as possible to the SCSI connector to minimize signal and power trace length, thereby resulting in less input capacitance and reflections which can degrade the bus signals.

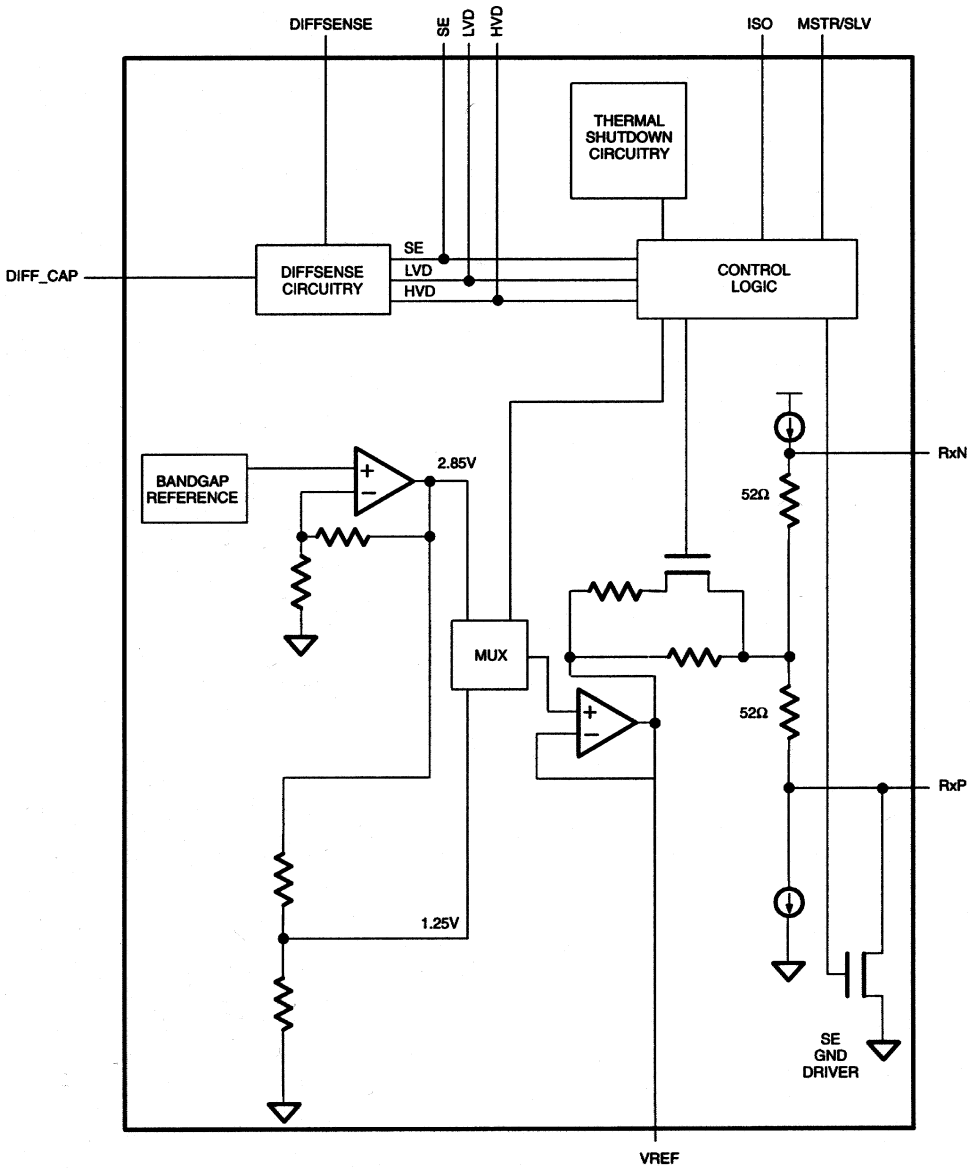
To maintain the specified regulation, a 4.7 µF capacitor is required between the Vref pin (VREF) and ground of each DS2120A. A high frequency cap (0.1 µF ceramic recommended) can also be placed on the Vref pin in applications that use fast rise/fall time drivers. A typical SCSI bus configuration is shown in Figure 2.

DIFFSENS noise filtering The DS2120A incorporates a digital filter to remove high frequency transients on the DIFFSENS control line, thereby eliminating erroneous switching between modes. This filter eliminates the need for the external capacitor and resistor, which heretofore performed this function. The external filter may be used in addition to the digital filter if the DS2120A and DS2118M are to be used interchangeably.

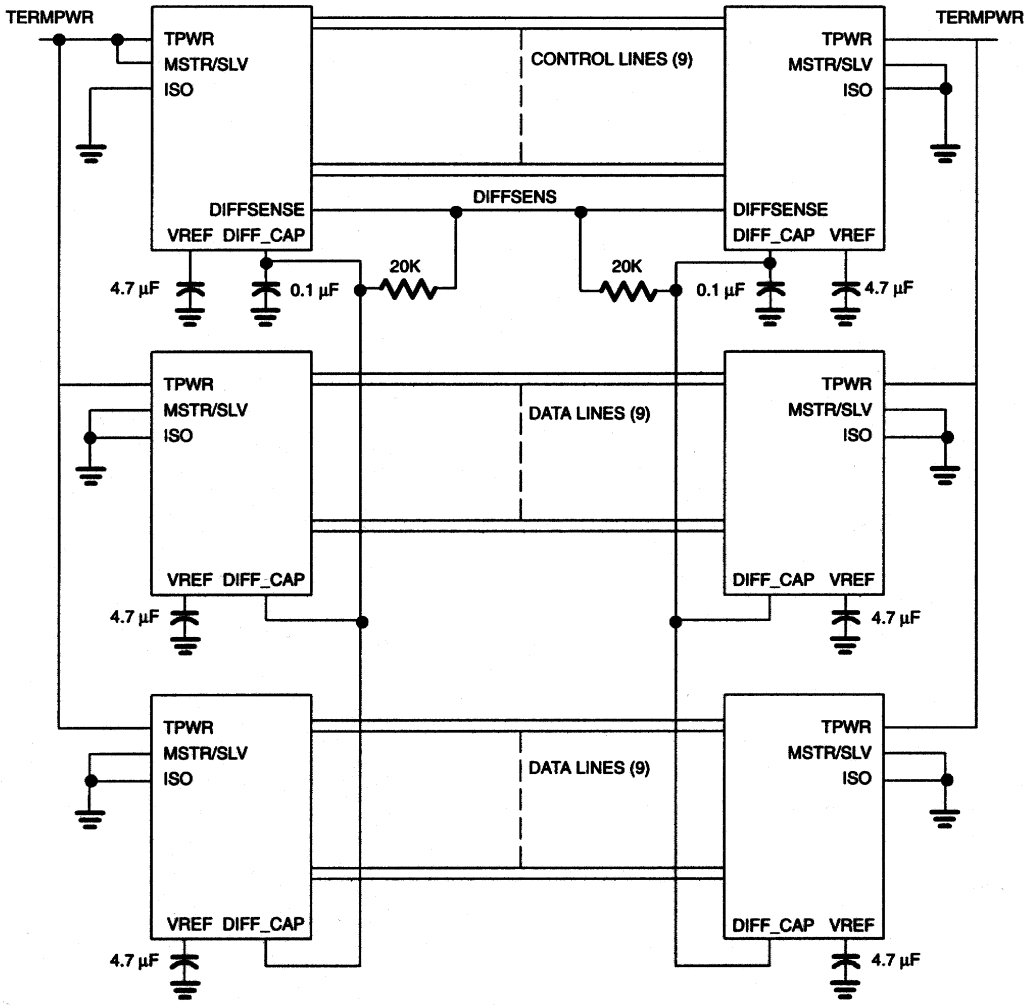
NOTE:

DIFFSENS – Refers to the SCSI bus signal.
DIFFSENSE – Refers to the DS2120A pin name and internal circuitry capable of driving the DIFFSENS line.
DIFF_CAP - Refers to the DS2120A pin name and internal circuitry relating to monitoring the DIFFSENS line.

DS2120A BLOCK DIAGRAM Figure 1



SCSI BUS CONFIGURATION Figure 2



PIN DESCRIPTION Table 1

PIN	SYMBOL	DESCRIPTION
1	VREF	**Reference Voltage.** 1.25 volt reference in LVD mode; must be decoupled with a 4.7 µF cap.
2, 3	NC	**No Connect.** Do not connect these pins.
4-7, 11-16, 22-25, 29-32	RxP RxN	**Signal Termination.** Connect to SCSI bus signal lines.
8, 10, 26, 9, 28, 27	HS GND	**Heat Sink Ground.** Internally connected to the mounting pad. Should be grounded.
17	ISO	**Isolation.** When pulled high, the DS2120A isolates its bus pins (RxP, RxN) from the SCSI bus.
18	GND	**Ground.** Signal ground; 0.0 volts.
19	MSTR/SLV	**Master/slave.** Mode select for the non-controlling terminator. When pulled high (MSTR), the DIFFSENSE driver is enabled.
20	DIFFSENSE	**DIFFSENSE.** Output to drive the SCSI bus DIFFSENS line.
21	DIFF_CAP	**DIFFSENSE CAPACITOR.** Connect 0.1 µF capacitor for DIFFSENSE filter. Input to detect the type of device (differential or single-ended) on the SCSI bus.
33	SE	**Single-ended.** SE output of DIFFSENSE receiver; output high indicates SE bus operation.
34	LVD	**Low Voltage Differential.** LVD output of DIFFSENSE receiver; output high indicates LVD bus operation.
35	HVD	**High Voltage Differential.** HVD output of DIFFSENSE receiver; output high indicates HVD bus operation or thermal shutdown.
36	TPWR	**Termination Power.** Connect to the SCSI TERMPWR line and decouple with 2.2 µF capacitor.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Termpower Voltage LVD mode	V_{tpwr}(LVD)	2.7		5.5	V	
Logic 0	V_{il}	-0.3		+0.8	V	
Logic 1	V_{ih}	2.0		V_{tpwr} + 0.3	V	
Operating Temperature	V_{amb}	0		70	°C	

LOW VOLTAGE DIFFERENTIAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Differential Mode Termination Resistance	Rdm	100		110	Ohms	
Common Mode Termination Resistance	Rcm	110		190	Ohms	
Differential Mode Bias	Vdm	100		125	mV	4
Common Mode Bias	Vcm	1.125		1.375	V	
Output Capacitance	Cout			3	pF	3

DC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Termpower Current	I_{tpmr}		12		mA	4
Input Leakage High	I_{ih}	-1.0			µA	
Input Leakage Low	I_{il}			1.0	µA	
Output Current High	I_{oh}	-1.0			mA	5, 7
Output Current Low	I_{ol}	4.0			mA	6, 7
DIFFSENS SE Operating Range	V_{seor}	-0.3		0.5	V	
DIFFSENS LVD Operating Range	V_{lvdor}	0.7		1.9	V	
DIFFSENS HVD Operating Range	V_{hvdor}	2.4		V_{tpwr} + 0.3	V	
DIFFSENSE Driver Output Voltage	V_{dso}	1.2		1.4	V	8, 9
DIFFSENSE Driver Source Current	I_{dsh}	5		15	mA	8, 10, 12
DIFFSENSE Driver Sink Current	I_{dsl}	20		200	µA	8, 11
Thermal Shutdown			150		ºC	3

REGULATOR CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Line Regulation	LI_{REG}		1.0	2.5	%	
Load Regulation	LO_{REG}		1.3	3.5	%	
Current Limit	I_{LIM}		550		mA	
Sink Current	I_{SINK}	200			mA	

NOTES:

1. Vline = 0-3.0 volts.
2. Vline = 0.2 volts.
3. Guaranteed by design.
4. All lines open.
5. V_{OUT} = 2.4 volts.
6. V_{OUT} = 0.4 volts.
7. SE/LVD/HVD pins only.
8. MSTR/SLV = 1.
9. I_{ds} = 0-5 mA.
10. V_{dso} = 0.0 volts.
11. V_{dso} = 2.75 volts.
12. TPWR = 5.5V

DS2120A 36-PIN SSOP PACKAGE

DIMENSIONS D AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.254 MM PER SIDE.

SECTION A-A DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.13 TO 0.25 MM FROM THE LEAD TIP.

THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

DIM	MIN	MAX
A	2.44	2.64
A1	0.12	-
b	0.29	0.43
c	0.23	0.32
D	15.20	15.54
E	10.11	10.52
E1	7.40	7.60
e	0.80 BSC	
h	0.25	0.71
L	0.51	1.02

DIMENSIONS ARE IN MILLIMETERS