DALLAS SEMICONDUCTOR

DS1921L-F5X
Thermochron iButton™

www.iButton.com

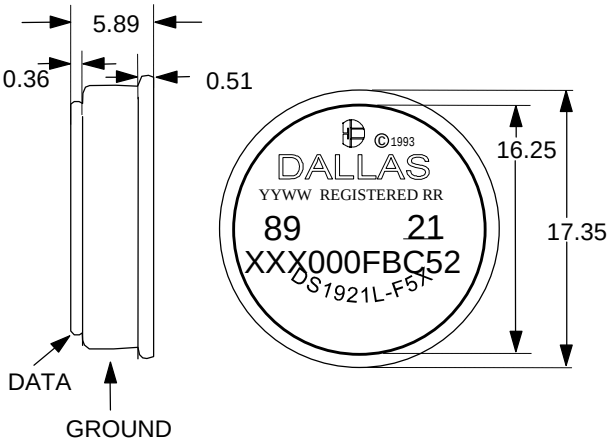
SPECIAL FEATURES

- Digital thermometer measures temperature from as low as -40°C to +85°C in 0.5°C increments
- Temperature conversion accuracy ± 1°C from as low as -20°C to +70°C
- Real-time clock/calendar in BCD format counts seconds, minutes, hours, date, month, day of the week, and year with leap year compensation; Y2K compliant
- Real-time clock accuracy ± 2 minutes per month from 0°C to 45°C
- Programmable temperature-high and temperature-low alarm trip points
- Automatically wakes up and measures temperature at user-programmable intervals from 1 to 255 minutes
- Logs up to 2048 consecutive temperature measurements in read-only nonvolatile memory
- Records a long-term temperature histogram with 2°C resolution (63 bins)
- Records time stamp and duration when temperature leaves the range specified by the trip points
- 4096 bits of general-purpose read/write nonvolatile memory
- 256-bit scratchpad ensures integrity of data transfer
- Overdrive mode boosts communication speed to 142k bits per second
- Memory partitioned into 256-bit pages for packetizing data
- On-chip 16-bit CRC generator to safeguard data read operations

COMMON iButton FEATURES

- Digital identification and information by momentary contact

F5 MICROCAN™



- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures absolute traceability because no two parts are alike
- Multidrop controller for MicroLAN
- Chip-based data carrier compactly stores information
- Data can be accessed while affixed to object
- Economically communicates to host with a single digital signal at 16.3 kbits per second
- Standard 16 mm diameter and 1-Wire™ protocol ensure compatibility with iButton Device family
- Button shape is self-aligning with cup-shaped probes
- Durable stainless steel case engraved with registration number withstands harsh environments
- Easily affixed with self-stick adhesive backing, latched by its flange, or locked with a ring pressed onto its rim
- Presence detector acknowledges when reader first applies voltage

- Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus: approved under Entity Concept for use in Class I, Division 1, Group A, B, C and D Locations (application pending)

EXAMPLES OF ACCESSORIES

DS9096P	Self-Stick Adhesive Pad
DS9101	Multi-Purpose Clip
DS9093RA	Mounting Lock Ring
DS9093A	Snap-In Fob
DS9092	iButton Probe

ORDERING INFORMATION

Part Number	Range of Accurate Operations	Packaging
DS1921L-F51	-10°C to +85°C	F5, Microcan
DS1921L-F52	-20°C to +85°C	F5, Microcan
DS1921L-F53	-30°C to +85°C	F5, Microcan

iButton DESCRIPTION

The DS1921L-F5X Thermochron iButtons are rugged, self-sufficient systems that, once setup for a mission, measure temperature and record the result in a protected memory section. The recording is done at a user-defined rate, both as a direct storage of temperature values at incrementing memory addresses as well as in the form of a histogram. Up to 2048 temperature values taken at equidistant intervals ranging from 1 to 255 minutes can be stored. The histogram provides 63 data bins for a resolution of 2°C. Each bin is implemented as a 16-bit binary counter that is incremented if the value of a temperature measurement falls into the range of the bin. If the temperature leaves a user-programmable range, the DS1921 will also record when this happened, for how long the temperature stayed outside the permitted range, and if the temperature was too high or too low. A total of 24 such events can be recorded, 12 for exceeding each temperature limit. Additional read/write non-volatile memory independent of the memory used for temperature logging offers a simple solution to storing and retrieving information pertaining to the object to which the DS1921 is associated. Data is transferred serially via the 1-Wire protocol, which requires only a single data lead and a ground return and which allows the device to be accessed with minimal hardware.

The scratchpad is an additional memory area that acts as a buffer when writing to the read/write memory and to the special function registers required to mission the device. Data is first written to the scratchpad where it can be read back. After the data has been verified, a Copy Scratchpad command will transfer the data to memory. This process ensures data integrity when modifying the memory. A 48-bit serial number is factory-lasered into each DS1921 to provide a guaranteed unique identity which allows for absolute traceability. The durable MicroCan package is highly resistant to environmental hazards such as dirt, moisture, and shock. Its compact, coin-shaped profile is self-aligning with mating receptacles, allowing the DS1921 to be easily used by human operators. Accessories permit the DS1921 to be mounted on almost any surface, including containers, pallets and bags.

APPLICATION

The DS1921 Thermochron iButton is an ideal device to monitor the temperature of any object it is attached to or shipped with, such as perishable goods or containers of temperature sensitive chemicals. Using TMEX, the read/write nonvolatile memory can store an electronic copy of shipping information, date of manufacture and other important data written as clear as well as encrypted files. The unique registration number and a non-resettable counter that increments with each new mission provide traceability and evidence in case of tampering with the device.

OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS1921. The DS1921 has seven main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 4096-bit SRAM, 4) 256-bit of timekeeping, control and counter registers, 5) 2048 bytes of data-logging memory, 6) 128 bytes of histogram memory, and 7) 96 bytes of event/duration recording memory. Except for the ROM and the scratchpad, all other memory is arranged in a single linear address space. All memory reserved for logging purposes, the counter registers and several other registers are read-only for the user. The timekeeping and control registers are write-protected while the device is programmed for a mission.

The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the seven ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Conditional Search ROM, 5) Skip ROM, 6) Overdrive-Skip ROM or 7) Overdrive-Match ROM. Upon completion of an Over-drive ROM command byte executed at standard speed, the device will enter Overdrive mode, where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 9. After a ROM function command is successfully executed, the memory functions become accessible and the master may provide any one of the seven memory function commands. The protocol for these memory function commands is described in Figure 7. All data is read and written least significant bit first.

PARASITE POWER

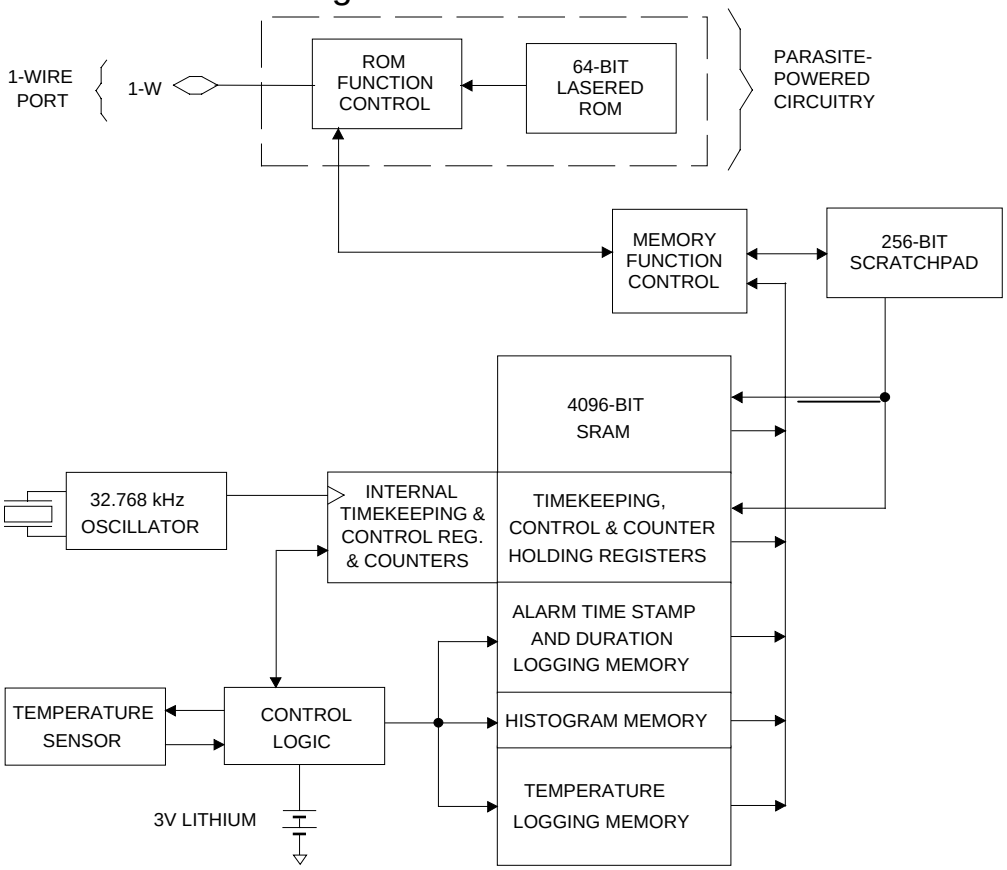
The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry "steals" power whenever the I/O input is high. I/O will provide sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) by parasiting off this input, lithium is conserved; and 2) if the lithium is exhausted for any reason, the ROM may still be read normally.

64-BIT LASERED ROM

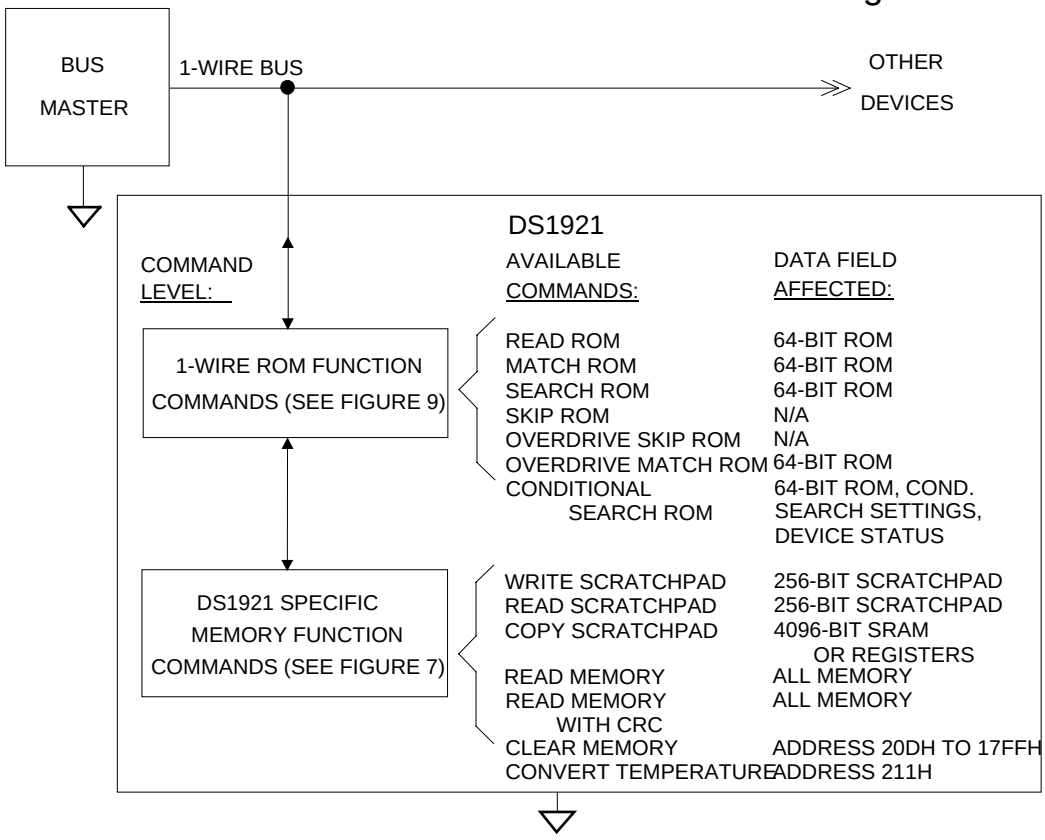
Each DS1921 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. (See Figure 3). The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in the Book of DS19xx iButton Standards.

The shift register bits are initialized to 0. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8^{th} bit of the family code has been entered, then the serial number is entered. After the 48^{th} bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC should return the shift register to all 0s.

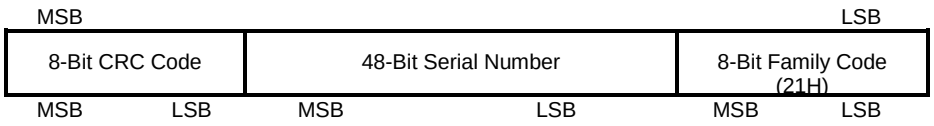
DS1921 BLOCK DIAGRAM Figure 1



HIERARCHICAL STRUCTURE FOR 1-WIRE PROTOCOL Figure 2

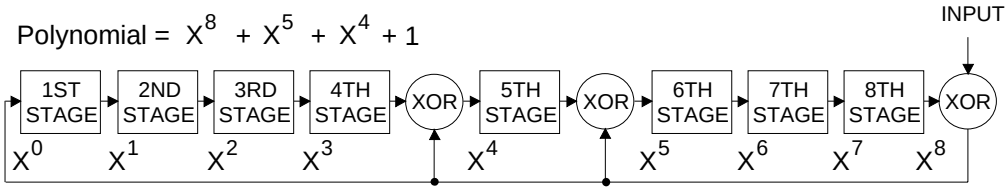


64-BIT LASERED ROM Figure 3



The most significant 12 bits of the 48-bit serial number are being used in the DS1921L-F5X Thermochron product series to identify both the lower limit and the range of accurate operations, as described in ROM ENCODING vs. RANGE OF ACCURATE OPERATIONS in the last section of this document. Software developers may use this coding mechanism to automatically determine the validity of sampled temperature values based on the content of this 12-bit field.

1-WIRE CRC GENERATOR Figure 4



MEMORY

The memory map in Figure 5a shows a 32-byte page called the scratchpad and additional 32-byte pages assigned to various purposes. The 4096-bit SRAM make up pages 0 through 15 of the DS1921. The timekeeping, control and counter registers fill page 16 (Register Page, Figure 5b). Pages 17 to 19 are assigned to storing the alarm time stamps and durations. The temperature histogram bins begin at page 64 and use up four pages. The temperature logging memory covers pages 128 to 191. Memory pages 20 to 63, 68 to 127 and 192 to 255 are reserved for future extensions. The scratchpad is an additional page that acts as a buffer when writing to the SRAM memory or the timekeeping, control and counter registers. The memory pages 17 and higher are read-only for the user. They are written to or erased solely under supervision of the on-chip control logic.

TIMEKEEPING

The real-time clock/alarm and calendar information is accessed by reading/ writing the appropriate bytes in the register page (Figure 5b, address 200h to 206h). Note that some bits are set to 0. These bits will always read 0 regardless of how they are written. The contents of the time, calendar, and alarm registers are in the BCD format (Binary-Coded Decimal).

Real-Time Clock/Calendar

The real-time clock of the DS1921 can run in either 12-hour or 24-hour mode. Bit 6 of the Hours Register (address 202h) is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic 1 being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20 - 23 hours).

To distinguish between the days of the week the DS1921 includes a counter with a range from 1 to 7. The assignment of counter value to the day of week is arbitrary. Typically the number 1 is assigned to a Sunday (U.S. standard) or to a Monday (European standard).

The calendar logic is designed to automatically compensate for leap years. For every year value that is either 00 or a multiple of 4 the device will add a 29th of February. This will work correctly up to (but not including) the year 2100.

The DS1921 is Year 2000-compliant. Bit 7 (CENT) of the Months Register at address 205h serves as a century flag. When the Year Register rolls over from (19)99 to (20)00 the century flag will toggle. It is recommended to write the century bit to a 0 when setting the real-time clock to a time/date before the year 2000.

Real-Time Clock Alarms

The DS1921 also contains a real-time clock alarm function. The alarm registers are located in registers 207h to 20Ah. The most significant bit of each of the alarm registers is a mask bit (see Table 1). When all of the mask bits are logic 0, an alarm will occur once per week when the values stored in timekeeping registers 200h to 203h match the values stored in the time of day alarm registers. Any alarm will set the Timer Alarm Flag (TAF) in the device's Status Register (address 214h). The bus master may set the Search Conditions (address 20Eh) to identify devices with timer alarms by means of the Conditional Search function (see ROM Function Commands).

TIME OF DAY ALARM BITS Table 1

ALARM REGISTER MASK BITS (BIT 7)				
MS	**MM**	**MH**	**MD**	
1	1	1	1	ALARM ONCE PER SECOND.
0	1	1	1	ALARM WHEN SECONDS MATCH (ONCE PER MINUTE).
0	0	1	1	ALARM WHEN MINUTES AND SECONDS MATCH (ONCE EVERY HOUR).
0	0	0	1	ALARM WHEN HOURS, MINUTES AND SECONDS MATCH (ONCE EVERY DAY).
0	0	0	0	ALARM WHEN DAY, HOURS, MINUTES AND SECONDS MATCH (ONCE EVERY WEEK).

Temperature Conversion

The temperature sensor of the DS1921 can accurately measure temperatures from as low as -40°C to +85°C in 0.5°C increments. Temperature readings are represented in a single byte as an unsigned binary number (Table 2). The possible values range from 00000000 (for -40°C) to 1111 1010 (for +85°C). With T[7..0] representing the decimal equivalent of the binary temperature reading the temperature value is calculated as

$$\theta(°C) = T[7..0] / 2 - 40$$

This formula is valid for converting temperature readings stored in the temperature logging memory as well as for data read from the Temperature Read-out Register (address 211h). To specify the high and low temperature alarm thresholds this formula needs to be resolved to

$$T[7..0] = 2 \times \theta(°C) + 80$$

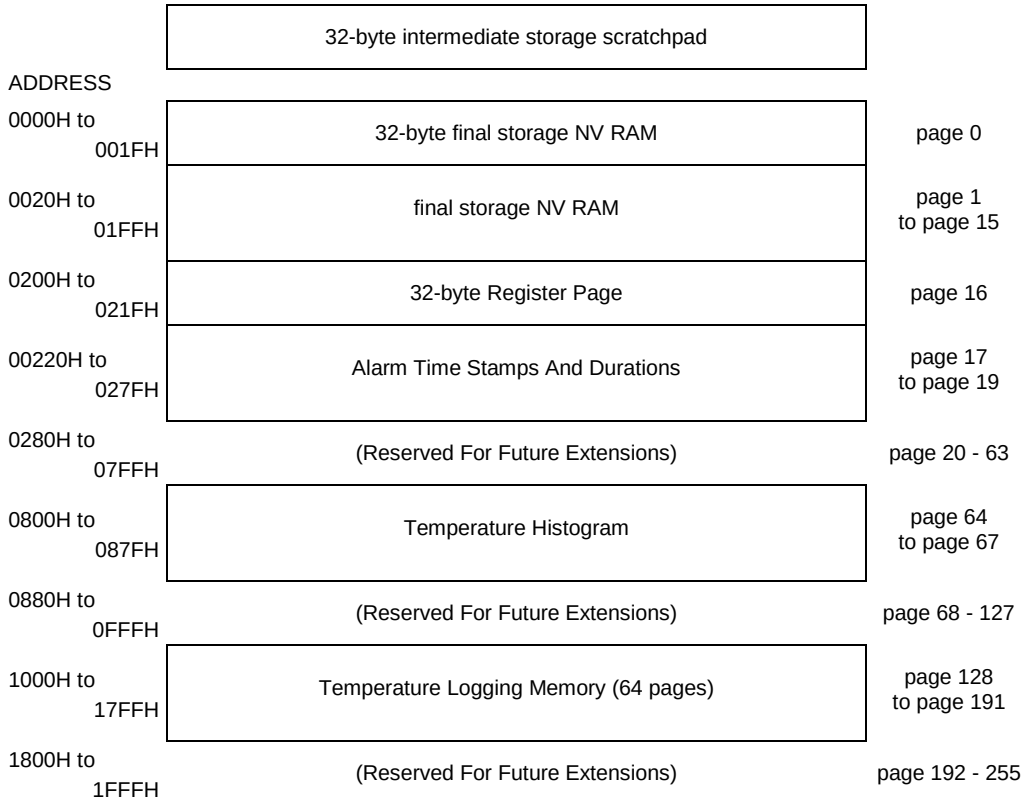
A value of 23°C, for example, thus translates into 126, which is then written as a binary pattern of 01111110 to the Temperature Alarm Register. The value of -20°C, as another example, is represented as 00101000.

Temperatures below -40°C will be recorded as 00000000 (=-40°C)[1]. Temperatures higher than +85°C will be recorded as 111111010 (=85°C).

TEMPERATURE DATA BYTE FORMAT Table 2

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
T7	T6	T5	T4	T3	T2	T1	T0

DS1921 MEMORY MAP Figure 5a



DS1921 REGISTER PAGE Figure 5b

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function
200	0	10 Seconds			Single Seconds				Real-Time Clock Registers
201	0	10 Minutes			Single Minutes				
202	0	12/24	10 h. A/P	10h.	Single Hours				
203	0	0	0	0	0	Day of Week			
204	0	0	10 Date		Single Date				
205	CENT	0	0	10 m.	Single Months				
206	10 Years				Single Years				
207	MS	10 Seconds Alarm			Single Seconds Alarm				Real-Time Clock Alarm
208	MM	10 Minutes Alarm			Single Minutes Alarm				
209	MH	12/24	10 ha. A/P	10 h. alm.	Single Hours Alarm				
20A	MD	0	0	0	0	Day of Week Alarm			
20B	Low Temperature Threshold								Temperature Alarm
20C	High Temperature Threshold								
20D	Number of Minutes Between Temperature Conversions								Sample Rate
20E	$\overline{\text{EOSC}}$	MCLRE	0	$\overline{\text{EM}}$	RO	TLS	THS	TAS	Control
20F	0	0	0	0	0	0	0	0	(No Function)
210	0	0	0	0	0	0	0	0	
211	Temperature Read Out (forced conversion)								Temperature
212	Low Byte								Mission Start Delay
213	High Byte								
214	$\overline{\text{TCB}}$	MEMCLR	MIP	SIP	0	TLF	THF	TAF	Status
215	0	10 Minutes			Single Minutes				Mission Time Stamp
216	0	12/24	10 h. A/P	10h.	Single Hours				
217	0	0	10 Date		Single Date				
218	Unused*	0	0	10 m.	Single Months				
219	10 Years				Single Years				
21A	Low Byte								Mission Samples Counter
21B	Medium Byte								
21C	High Byte								
21D	Low Byte								Device Samples Counter
21E	Medium Byte								
21F	High Byte								

ADDRESS REGISTERS Figure 6

TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	1)	PF	E4	E3	E2	E1	E0

1) THIS BIT WILL ALWAYS BE 0.

* This bit maybe used in the future to represent the century as does the CENT bit of the RTC registers. See end note 11 for an example of program logic that works with both the current and future versions of Thermochrons.

Temperature Logging And Histogram

Once setup for a mission, the DS1921 logs the temperature measurements simultaneously byte after byte in the temperature logging memory as well as in histogram form in the histogram memory.

The temperature logging memory is able to store 2048 temperature values measured at equidistant time points. The time/date stamp of when the device was setup for a mission is stored as Mission Time Stamp in the register page, addresses 215h to 219h. The first temperature value of a mission is written to address location 1000h of the temperature logging memory, the second value to address location 1001h and so on. With the starting time point and the interval between temperature measurements known, one can exactly reconstruct the time and date each measurement was taken.

There are two alternatives to the way the DS1921 will behave after the 2048 bytes of temperature logging memory is filled with data. The user can program the device to either stop any further recording or overwrite the previously recorded data (enable "rollover"), one byte at a time, starting again at address 1000h for the 2049th temperature value. The contents of the Mission Samples Counter (addresses 21Ah to 21Ch) in conjunction with the sample rate and the mission time stamp will then allow reconstructing the time points of all values stored in the temperature logging memory. This gives the exact temperature history over time for the latest 2048 measurements taken. All earlier measurements cannot be reconstructed. Regardless of enabling the rollover, these values indirectly show up in the temperature histogram.

For the temperature histogram, the DS1921 provides 63 bins that begin at memory address 0800h. Each bin consists of a 16-bit, non-rolling-over binary counter that is incremented each time a temperature value acquired during a mission falls into the range of the bin. The least significant byte of each bin is stored at the lower address. Bin 1 begins at memory address 0800h, bin 2 at 0802h, and so on up to 087Ch for bin 63.

After a temperature conversion is completed the number of the bin to be updated is determined by cutting off the two least significant bits of the binary temperature value. Thus bin 1 will be updated with every temperature reading from -40°C or lower to -38.5°C. Bin 2 is associated with the range of -38.0°C to -36.5°C and so on[1]. Bin 63, finally, counts temperature values of +84°C and higher. Since each data bin is 2 bytes it can increment up to 65535 times. If more samples for a given data bin are measured, the data bin will remain at its maximum value. With the fastest sample rate of one sample every minute, this is sufficient for up to 45 days if all temperature readings fall into the same bin.

Temperature Alarm logging

For some applications it may be essential to not only record temperature over time and the temperature histogram, but also record **when** exactly the temperature has exceeded a predefined tolerance band and for **how long** the temperature stayed outside the desirable range. The DS1921 is able to provide this information, too. The tolerance band is specified by means of the Temperature Alarm Registers, addresses 20Bh and 20Ch in the register page. One can set a high and a low temperature threshold. See section "Temperature Conversion" for the data format the temperature has to be written in. As long as the temperature values stay within the tolerance band, i.e., are higher than the low threshold and lower than the high threshold, the DS1921 will not record any temperature alarm. If the temperature during a mission reaches or exceeds either threshold, the DS1921 will generate an alarm and set either the Temperature High Flag (THF) or the Temperature Low Flag (TLF) in the Status Register (address 214h). In addition, the device generates a time stamp of when the alarm occurred and begins recording the duration of the alarming condition.

[1] The temperature and histogram logs are meaningful only when the temperature values are within the stated range of accurate operations, as shown in the ordering information table.

The device stores a time stamp as a copy of the Mission Samples Counter when the alarm occurred. The least significant byte is stored at the lower address. One address higher than a time stamp the DS1921 maintains a 1-byte duration counter that stores the number of times the temperature was found to be beyond the threshold. If this counter has reached its limit after 255 consecutive temperature readings and the temperature has not yet returned to within the tolerance band, the device will issue another time stamp at the next higher address and open another counter to record the duration. If the temperature returns to normal before the counter has reached its limit, the duration counter of the particular time stamp will not increment any further. Should the temperature again cross this threshold, another time stamp will be recorded and its associated counter will increment with each temperature reading outside the tolerance band. This algorithm is implemented for the low as well as for the high temperature threshold.

Time stamps and durations where the temperature leaves the tolerance band to the low (cold) side are stored in the address range 0220h to 024Fh (48 bytes). The memory address range 0250h to 027Fh (48 bytes) is reserved for time stamps and duration where the temperature leaves the tolerance band to the high (hot) side. This allocation allows recording 24 individual alarm events and periods (12 periods for too hot and 12 for too cold). The date and time of each of these periods can be determined from the Mission Time Stamp and the time distance between each temperature reading.

Devices with temperature alarms can be identified by the bus master by means of the Conditional Search function (see "ROM Function Commands") if the Search Conditions (address 20Eh) are set accordingly.

CONTROL/STATUS REGISTER

The DS1921 is set up for its operation by writing appropriate data to its special function registers that are located in the register page. Several functions that are controlled by a single bit only are combined into a single byte called Control Register (address 20Eh). This register can be read and written. If the device is programmed for a mission, writing to the Control Register or any other writable register (addresses 200 to 213h) **will at the first attempt end the mission**, but not overwrite any settings. Every subsequent write attempt, however, will change the register contents.

In the same way as the Control Register is used to control single-bit functions, the Status Register provides a read-out for single-bit status information. The Status Register is located at address 214h and is read-only, except for bit 5 (MIP). Write accesses to any other register/counter in the address range of 215h and higher are ignored. They do not have any effect on the status or behavior of the device.

Control Register (Address 20Eh)

Bit 0 | TAS | Timer Alarm Search

If this bit is 1, the device will respond to a Conditional Search command if during a mission a timer alarm has occurred. Since a timer alarm cannot be disabled, the TAF flag usually reads 1 during a mission. Therefore it may be advisable to set the TAS bit to a 0, in most cases.

Bit 1 | THS | Temperature High Alarm Search

If this bit is 1, the device will respond to a Conditional Search command if during a mission the temperature has reached or is higher than the High Temperature Threshold.

Bit 2 | TLS | Temperature Low Alarm Search

If this bit is 1, the device will respond to a Conditional Search command if during a mission the temperature has reached or is lower than the Low Temperature Threshold.

Bit 3 | RO | Rollover Enable/Disable

This bit controls whether the temperature logging memory is overwritten with new data or whether data logging is stopped once the memory is filled with data during a mission. Setting this bit to a 1 enables the rollover and data logging continues at the beginning overwriting previously collected data. Clearing this bit to a 0 disables the rollover and no further temperature values will be stored in the temperature logging memory once it is filled with data.

Bit 4 | $\overline{\text{EM}}$ | Enable Mission

This bit controls whether the DS1921 will begin a mission as soon as the sample rate is written. To enable the device for a mission, this bit must be 0.

Bit 5 | 0 | 0 (no function, reads always 0)

Bit 6 | MCLRE | Memory Clear Enable

This bit needs to be set to a logic 1 to enable the Clear Memory function which is invoked as a memory function command. The Time-Stamp, Histogram and Logging Memory as well as the Mission Time Stamp, Mission Samples Counter, Mission Start Delay and Sample Rate will be cleared only if the Clear Memory command is issued **with the next access to the device**. The MCLRE bit will return to 0 as the next memory function command is executed.

Bit 7 | $\overline{\text{EOSC}}$ | Enable Oscillator

This bit controls the crystal oscillator of the real-time clock. When set to a logic 0, the oscillator will start operation. When written to a logic 1, the oscillator will stop and the device is in a low-power data retention mode. **This bit must be 0 for normal operation.**

Status Register (Address 214h)

Bit 0 | TAF | Timer Alarm Flag

If this bit reads 1 a real-time clock alarm has occurred (see section TIMEKEEPING for details). The Timer Alarm Flag is cleared by writing this bit to a logic 0. Since the timer alarm cannot be disabled, the TAF flag usually reads 1 during a mission.

Bit 1 | THF | Temperature High Flag

A logic 1 in the Temperature High Flag bit indicates that a temperature measurement during a mission revealed a temperature equal to or higher than the value in the High Temperature Threshold Register. THF is cleared by writing this bit to a logic 0.

Bit 2 | TLF | Temperature Low Flag

A logic 1 in the Temperature Low Flag bit indicates that a temperature measurement during a mission revealed a temperature equal to or lower than the value in the Low Temperature Threshold Register. TLF is cleared by writing this bit to a logic 0.

Bit 3 | 0 | (no function, reads always 0)

Bit 4 | SIP | Sample in Progress

If this bit reads 1 the DS1921 is currently performing a self-initiated temperature conversion as part of a mission in progress. The SIP bit will change from 0 to 1 approximately 250 ms before the actual temperature conversion begins allowing the circuitry of the chip to wake-up. A temperature conversion including a "wake-up phase" takes maximum 750 ms. During this time read accesses to the memory pages 17 and higher are permissible but may reveal invalid data.

Bit 5 | MIP | Mission In Progress

If this bit reads 1 the DS1921 has been set up for a mission and this mission is still in progress. A mission is started if the $\overline{EM}$ bit of the Control Register (address 20Eh) is 0 and a non-0 value is written to the Sample Rate Register, address 20Dh. The MIP bit returns from a logic 1 to a logic 0 when a mission is ended. A mission will end with the first write attempt (Copy Scratchpad command) to any register in the address range of 200h to 213h. The first write access will only end the mission and not alter any data, even if the AA-bit in the E/S Register reads 1 (see Copy Scratchpad command). An alternative method to end a mission is directly writing to the Status Register, address 214, and setting the MIP bit to 0. This write access will alter the bit already at the first attempt. The MIP bit can only be written to a 0. All other status bits are read-only.

Bit 6 | MEMCLR | Memory cleared

If this bit reads 1 all the memory pages 17 and higher (alarm time stamps/durations, temperature histogram, temperature log), as well as the Mission Time Stamp, Mission Samples Counter, Mission Start Delay and Sample Rate have been cleared to 0 from executing a Clear Memory function command. The MEMCLR bit will return to 0 as soon as a new mission is started by writing a non-0 value to the Sample Rate Register provided that the $\overline{EM}$ bit is also 0. **The memory has to be cleared in order for a mission to start**.

Bit 7 | $\overline{TCB}$ | Temperature Core Busy

If this bit reads 0 the DS1921 is currently performing a temperature conversion, either self-initiated because of a mission being in progress or initiated by a command when a mission is not in progress. The SIP bit will change from 1 to 0 approximately 250 ms before the actual temperature conversion begins allowing the circuitry of the chip to wake-up. A temperature conversion including a "wake-up phase" takes maximum 750 ms. During this time read accesses to the memory pages 17 and higher are permissible but may reveal invalid data.

MISSIONING

The typical task of the DS1921 is recording the temperature of a temperature-sensitive object that is traveling from one place to another. Usually space limitations and economic reasons do not allow such objects being monitored by sensors directly connected to a computer. Since it is small enough to be mounted on almost any object the DS1921 can travel directly with the object and monitor its temperature. Setting up the DS1921 for such a journey or mission is called missioning.

Before it is able to record valid data, the DS1921 needs to have its real-time clock set to valid time and date. This reference time may be UTC (also called GMT, Greenwich Mean Time) or any other time standard the sender and receiver of the object have agreed on. The clock must be running ($\overline{EOSC}$ = 0). Setting a real-time clock alarm is optional. The memory assigned to storing alarm time stamps and durations, temperature histogram, temperature log as well as the Mission Time Stamp, Mission Samples Counter, Mission Start Delay and Sample Rate must be cleared using the Memory Clear command. To enable the device for a mission, the $\overline{EM}$ flag must be set to 0. These are general settings that have to be made regardless of the type of object to be monitored and the duration of the mission.

Next the low temperature and high temperature thresholds to specify the temperature tolerance band must be written. How to convert a temperature value into the binary code to be written to the threshold registers is described under “Temperature Conversion” earlier in this document.

The state of the Search Condition bits in the Control Register does not affect the mission. If multiple devices are connected to form a MicroLAN bus, the setting of the search condition will enable devices to participate in the conditional search if certain events such as timer or temperature alarm have occurred. Details on the search conditions are found in the section “ROM Function Commands” later in this document and in the Control Register description.

The setting of the RO bit (rollover enable) and sample rate depend on the duration of the mission and the monitoring requirements. If the most recent temperature history is important, the rollover should be enabled (RO = 1). Otherwise one should estimate the duration of the mission in minutes and divide the number by 2048 to calculate the value of the sample rate (number of minutes between temperature conversions). If the estimated duration of a mission is 10 days (= 14400 minutes), for example, then the 2048-byte capacity of the temperature logging memory would be sufficient to store a new value every 7 minutes. Since large objects do not change their temperature very quickly when left to their environment, one could even chose a sample rate of 10 minutes without the risk of losing valuable information, reserving memory space for unexpected delays.

If a mission is fairly long and the temperature logging memory of the DS1921 is not large enough to store all temperature readings, one can use several DS1921 and set the Mission Start Delay to values that make the second device start recording as soon as the memory of the first device is full, and so on for the third and fourth device, etc. The RO bit needs to be set to 0 to disable rollover that would otherwise overwrite the recorded temperature log. The Mission Start Delay is stored in minutes as unsigned 16-bit integer number at addresses 212h and 213h. The maximum delay is 65535 minutes, equivalent to 45 days, 12 hours and 15 minutes. The delay determines how many minutes will have to expire after the beginning of a mission until the first temperature measurement of the mission is done.

After the RO bit and the Mission Start Delay are set, the sample rate is the last element of data that is written to the Sample Rate Register. The sample rate may be any value from 1 to 255, coded as an unsigned 8-bit binary number. As soon as the sample rate is written, the DS1921 will copy the current

time and date into the Mission Time Stamp Register[2], and set the MIP flag and clear the MEMCLR flag. After as many minutes as specified by the Mission Start Delay are over, the device will do the first temperature conversion of the mission. This will increment both the Mission Samples Counter and Device Samples Counter. All subsequent temperature measurements will be made as many minutes apart from each other as specified by the value in the Sample Rate Register. One may read the memory of the DS1921 to watch the mission as it progresses at any time.

After the mission is started, one should read the complete register page and store the contents of the Temperature Alarm Registers up to the Device Samples Counter in encrypted form as data file in the 4096-bit SRAM section of the device. This general purpose memory operates independently of the memory used for recording during a mission. However, one must not try writing any of the writable registers of the register page since this will end the mission.

ADDRESS REGISTERS AND TRANSFER STATUS

Because of the serial data transfer, the DS1921 employs three address registers, called TA1, TA2 and E/S (Figure 6). Registers TA1 and TA2 must be loaded with the target address to which the data will be written or from which data will be sent to the master upon a Read command. Register E/S acts like a byte counter and transfer status register. It is used to verify data integrity with Write commands. Therefore, the master only has read access to this register. The lower 5 bits of the E/S Register indicate the address of the last byte that has been written to the scratchpad. This address is called Ending Offset. Bit 5 of the E/S Register, called PF or "partial byte flag," is set if the number of data bits sent by the master is not an integer multiple of 8. Bit 6 is always a 0. Note that the lowest 5 bits of the target address also determine the address within the scratchpad, where intermediate storage of data will begin. This address is called byte offset. If the target address for a Write command is 13Ch, for example, then the scratchpad will store incoming data beginning at the byte offset 1Ch and will be full after only 4 bytes. The corresponding ending offset in this example is 1Fh. For best economy of speed and efficiency, the target address for writing should point to the beginning of a new page, i.e., the byte offset will be 0. Thus the full 32-byte capacity of the scratchpad is available, resulting also in the ending offset of 1Fh. However, it is possible to write 1 or several contiguous bytes somewhere within a page. The ending offset together with the Partial and Overflow Flag is mainly a means to support the master checking the data integrity after a Write command. The highest valued bit of the E/S Register, called AA or Authorization Accepted, acts as a flag to indicate that the data stored in the scratchpad has already been copied to the target memory address. Writing data to the scratchpad clears this flag.

WRITING WITH VERIFICATION

To write data to the DS1921, the scratchpad has to be used as intermediate storage. First the master issues the Write Scratchpad command to specify the desired target address, followed by the data to be written to the scratchpad. In the next step, the master sends the Read Scratchpad command to read the scratchpad and to verify data integrity. As preamble to the scratchpad data, the DS1921 sends the requested target address TA1 and TA2 and the contents of the E/S Register. If the PF flag is set, data did not arrive correctly in the scratchpad. The master does not need to continue reading; it can start a new trial to write data to the scratchpad. Similarly, a set AA flag indicates that the Write command was not recognized by the iButton. If everything went correctly, both flags are cleared and the ending offset indicates the address of the last byte written to the scratchpad. Now the master can continue verifying every data bit. After the master has verified the data, it has to send the Copy Scratchpad command. This command must be

[2] Note that currently the CENT bit of the RTC registers is not copied to the Mission Time Stamp. The future versions of Thermochron may implement the corresponding CENT bit in the Mission Time Stamp registers and the RTC CENT bit value would be copied into it. Please see note 11 for an example of how Dallas Semiconductor's iButton viewer implements the Mission Time Stamp century bit calculation that would work with both the current and future versions of Thermochrons.

followed exactly by the data of the three address registers TA1, TA2 and E/S as the master has read them verifying the scratchpad. As soon as the DS1921 has received these bytes, it will copy the data to the requested location beginning at the target address.

MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 7) describes the protocols necessary for accessing the memory. An example follows the flowchart. The communication between master and DS1921 takes place either at regular speed (default, OD = 0) or at Overdrive Speed (OD = 1). If not explicitly set into the Overdrive Mode the DS1921 assumes regular speed.

Write Scratchpad Command [0Fh]

After issuing the Write Scratchpad command, the master must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data will be written to the scratchpad starting at the byte offset (T4:T0). The ending offset (E4:E0) will be the byte offset at which the master stops writing data. Only full data bytes are accepted. If the last data byte is incomplete, its content will be ignored and the partial byte flag PF will be set.

When executing the Write Scratchpad command the CRC generator inside the DS1921 (see Figure 12) calculates a CRC of the entire data stream, starting at the command code and ending at the last data byte sent by the master. This CRC is generated using the CRC16 polynomial by first clearing the CRC generator and then shifting in the command code (0Fh) of the Write Scratchpad command, the Target Addresses TA1 and TA2 as supplied by the master and all the data bytes. The master may end the Write Scratchpad command at any time. However, if the ending offset is 11111b, the master may send 16 read time slots and will receive the CRC generated by the DS1921.

The range 200h to 213h of the register page is write-protected during a mission. See the Status Register description for details.

Read Scratchpad Command [AAh]

This command is used to verify scratchpad data and target address. After issuing the Read Scratchpad command, the master begins reading. The first 2 bytes will be the target address. The next byte will be the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset (T4:T0). Regardless of the actual ending offset the master may read data until the end of the scratchpad after which it will receive a CRC16 of the command code, Target Addresses TA1 and TA2, the E/S byte, and the scratchpad data starting at the target address. After the CRC is read, the bus master will receive logical 1s from the DS1921 until a reset pulse is issued.

Copy Scratchpad [55h]

This command is used to copy data from the scratchpad to memory. After issuing the Copy Scratchpad command, the master must provide a 3-byte authorization pattern which can be obtained by reading the scratchpad for verification. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA (Authorization Accepted) flag will be set and the copy will begin. A pattern of alternating 1s and 0s will be transmitted after the data has been copied until a reset pulse is issued by the master. Any attempt to reset the part will be ignored while the copy is in progress. Copy typically takes 2 µs per byte.

The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset, will be copied to memory, starting at the target address. Anywhere from 1 to 32 bytes may be copied to memory with this command. The AA flag will be cleared only by executing a Write Scratchpad command.

Read Memory [F0h]

The Read Memory command may be used to read the entire memory. After issuing the command, the master must provide the 2-byte target address. After the 2 bytes, the master reads data beginning from the target address and may continue until the end of memory, at which point logic 1s will be read. It is important to realize that the target address registers will contain the address provided. The ending offset/data status byte is unaffected.

The hardware of the DS1921 provides a means to accomplish error-free writing to the memory section. To safeguard reading data in the 1-Wire environment and to simultaneously speed up data transfers, it is recommended to packetize data into data packets of the size of one memory page each. Such a packet would typically store a 16-bit CRC with each page of data to ensure rapid, error-free data transfers that eliminate having to read a page multiple times to determine if the received data is correct or not. (See the Book of DS19xx iButton Standards, Chapter 7 or Application Note 114 for the recommended file structure.)

Read Memory with CRC [A5h]

The Read Memory with CRC command is used to read memory data that cannot be packetized, such as the register page and the data recorded by the device during a mission. Following the last data byte of the memory page addressed the DS1921 transmits a 16-bit CRC generated by the device.

After having sent the command code of the Read Memory with CRC command, the bus master sends a 2-byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. With the subsequent read data time slots the master receives data from the DS1921 starting at the initial address and continuing until the end of a 32-byte page is reached. At that point the bus master will send 16 additional read data time slots and receive the 16-bit CRC. With subsequent read data time slots the master will receive data starting at the beginning of the next page followed again by the CRC for that page. This sequence will continue until the final page is read by the bus master.

With the initial pass through the Read Memory with CRC flow chart the 16-bit CRC value is the result of shifting the command byte into the cleared CRC generator followed by the 2 address bytes and the contents of the data memory. Subsequent passes through the Read Memory with CRC flow chart will generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the contents of the data memory page. After the 16-bit CRC of the last page is read, the bus master will receive logical 1s from the DS1921 until a reset pulse is issued. The Read Memory with CRC command sequence can be ended at any point by issuing a reset pulse.

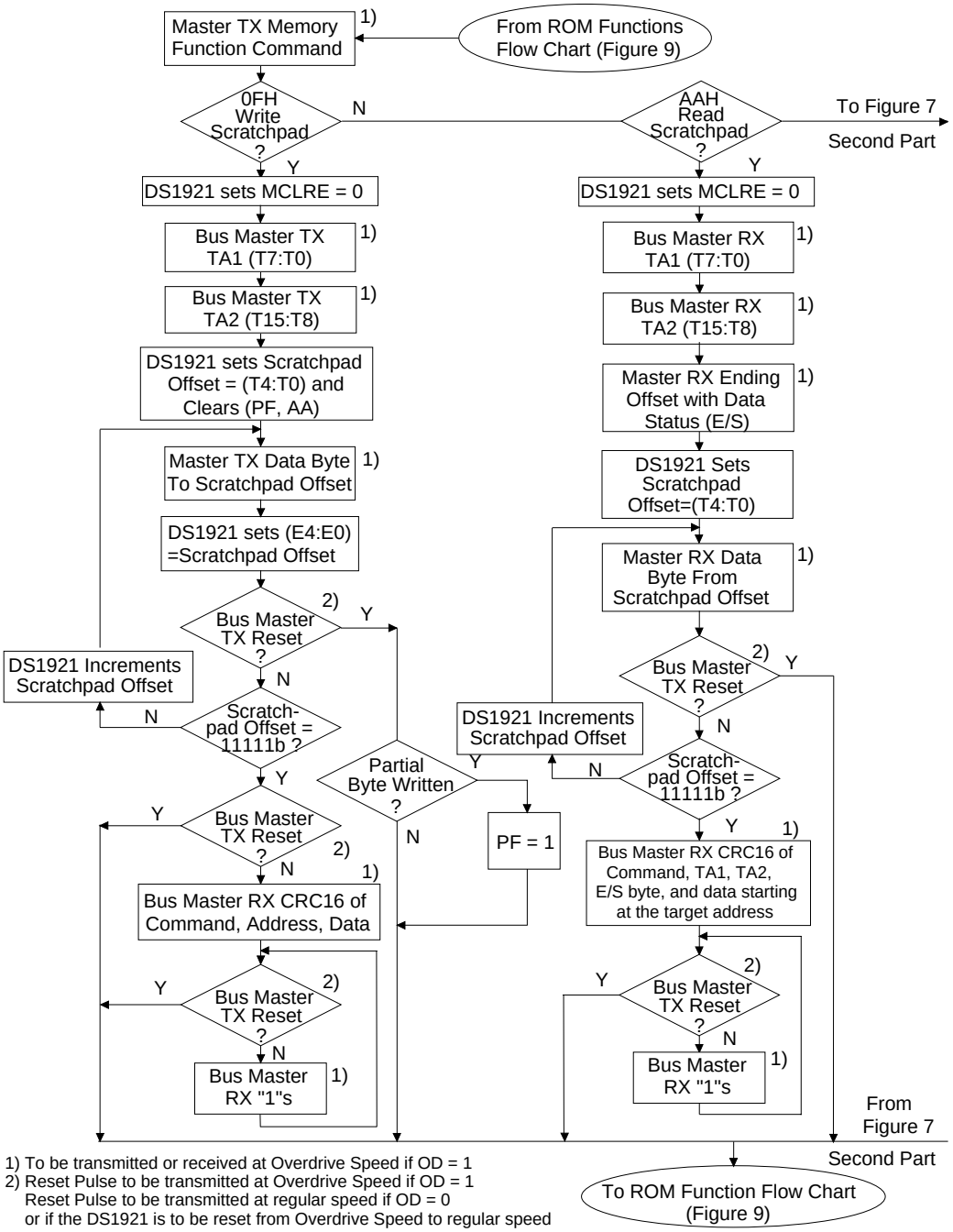
Clear Memory [3Ch]

The Clear Memory command is used to clear the memory address range from 220h and higher as well as the Sample Rate, Mission Start Delay, Mission Time Stamp, and Mission Samples Counter in the register page. The memory must be cleared for the device to be set up for another mission. For the Clear Memory command to function the MCLRE bit in Control Register must be set to 1. The Clear Memory command must be issued with the very next access to the device's memory functions ("timed access"). Issuing any other valid memory function command will reset the MCLRE bit. The Clear Memory command takes approximately 500 µs to complete and cannot be interrupted. However, it is possible to issue a reset/presence sequence, execute any ROM command and access the 4096 bits of user-RAM or read the real-time clock or Status Register while the Clear Memory command is in progress. As the Clear Memory command is completed the MEMCLR bit in the Status Register will read 1 and the MCLRE bit will be 0.

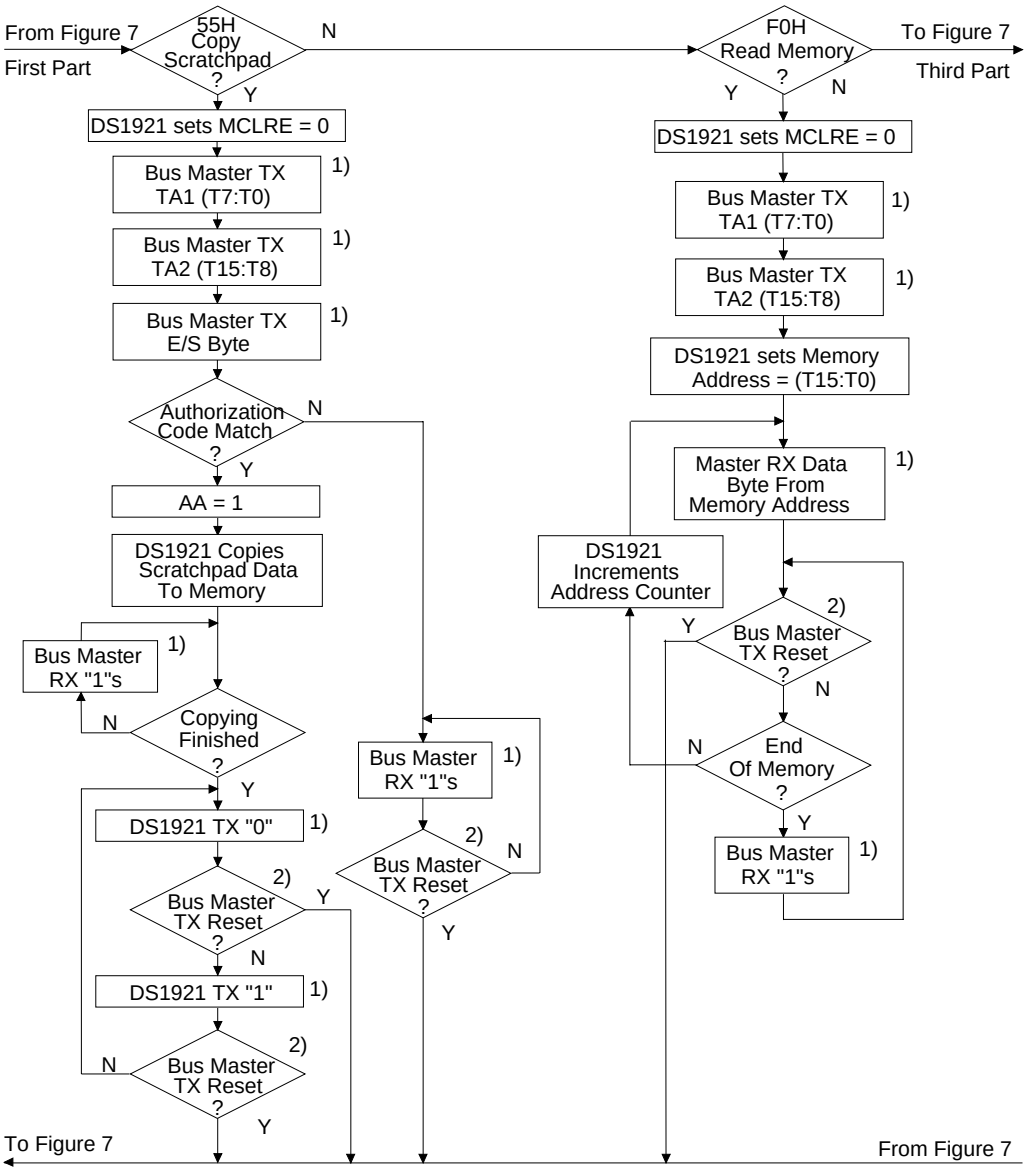
Convert Temperature [44h]

The Convert Temperature command can be issued if a mission is not in progress to measure the current temperature of the device. The result of the temperature conversion will be found at memory address 211h in the register page. This command takes approximately 750 ms to complete and cannot be interrupted. Memory access to any location of the device is possible while the temperature conversion takes place.

MEMORY FUNCTION FLOW CHART Figure 7

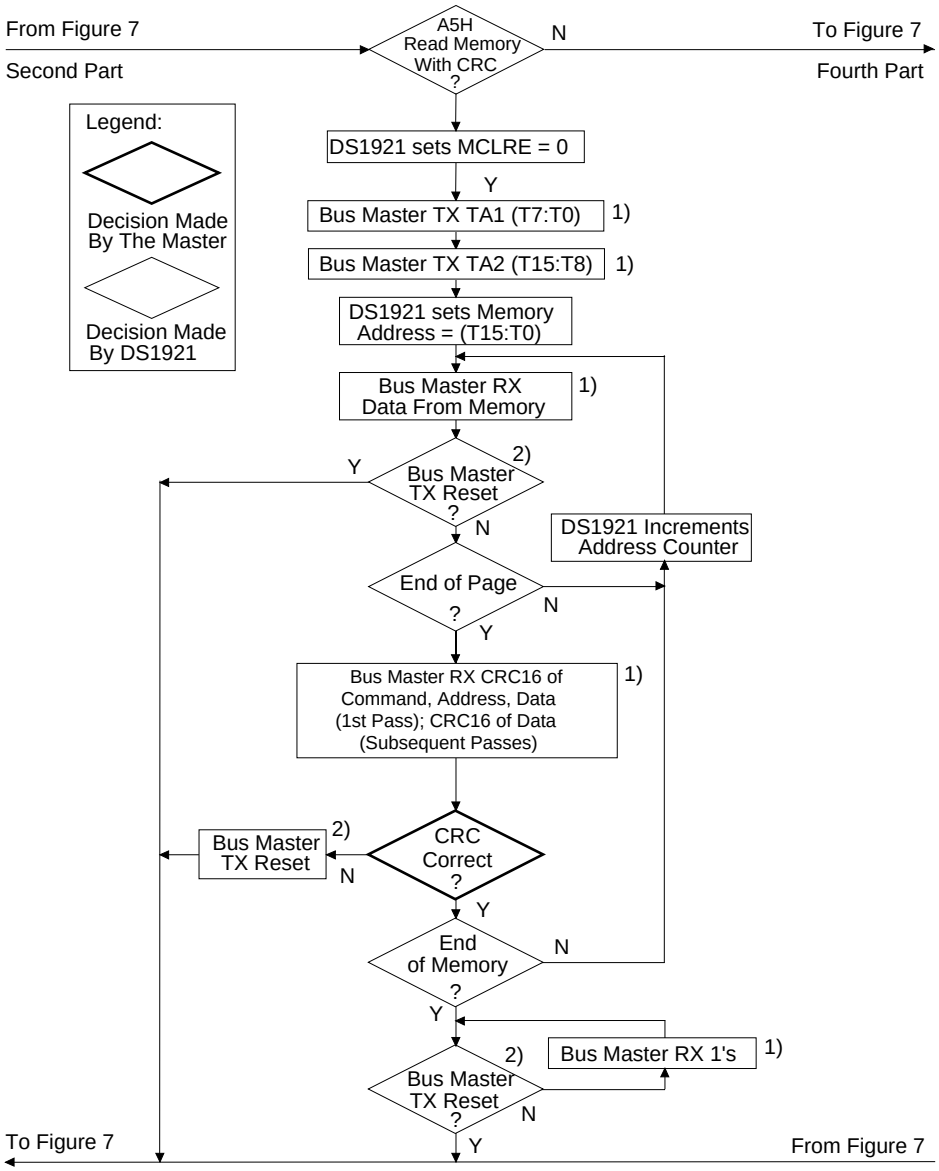


MEMORY FUNCTION FLOW CHART Figure 7 (cont'd)



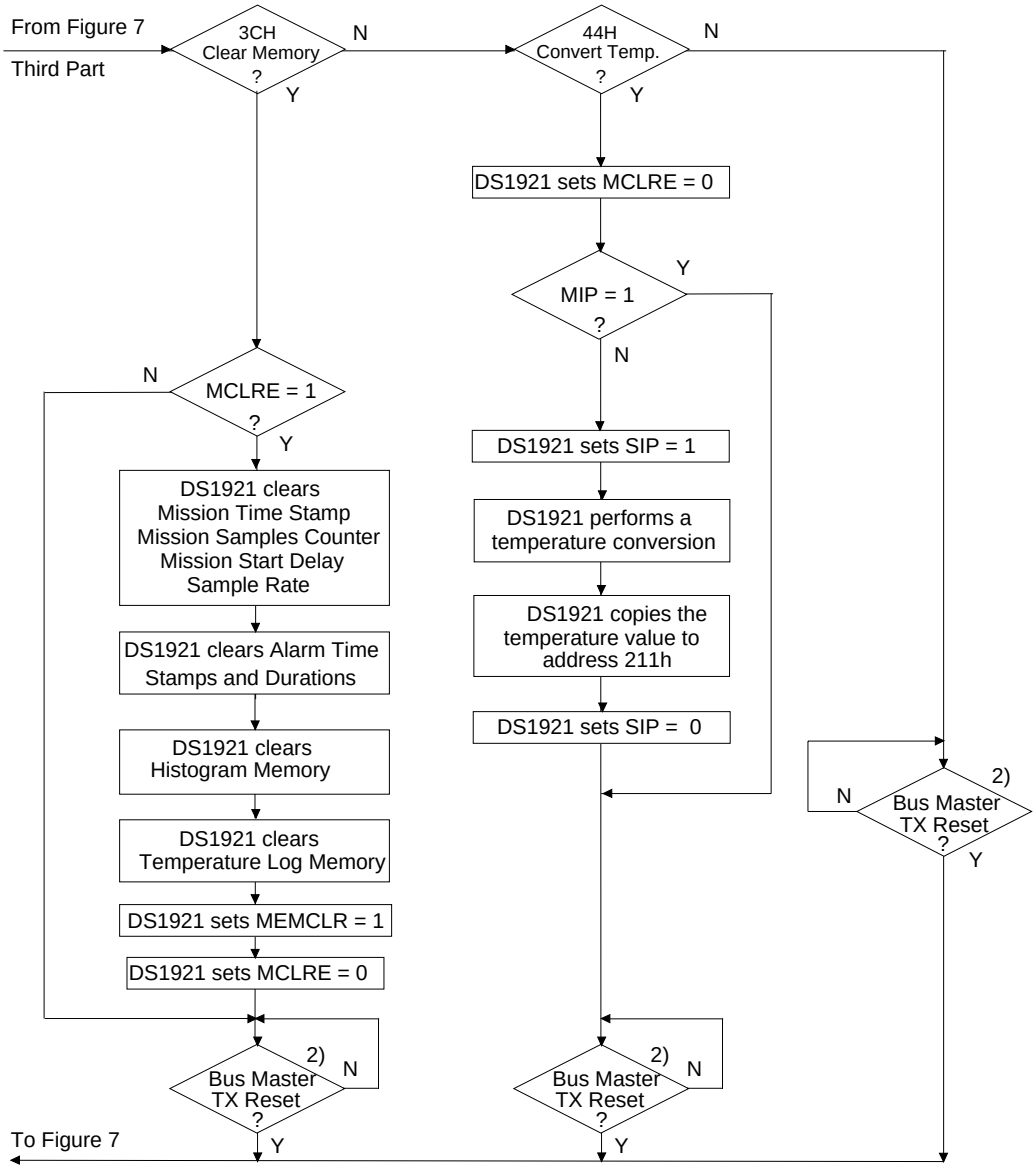
1) To be transmitted or received at Overdrive Speed if OD = 1
2) Reset Pulse to be transmitted at Overdrive Speed if OD = 1
Reset Pulse to be transmitted at regular speed if OD = 0
or if the DS1921 is to be reset from Overdrive Speed to regular speed

MEMORY FUNCTION FLOW CHART Figure 7 (cont'd)



1) To be transmitted or received at Overdrive Speed if OD = 1
2) Reset Pulse to be transmitted at Overdrive Speed if OD = 1
Reset Pulse to be transmitted at regular speed if OD = 0
or if the DS1921 is to be reset from Overdrive Speed to regular speed

MEMORY FUNCTION FLOW CHART Figure 7 (cont'd)



1) To be transmitted or received at Overdrive Speed if OD = 1
2) Reset Pulse to be transmitted at Overdrive Speed if OD = 1
Reset Pulse to be transmitted at regular speed if OD = 0
or if the DS1921 is to be reset from Overdrive Speed to regular speed

1-WIRE BUS SYSTEM

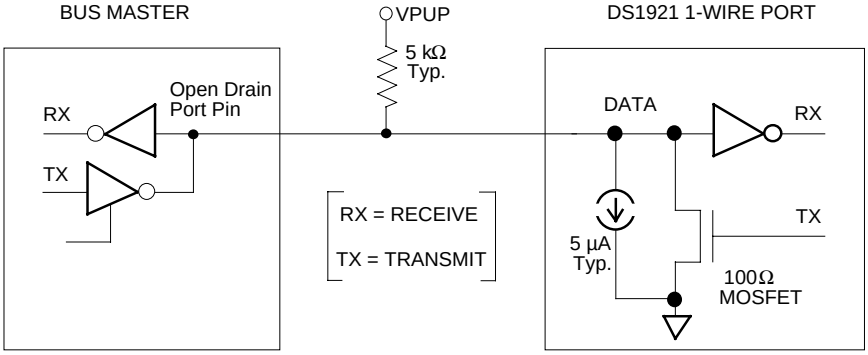
The 1-Wire bus is a system which has a single bus master and one or more slaves. In all instances the DS1921 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). A 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx iButton Standards.

HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain or three-state outputs. The 1-Wire port of the DS1921 is open-drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. At regular speed the 1-Wire bus has a maximum data rate of 16.3 kbits per second. The speed can be boosted to 142 kbits per second by activating the Overdrive mode. The 1-Wire bus requires a pullup resistor of approximately 5 kΩ.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16 µs (Overdrive speed) or more than 120 µs (regular speed), one or more devices on the bus may be reset.

HARDWARE CONFIGURATION Figure 8



TRANSACTION SEQUENCE

The protocol for accessing the DS1921 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS1921 is on the bus and is ready to operate. For more details, see the "1-Wire Signaling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the seven ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure 9).

Read ROM [33h]

This command allows the bus master to read the DS1921's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS1921 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The resultant family code and 48-bit serial number will result in a mismatch of the CRC.

Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS1921 on a multidrop bus. Only the DS1921 that exactly matches the 64-bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a Read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired-AND result).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The Search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The search ROM process is the repetition of a simple three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, three-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx iButton Standards for a comprehensive discussion of a search ROM, including an actual example.

Conditional Search [ECh]

The Conditional Search ROM command operates similarly to the Search ROM command except that only devices fulfilling the specified condition will participate in the search. The condition is specified by the bit functions TAS, THS and TLS in the Control Register, address 20Eh. The Conditional Search ROM provides an efficient means for the bus master to determine devices on a multidrop system that have to signal an important event, such as a temperature leaving the tolerance band. After each pass of the conditional search that successfully determined the 64-bit ROM for a specific device on the multidrop bus, that particular device can be individually accessed as if a Match ROM had been issued, since all other devices will have dropped out of the search process and will be waiting for a reset pulse.

For the conditional search, one can select any combination of the three search conditions by writing the associated bit to a logical 1. These bits correspond directly to the flags in the Status Register of the device. If the flag in the status register reads 1 AND the corresponding bit in the Control Register is a logical 1, too, the device will respond to the Conditional Search command. If more than one bit search condition is selected, the first event occurring will make the device respond to the Conditional Search command.

Overdrive Skip ROM [3Ch]

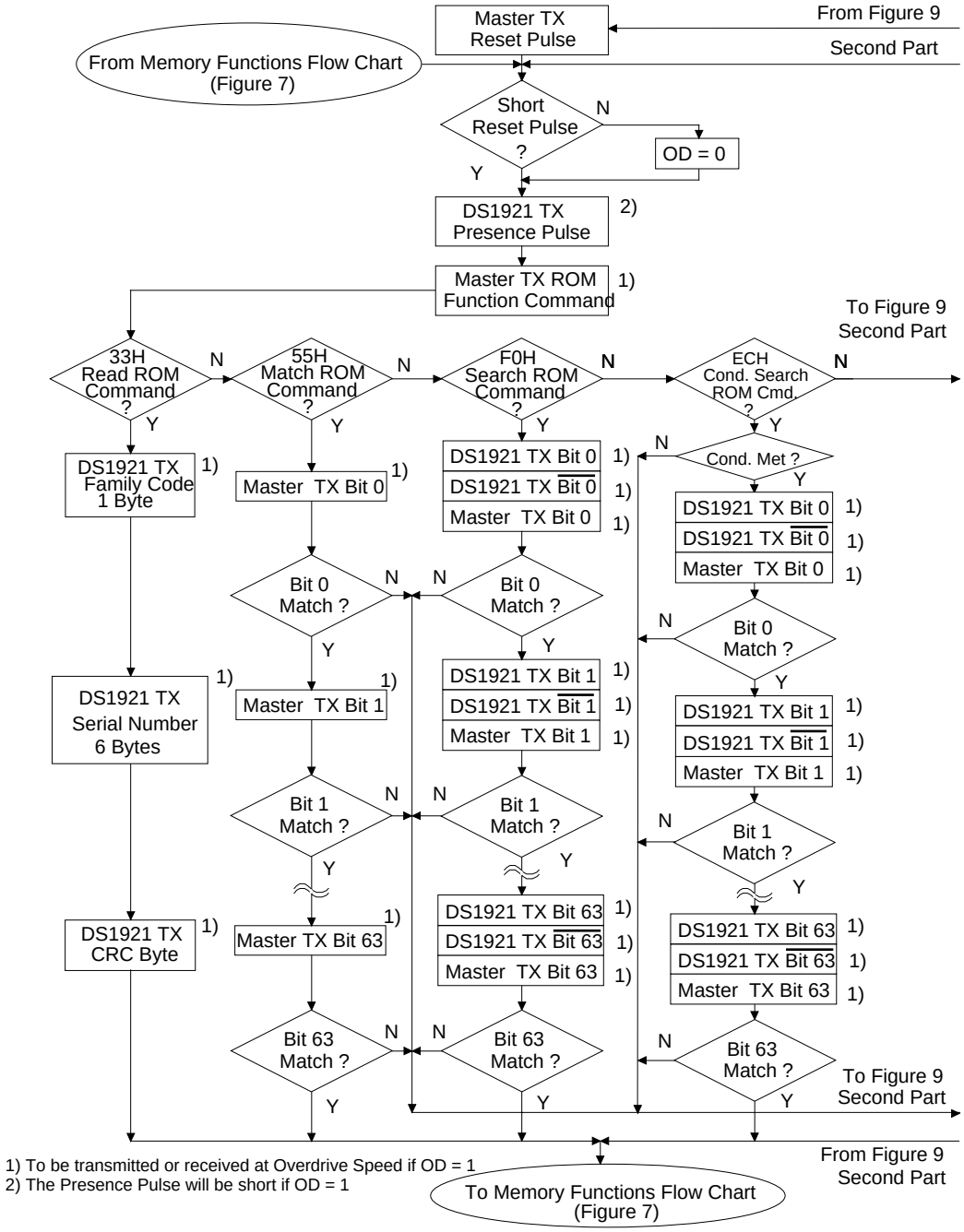
On a single-drop bus this command can save time by allowing the bus master to access the memory functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command, the Overdrive Skip ROM sets the DS1921 in the Overdrive mode (OD = 1). All communication following this command has to occur at Overdrive speed until a reset pulse of minimum 480 µs duration resets all devices on the bus to regular speed (OD = 0).

When issued on a multidrop bus this command will set all Overdrive-supporting devices into Overdrive mode. To subsequently address a specific Overdrive-supporting device, a reset pulse at Overdrive speed has to be issued followed by a Match ROM or Search ROM command sequence. This will speed up the time for the search process. If more than one slave supporting Overdrive is present on the bus and the Overdrive Skip ROM command is followed by a Read command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired-AND result).

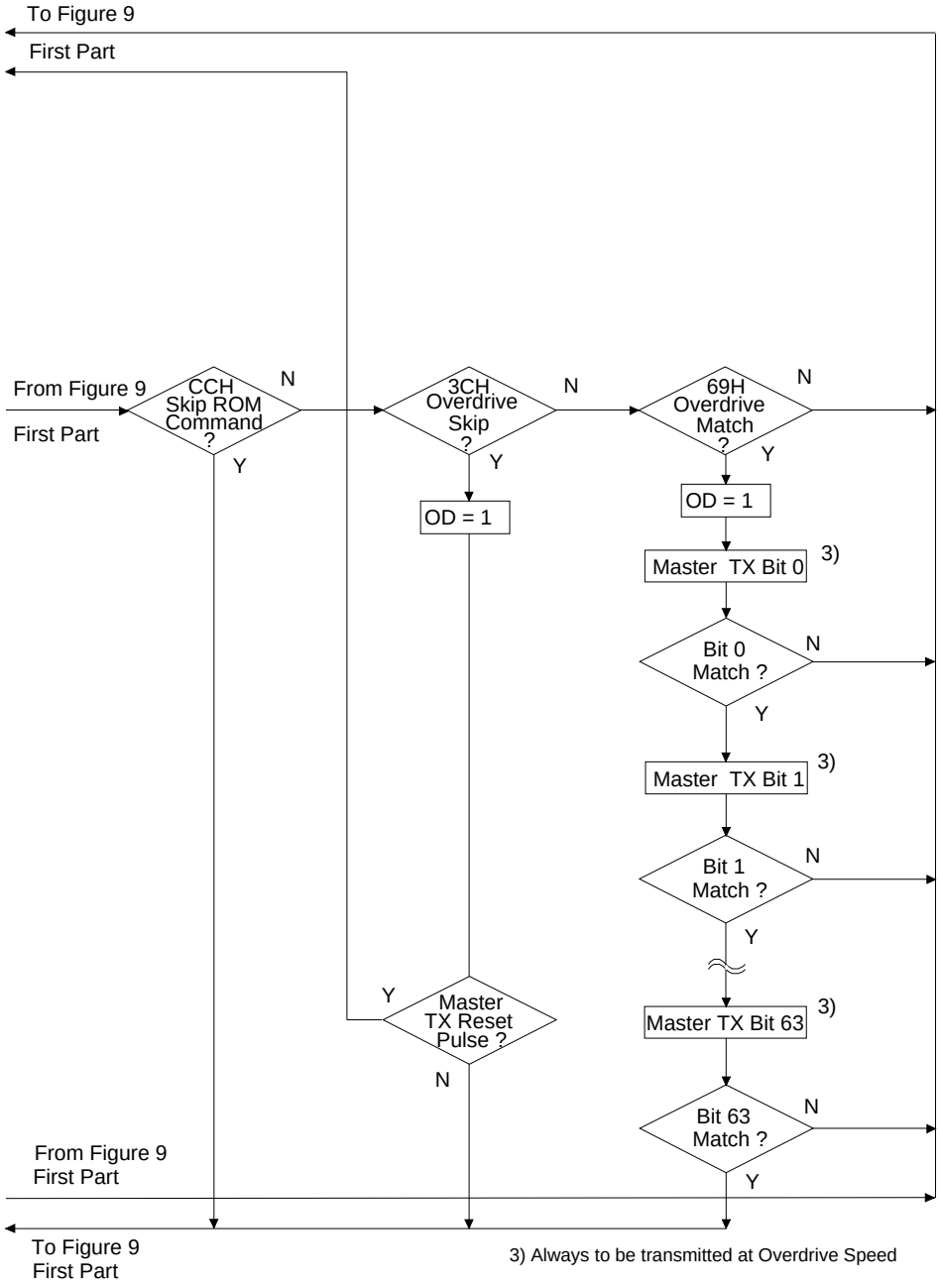
Overdrive Match ROM [69h]

The Overdrive Match ROM command followed by a 64-bit ROM sequence transmitted at Overdrive Speed allows the bus master to address a specific DS1921 on a multidrop bus and to simultaneously set it in Overdrive mode. Only the DS1921 that exactly matches the 64-bit ROM sequence will respond to the subsequent memory function command. Slaves already in Overdrive mode from a previous Overdrive Skip or Match command will remain in Overdrive mode. All overdrive-capable slaves will return to regular speed at the next Reset Pulse of minimum 480 µs duration. The Overdrive Match ROM command can be used with a single or multiple devices on the bus.

ROM FUNCTIONS FLOW CHART Figure 9



ROM FUNCTIONS FLOW CHART Figure 9 (cont'd)



MISSION EXAMPLE: PREPARE AND START A NEW MISSION

Assumption: The previous mission has come to an end. To end an ongoing mission one may, for example, perform a sequence as in step 1 or write the MIP bit in the Status Register to 0.

The preparation of the DS1921 for a mission including the start of the mission requires up to four steps:

Step 1: set the real-time clock (if it needs to be adjusted)
Step 2: clear the data of the previous mission
Step 3: set the search condition and mission start delay
Step 4: set the temperature alarms and write the sample rate to start the mission

STEP 1

Let the actual time be 15:30:00 hours on Wednesday, the 7th of April in 1999. This results in the following data to be written to the real-time clock registers:

Address:	200h	201h	202h	203h	204h	205h	206h
Data:	00h	30h	15h	03h	07h	04h	99

With only a single DS1921 connected to the bus master, the communication of step 1 looks like this:

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480-960 µs)
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	0Fh	Issue “write scratchpad” command
TX	00h	TA1, beginning offset=00h
TX	02h	TA2, address=0200h
TX	<7 data bytes>	Write 7 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	AAh	Issue “read scratchpad” command
RX	00h	Read TA1, beginning offset=00h
RX	02h	Read TA2, address=0200h
RX	06h	Read E/S, ending offset=6h, flags=0h
RX	<7 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	55h	Issue “copy scratchpad” command
TX	00h	TA1
TX	02h	TA2 AUTHORIZATION CODE
TX	06h	E/S
TX	Reset	Reset pulse
RX	Presence	Presence pulse

STEP 2

Set the MCLRE bit to 1, enable the real-time clock and then execute the Clear Memory command. This results in the following data to be written to the Status Register:

Address:	20Eh
Data:	40h

With only a single DS1921 connected to the bus master, the communication of step 2 looks like this:

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480-960 µs)
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	0Fh	Issue “write scratchpad” command
TX	0Eh	TA1, beginning offset=0Eh
TX	02h	TA2, address=020Eh
TX	40h	Write status byte to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue "skip ROM" command
TX	AAh	Issue “read scratchpad” command
RX	0Eh	Read TA1, beginning offset=0Eh
RX	02h	Read TA2, address=020Eh
RX	0Eh	Read E/S, ending offset = 0Eh, flags = 0h
RX	40h	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	55h	Issue “copy scratchpad” command
TX	0Eh	TA1
TX	02h	TA2 AUTHORIZATION CODE
TX	0Eh	E/S
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	3Ch	Issue “clear memory” command
TX	Reset	Reset pulse
RX	Presence	Presence pulse

STEP 3

In this example the rollover is disabled and the search condition is set for a high temperature only. The mission is to start with a delay of 90 (5Ah) minutes. This results in the following data to be written to the special function registers:

Address:	20Eh	20Fh	210h	211h	212h	213h
Data:	02h	00*	00*	00*	5Ah	00

* Writing through address locations 20Fh to 211h is faster than accessing the Mission Start Delay Register in a separate cycle. The write attempt has no effect on the contents of these registers.

With only a single DS1921 connected to the bus master, the communication of step 3 looks like this:

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset Pulse (480-960 µs)
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	0Fh	Issue “write scratchpad” command
TX	0Eh	TA1, beginning offset=0Eh
TX	02h	TA2, address=020Eh
TX	<6 data bytes>	Write 6 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	AAh	Issue “read scratchpad” command
RX	0Eh	Read TA1, beginning offset=0Eh
RX	02h	Read TA2, address=020Eh
RX	13h	Read E/S, ending offset=13h, flags=0h
RX	<6 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	55h	Issue “copy scratchpad” command
TX	0Eh	TA1
TX	02h	TA2 AUTHORIZATION CODE
TX	13h	E/S
TX	Reset	Reset pulse
RX	Presence	Presence pulse

STEP 4

In this example the temperature alarms are set to -5°C for the low temperature threshold and 0°C for the high temperature threshold. The sample rate is once every 10 minutes, allowing the mission to last up to 14 days. This results in the following data to be written to the special function registers:

Address:	20Bh	20Ch	20Dh
Data:	46h	50h	0Ah

With only a single DS1921 connected to the bus master, the communication of step 4 looks like this:

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480-960 µs)
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	0Fh	Issue “write scratchpad” command
TX	0Bh	TA1, beginning offset=0Bh
TX	02h	TA2, address=020Bh
TX	<3 data bytes>	Write 3 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	AAh	Issue “read scratchpad” command
RX	0Bh	Read TA1, beginning offset=0Bh
RX	02h	Read TA2, address=020Bh
RX	0Dh	Read E/S, ending offset=0Dh, flags=0h
RX	<3 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	CCh	Issue “skip ROM” command
TX	55h	Issue “copy scratchpad” command
TX	0Bh	TA1
TX	02h	TA2 AUTHORIZATION CODE
TX	0Dh	E/S
TX	Reset	Reset pulse
RX	Presence	Presence pulse

If step 4 was successful, the Mission Time Stamp Register will contain the date and time of the real-time clock, the MIP bit in the Status Register will be 1 and the MEMCLR bit will be 0.

1-WIRE SIGNALING

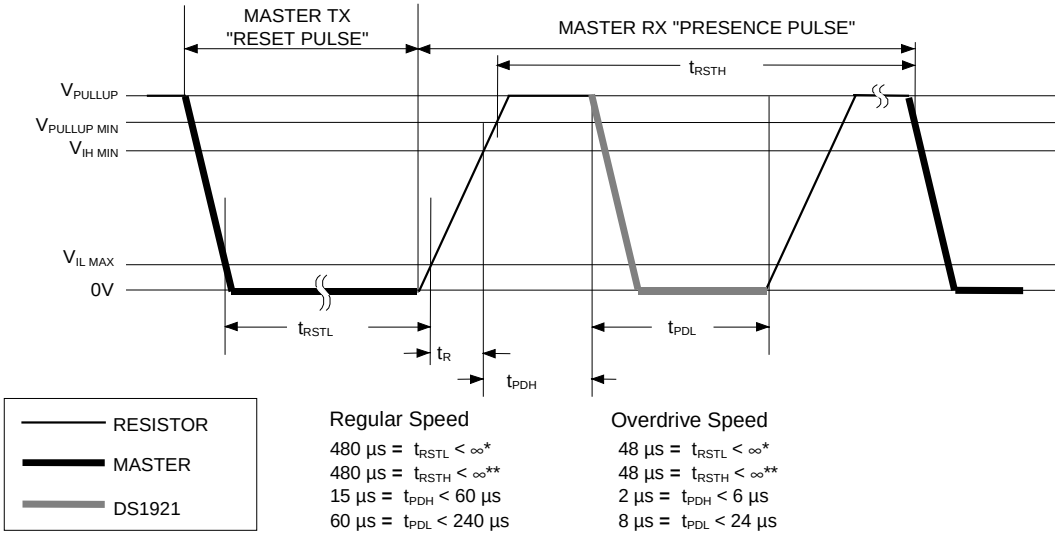
The DS1921 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1 and Read Data. All these signals except presence pulse are initiated by the bus master. The DS1921 can communicate at two different speeds, regular speed and Overdrive speed. If not explicitly set into the Overdrive mode, the DS1921 will communicate at regular speed. While in Overdrive mode the fast timing applies to all waveforms.

The initialization sequence required to begin any communication with the DS1921 is shown in Figure 10. A reset pulse followed by a presence pulse indicates the DS1921 is ready to send or receive data, given the correct ROM command and memory function command. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480 µs at regular speed, 48 µs at Overdrive speed). The bus master then releases the line and goes into receive mode (RX). The 1-Wire bus is pulled to a high state via the pullup resistor. After detecting the rising edge on the data pin, the DS1921 waits (t_{PDH}, 15-60 µs at regular speed, 2-6 µs at Overdrive speed) and then transmits the presence pulse (t_{PDL}, 60-240 µs at regular speed, 8-24 µs at Overdrive speed). A reset pulse of 480 µs or longer will exit the Overdrive mode, returning the device to regular speed. If the DS1921 is in Overdrive mode and the reset pulse is no longer than 80 µs, the device will remain in Overdrive mode.

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 11. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS1921 to the master by triggering a delay circuit in the DS1921. During write time slots, the delay circuit determines when the DS1921 will sample the data line. For a read data time slot, if a 0 is to be transmitted, the delay circuit determines how long the DS1921 will hold the data line low overriding the 1 generated by the master. If the data bit is a 1, the device will leave the read data time slot unchanged.

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 10

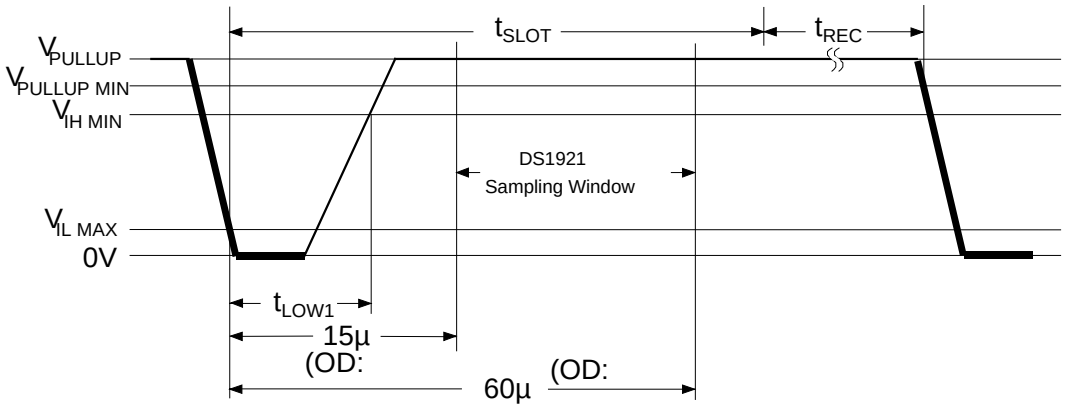


* In order not to mask interrupt signalling by other devices on the 1-Wire bus, $t_{RSTL} + t_R$ should always be less than 960 µs

** includes recovery time

READ/WRITE TIME DIAGRAM Figure 11

Write-one Time Slot



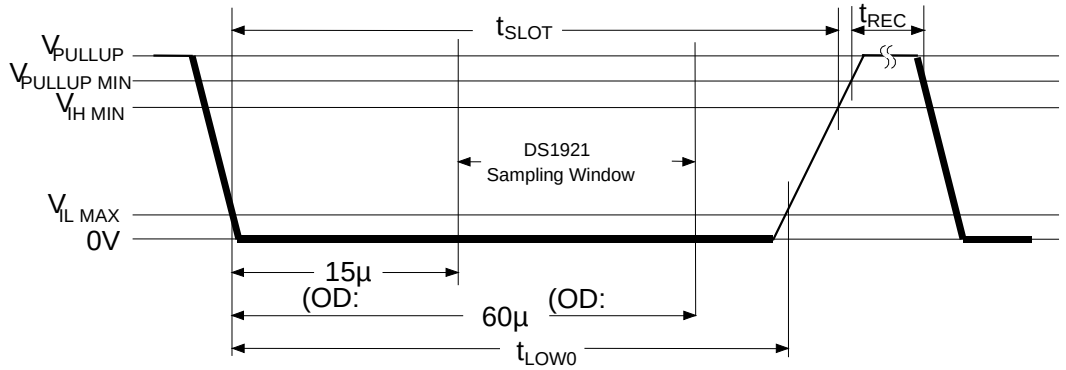
REGULAR SPEED

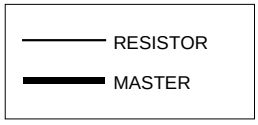
60 µs = tSLOT < 120 µs
1 µs = tLOW1 < 15 µs
1 µs = tREC < 8

OVERDRIVE SPEED

6 µs = tSLOT < 16 µs
1 µs = tLOW1 < 2 µs
1 µs = tREC < 8

Write-zero Time Slot





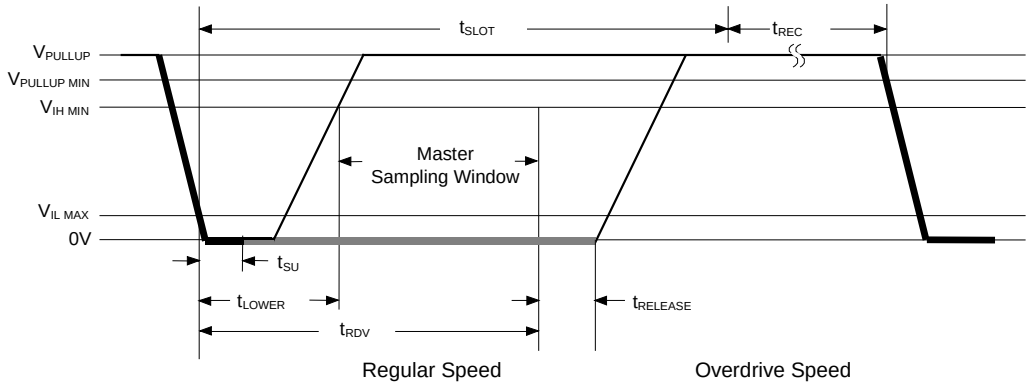
REGULAR SPEED

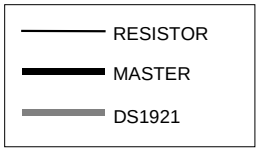
60 µs = tLOW0 < tSLOT < 120 µs
1 µs = tREC < 8

OVERDRIVE SPEED

6 µs = tLOW0 < tSLOT < 16 µs
1 µs = tREC < 8

Read-data Time Slot





Regular Speed

60 µs ≤ t_{SLOT} < 120 µs
1 µs ≤ t_{LOWER} < 15 µs
0 µs ≤ $t_{RELEASE}$ < 45 µs
1 µs ≤ t_{REC} < ∞
t_{RDV} = 45 µs
t_{SU} < 1 µs

Overdrive Speed

6 µs ≤ t_{SLOT} < 16 µs
1 µs ≤ t_{LOWER} < 2 µs
0 µs ≤ $t_{RELEASE}$ < 4 µs
1 µs ≤ t_{REC} < ∞
t_{RDV} = 2 µs
t_{SU} < 1 µs

CRC GENERATION

With the DS1921 there are two different types of CRCs (Cyclic Redundancy Checks). One CRC is an 8-bit type and is stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM and compare it to the value stored within the DS1921 to determine if the ROM data has been received error-free by the bus master. The equivalent polynomial function of this CRC is: $X^8 + X^5 + X^4 + 1$. This 8-bit CRC is received in the true (non-inverted) form when reading the ROM of the DS1921. It is computed at the factory and lasered into the ROM.

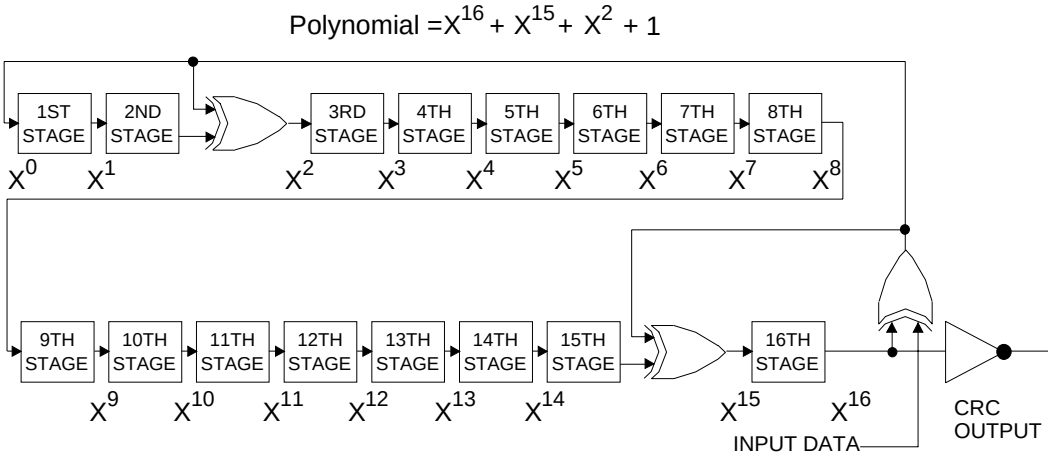
The other CRC is a 16-bit type, generated according to the standardized CRC16-polynomial function $x^{16} + x^{15} + x^2 + 1$. This CRC is used for error detection when reading data memory using the Read Memory with CRC command and for fast verification of a data transfer when writing to or reading from the scratchpad. It is the same type of CRC as is used with NV RAM-based iButtons for error detection within the iButton Extended File Structure. In contrast to the 8-bit CRC, the 16-bit CRC is always returned or sent in the complemented (inverted) form. A CRC-generator inside the DS1921 chip (Figure 12) will calculate a new 16-bit CRC as shown in the command flow chart of Figure 7. The bus master compares the CRC value read from the device to the one it calculates from the data and decides whether to continue with an operation or to reread the portion of the data with the CRC error. With the initial pass through the Read Memory with CRC flow chart, the 16-bit CRC value is the result of shifting the command byte into the cleared CRC generator, followed by the 2 address bytes and the data bytes. Subsequent passes through the Read Memory with CRC flow chart will generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the data bytes.

With the Write Scratchpad command the CRC is generated by first clearing the CRC generator and then shifting in the command code, the Target Addresses TA1 and TA2 and all the data bytes. The DS1921 will transmit this CRC only if the data bytes written to the scratchpad include scratchpad ending offset 11111b. The data may start at any location within the scratchpad.

With the Read Scratchpad command the CRC is generated by first clearing the CRC generator and then shifting in the command code, the Target Addresses TA1 and TA2, the E/S byte, and the scratchpad data starting at the target address. The DS1921 will transmit this CRC only if the reading continues through the end of the scratchpad, regardless of the actual ending offset.

For more details on generating CRC values, including example implementations in both hardware and software, see the “Book of DS19xx iButton Standards.”

CRC-16 HARDWARE DESCRIPTION AND POLYNOMIAL Figure 12



PHYSICAL SPECIFICATION

Size	See mechanical drawing
Weight	3.3 grams
Humidity	90% RH at 50°C
Altitude	10,000 feet
Expected Service Life	10 years at 25°C
Safety	Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, approval under Entity Concept for use in Class I, Division 1, Group A, B, C and D Locations (application pending)

ABSOLUTE MAXIMUM RATINGS*

Voltage on DATA to Ground -0.5V to +6.0V
Operating and Storage Temperature -40°C to +85°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability. This devices must not be exposed to temperatures over 70°C for extended time periods.

DC ELECTRICAL CHARACTERISTICS (VPUP=2.8V to 6.0V; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2			V	1, 8
Logic 0	V_{IL}	-0.3		+0.8	V	1, 9
Output Logic Low @ 4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Load Current	I_L		5		µA	3
Battery Life Time (Samples)	N_S		2500000		-----	10

CAPACITANCE (TA = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	$C_{IN/OUT}$		100	800	pF	6

AC ELECTRICAL CHARACTERISTICS REGULAR SPEED (VPUP=2.8V to 6.0V; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write-1 Low Time	t_{LOW1}	1		15	µs	
Write-0 Low Time	t_{LOW0}	60		120	µs	
Read Low Time	t_{LOWR}	1		15	µs	
Read Data Valid	t_{RDV}	exactly 15			µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480			µs	7
Presence Detect High	t_{PDH}	15		60	µs	
Presence Detect Low	t_{PDL}	60		240	µs	

AC ELECTRICAL CHARACTERISTICS
OVERDRIVE SPEED (VPUP=2.8V to 6.0V; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		16	µs	
Write-1 Low Time	t_{LOW1}	1		2	µs	
Write-0 Low Time	t_{LOW0}	60		16	µs	
Read Low Time	t_{LOWR}	1		2	µs	
Read Data Valid	t_{RDV}	exactly 2			µs	
Release Time	$t_{RELEASE}$	0	1.5	4	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	48			µs	4
Reset Time Low	t_{RSTL}	48		80	µs	
Presence Detect High	t_{PDHIGH}	2		6	µs	
Presence Detect Low	t_{PDLOW}	8		24	µs	

ROM ENCODING vs RANGE OF ACCURATE OPERATIONS

The most significant 12 bits of the 48-bit serial number are being used in the DS1921L-F5X Thermochron product series to identify both the lower limit and the range of accurate operations, as elaborated below. Software developers may use this coding mechanism to automatically determine the validity of sampled temperature values based on the content of this 12-bit field.

PART NUMBER	RANGE OF ACCURATE OPERATIONS	S/N 48 BITS ENCODEING	FAMILY CODE
DS1921L-F51	-10°C to +85°C	34Cxxxxxxxxx	21
DS1921L-F52	-20°C to +85°C	254xxxxxxxxx	21
DS1921L-F53	-30°C to +85°C	15Cxxxxxxxxx	21
DS1921L-F50	-40°C to +85°C	064xxxxxxxxx	21

The custom ROM coding mechanism reflects both the lower limit and the operating range of the Thermochron iButton by combining coded representations of these two parameters. Each parameter is first represented by a 5-bit binary code according to the following equations:

Starting temperature mapping code:

$$C_{start} = (T_L + 40)/5$$

where T_L is the lower temperature limit of the specified accurate operation range.

Width of accurate operation range mapping code:

$$C_{range} = (T_U - T_L)/5$$

where T_L and T_U are respectively the lower and upper temperature limits of the specified accurate operation range.

For example, if a part's accurate operation range is –30°C to +85°C. The custom code 15Ch is determined as follows:

1) starting temperature -30 maps to a 5-bit binary code: $C_{start}=(-30+40)/5=2d=00010b$
2) operation range width 85-(-30) = 115 maps to a 5-bit binary code: $C_{range}=115/5=23d=10111b$
3) pad two 00 onto these two codes to make a 12-bit binary code: 00010 10111 00
4) in hex form the above 12-bit code becomes: 15C

NOTES:

1. All voltages are referenced to ground.

2. V_{PUP} = external pull-up voltage.

3. Input load is to ground.

4. An additional reset or communication sequence cannot begin until the reset high time has expired.

5. Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge.

1. Capacitance on the data pin could be 800 pF when power is first applied. If a 5 kΩ resistor is used to pull up the data line to V_{PUP}, 5 µs after power has been applied the parasite capacitance will not affect normal communications.

7. The reset low time (t_{RSTL}) should be restricted to a maximum of 960 µs to allow interrupt signaling; otherwise, it could mask or conceal interrupt pulses.

8. V_{IH} is a function of the external pull-up resistor and V_{PUP}.

9. Under certain low-voltage conditions V_{ILMAX} may have to be reduced to as much as 0.5V to always guarantee a presence pulse.

1. The number of temperature conversions (= Samples) possible with the built-in energy source depends on the operating and storage temperature of the device. When not in use for a mission, the device should be stored at a temperature not exceeding 25°C.

11. The 'CENT' bit in the 'Real Time Clock Registers' describes what century it is. The convention that the data sheet and our demo software uses is 19XX = 0 and 20XX = 1. There is no corresponding 'CENT' bit in the 'Mission Time Stamp' as might be expected. To compensate for this, the following logic has been implemented in the iButton Viewer and other examples:

```
IF 'CENT' in 'Mission Time Stamp' is 1 THEN
  century is 20
ELSE IF there is a mission ongoing THEN
       check century of mission start by calculating the century of ('Real Time Clock' - 'Sample Rate' *
       'Mission Samples Counter')
ELSE
  IF 'Mission Time Stamp'(years) <= 70 THEN
    century is 20
  ELSE
    century is 19
```

Note that the first condition (CENT = 1 in the Mission Time Stamp) will never be true for the current version of the DS1921. However, at some point in the future, there may be other versions of the DS1921 or similar products offered that copy the CENT bit from the RTC down to the Mission Time Stamp along with the rest of the RTC information. By implementing the logic outlined above, if that change does occur in the future there will be no need to update any code written up to that point.