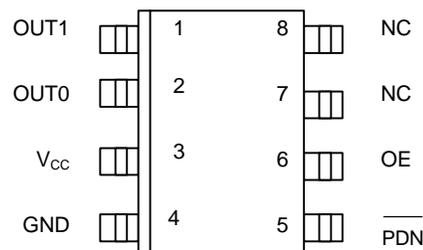**DALLAS**
SEMICONDUCTOR

DS1075 Custom
EconOscillator/Divider

www.dalsemi.com

FEATURES
- Dual Fixed frequency outputs (30 kHz - 100 MHz)
- No external components
- 0.5% Initial tolerance
- 1% variation over temperature and voltage
- Single 5V supply
- Power-down mode
- Synchronous output gating

OUT1	1	8 NC
OUT0	2	7 NC
V_{CC}	3	6 OE
GND	4	5 $\overline{PDN}$

DS1075Z 150-MIL SOIC
DS1075M 300-MIL DIP

DESCRIPTION
The DS1075 Custom is a fixed frequency oscillator requiring no external components for operation. Numerous operating frequencies are possible in the range 29.2 kHz to 100 MHz through the use of an on-chip factory-programmable prescaler and divider.

The DS1075 Custom is shipped from the factory pre-programmed on a custom basis to the customers specified output frequency and mode of operation. The part is branded according to the device's master frequency (see DS1075 data sheet). The customer fills out a "1075 Custom Order Form" with the required information and submits it to the factory for approval.

Custom EconOscillators are available in two versions, Simple Custom and Complex Custom, that can be programmed at the factory in sample and volume quantities.

Simple Custom parts are based on one of the standard master frequencies of 60, 66, 80 and 100 MHz with non-standard values programmed for the dividers and function select bits. An impressive number (over 1500) of sub-frequencies can be programmed using a Simple Custom part.

Complex Custom parts have a non-standard Master frequency (within the 60 MHz to 110 MHz range) programmed into the internal master oscillator and non-standard values are programmed for the dividers and function select bits. Virtually any frequency within the 29.24 kHz to 110 MHz range is possible using complex custom parts Contact the factory for Custom Part selection and ordering information.

The DS1075 Custom is available in 8-pin DIP or SOIC packages, allowing the generation of a clock signal easily, economically and using minimal board area.

091399

BLOCK DIAGRAM Figure 1
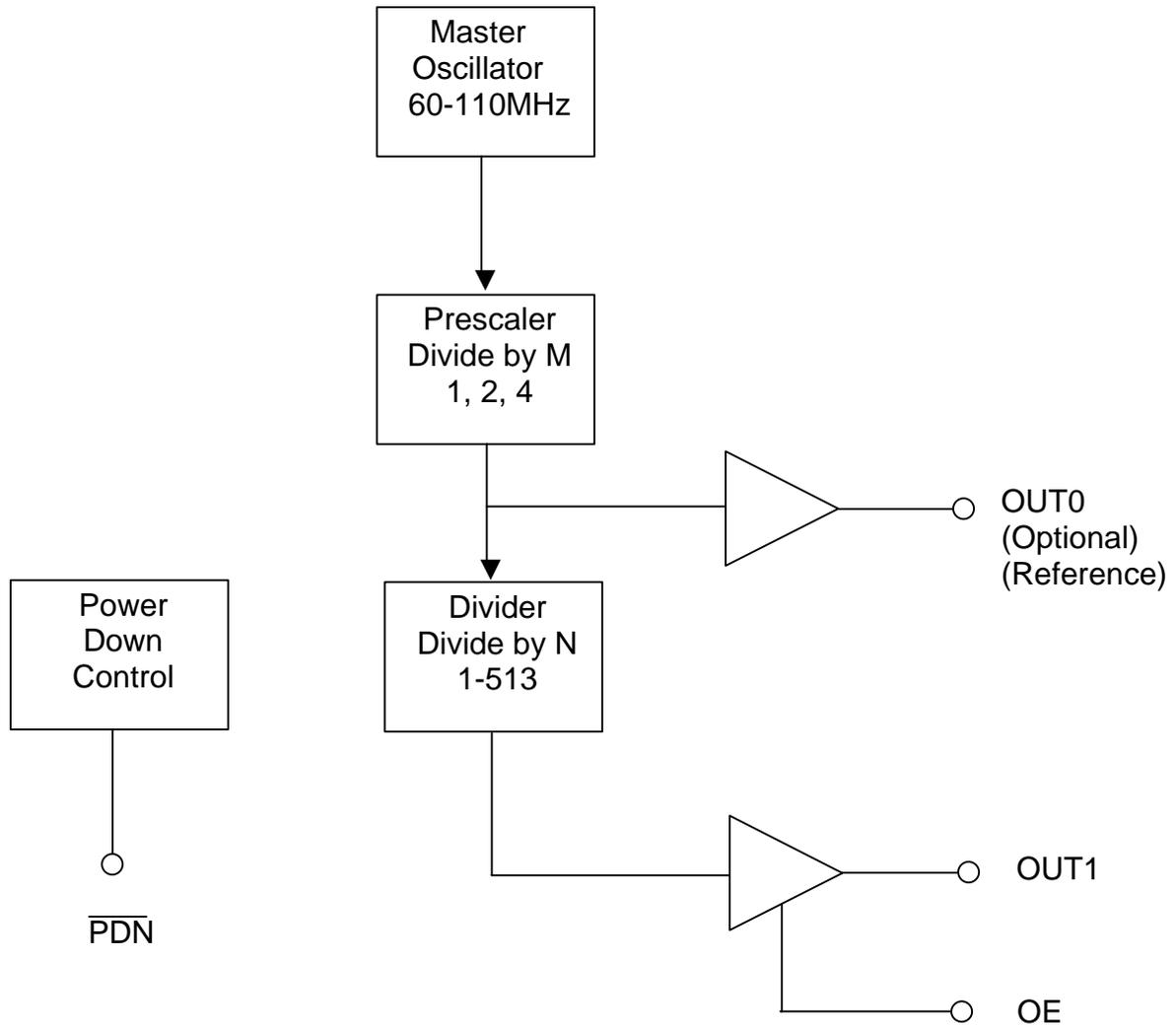
1075 Custom Order Form

Use this form for **DS1075 Custom programmed EconOscillators .** All sections must be completed.
Refer to the datasheet or contact Bob Brown at (972) 371-3719 for assistance.

Parent Part Number: <u>**DS1075**</u>

Customer Name: _____

Customer Contact: _____

Customer Address: _____

_____

Customer Phone: (Area) _____   _____   _____

Salesman: _____

Sales Representative: _____

Distributor (if any): _____

Package: 300mil 8-pin DIP   150mil 8-pin SOIC (circle one)

Parent Device: DS _____ (part will be branded with this speed)

Master Frequency: _____ **MHz**   **Standard   or   Custom** (circle one)
(60,66,80 or 100MHz)

Reference Output: ☐ Disabled   ☐ Enabled - Frequency _____
(Equals master frequency/M)

Output Frequency: _____   (Equals master frequency/MN)

Prescaler (M) :   _____   **Divider (N):** _____

Special Instructions (Tape & Reel, etc.):

_____

_____

_____

_____

_____

Customer Signature: _____
(acknowledges acceptance of custom settings)

Fax the completed form to Bob Brown at (972) 371-3717

PIN DESCRIPTIONS

Output Pin (OUT1 pin): This pin is the main oscillator output, with a frequency determined by clock reference, M and N dividers.

Output Enable Function (OE pin): The DS1075 Custom features a "synchronous" output enable. When OE is at a high logic level the oscillator free runs. When this pin is taken low OUT/ is held low, immediately if OUT/ is already low, or at the next high-to-low transition if OUT/ is high. This prevents any possible truncation of the output pulse width when the enable is used. While the output is disabled the master oscillator continues to run (producing an output at OUT0, if the $\overline{EN0}$ bit = 0) but the internal counters (/N) are reset. This results in a constant phase relationship between OE's return to a high level and the resulting OUT/ signal. When the enable is released OUT/ will make its first transition within one to two clock periods of the master clock.

Power-Down ($\overline{PDN}$ pin): A low logic level on this pin can be used to make the device stop oscillating (active low) and go into a reduced power consumption state. Internal "Enabling Sequencer" circuitry will first disable OUT in the same way as when OE is used. Next OUT0 will be disabled in a similar fashion. Finally the oscillator circuitry will be disabled. In this mode both outputs will go into a high impedance state. The power consumption in the power-down state is much less than if OE is used because the internal oscillator is completely powered down. Consequently the device will take considerably longer to recover (i.e., achieve stable oscillation) from a power-down condition than if the OE is used.

Reference Output (OUT0 pin): A reference output, OUT0, is also available from the output of the prescaler. OUT0 is unaffected by the OE pin, but is disabled in a glitchless fashion if the device is powered down. If this output is not required it can be permanently disabled and there will be a corresponding reduction in overall power consumption. The availability of this output and its frequency are specified on the custom order form.
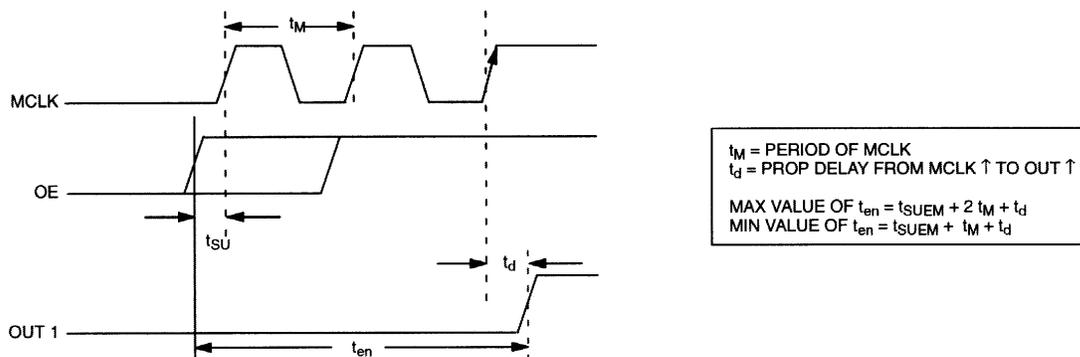
OPERATION OF OUTPUT ENABLE
Since the output enable and internal master oscillator are asynchronous there is the possibility of timing difficulties in the application. To minimize these difficulties the DS1075 features an "enabling sequencer" to produce predictable results when the device is enabled and disabled. In particular the output gating is configured so that truncated output pulses can never be produced.

ENABLE TIMING
The output enable function is produced by sampling the OE input with the output from the pre-scaler mux (MCLK) and gating this with the output from the programmable divider. The exact behavior of the device is therefore dependent on the setup time (t_{SU}) from a transition on the OE input to the rising edge of MCLK. If the actual setup time is less than t_{SUEM} then one more complete cycle of MCLK will be required to complete the enable or disable operation (see diagrams). This is unlikely to be of any consequence in most applications, and then only if the value for N is small. In general, the output will make its first positive transition between approximately one and two clock periods of MCLK after the rising edge of OE. (Figure 2)

Figure 2

t_M = PERIOD OF MCLK
t_d = PROP DELAY FROM MCLK ↑ TO OUT ↑

MAX VALUE OF t_{en} = t_{SUEM} + 2 t_M + t_d
MIN VALUE OF t_{en} = t_{SUEM} + t_M + t_d

Disable Timing

If OE goes low while OUT1 is high, the output will be disabled on the completion of the output pulse. If OUT1 is low, the disabling behavior will be dependent on the setup time between the falling edge of OE and the rising edge of MCLK. If t_{SU} < t_{SUEM} the result will be one additional pulse appearing on the output before disabling occurs.

If the device is in divide-by-one mode, the disabling occurs slightly differently. In this case if t_S > t_{SUEM} one additional output pulse will appear, if t_{SU} < t_{SUEM} then two additional output pulses will appear. The following diagrams illustrate the timing in each of these cases. (Figure 3 and 4)
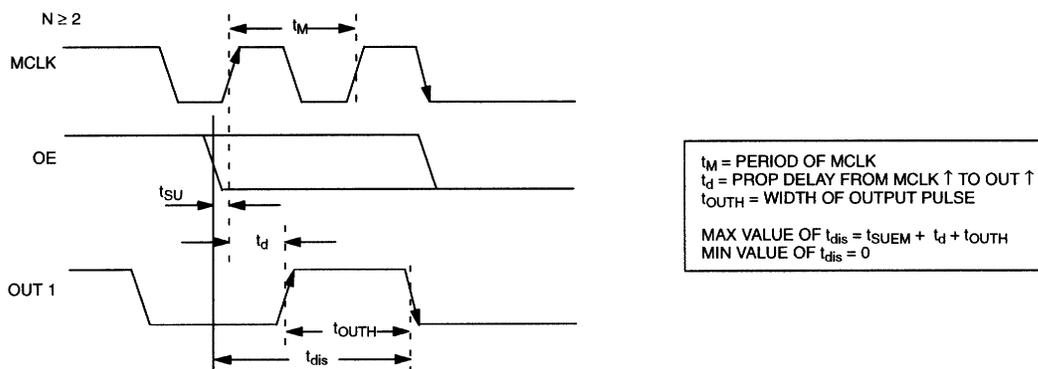
Figure 3

t_M = PERIOD OF MCLK
t_d = PROP DELAY FROM MCLK ↑ TO OUT ↑
t_{OUTH} = WIDTH OF OUTPUT PULSE

MAX VALUE OF t_{dis} = t_{SUEM} + t_d + t_{OUTH}
MIN VALUE OF t_{dis} = 0

Figure 4

t_M = PERIOD OF MCLK
t_d = PROP DELAY FROM MCLK ↑ TO OUT ↑
t_{OUTH} = WIDTH OF OUTPUT PULSE

MAX VALUE OF t_{dis} = t_{SUEM} + t_d + t_{OUTH} + t_M
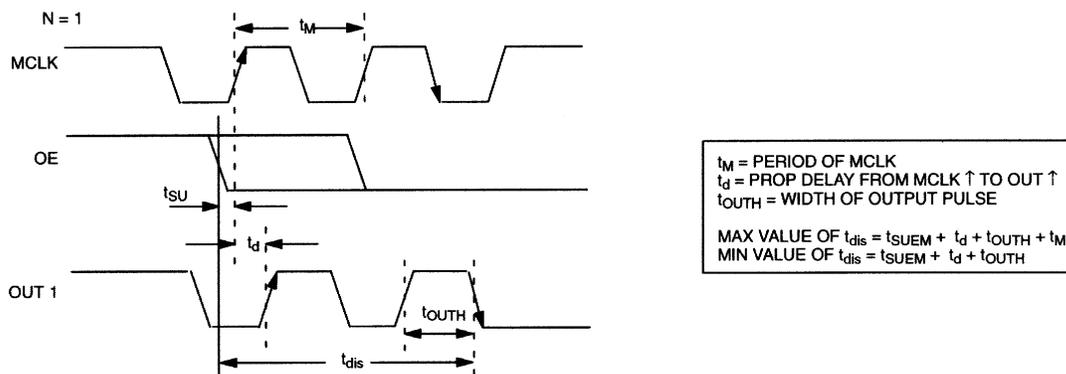MIN VALUE OF t_{dis} = t_{SUEM} + t_d + t_{OUTH}

POWER-DOWN CONTROL

POWER-DOWN

If $\overline{\text{PDN}}$ is taken low a power-down sequence is initiated. The "Enabling Sequencer" is used to execute events in the following sequence:

1. Disable OUT1 (same sequence as when OE is used) and reset N counters.

2. When OUT1 is low, switch OUT1 to high-impedance state.

3. Disable MCLK, switch OUT0 to high impedance state.

4. Disable master oscillator.

POWER-UP

When $\overline{\text{PDN}}$ is taken to a high level the following power-up sequence occurs:

1. Enable internal oscillator.

2. Set M and N to maximum values.

3. Wait approximately 256 cycles of MCLK for it to stabilize.

4. Reset M and N to programmed values.

5. Enable OUT0 (if enabled)

6. Enable OUT1.

Steps 2 through 4 exist to allow the oscillator to stabilize before enabling the outputs.

Figure 5
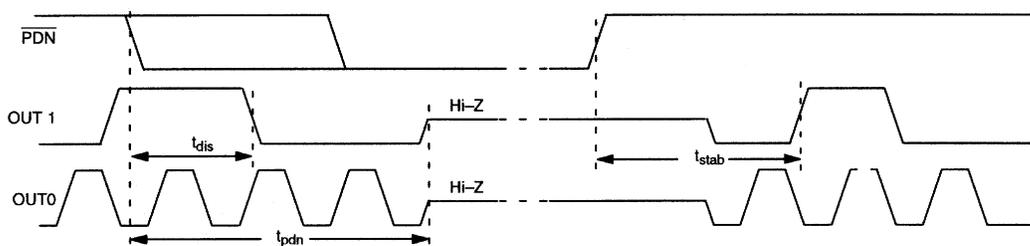
POWER-ON RESET

When power is initially applied to the device supply pin, a power-on reset sequence is executed, similar to that which occurs when the device is restored from a power-down condition. This sequence comprises two stages, first a conventional POR to initialize all on-chip circuitry, followed by a stabilization period to allow the oscillator to reach a stable frequency before enabling the outputs:

1. Initialize internal circuitry.

2. Enable internal oscillator.

3. Set M and N to maximum values.

4. Wait approximately 256 cycles of MCLK for the oscillator to stabilize.

5. Load M and N programmed values from EEPROM.

6. Enable OUT0 (if enabled).

7. Enable OUT1.

Figure 6
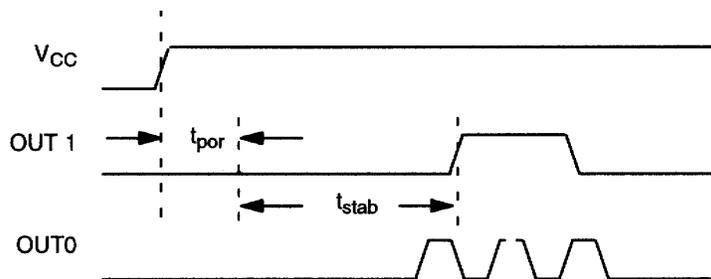
ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground   -1.0V to +7.0V
Operating Temperature   0°C to 70°C
Storage Temperature   -55°C to +125°C
Soldering Temperature   260°C for 10 seconds

∗   This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS   (T_A=0ºC to 70ºC; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5	5.25	V	
High-level Output Voltage (OUT1, OUT0)	V_{OH}	I_{OH}=-4 mA, V_{CC} = MIN	2.4			V	
Low-level Output Voltage (OUT1, OUT0)	V_{OL}	I_{OL}=4 mA			0.4	V	
High-level Input Voltage ($\overline{PDN}$, OE)	V_{IH} V_{IH}		2 3			V V	
Low-level Input Voltage ($\overline{PDN}$,OE)	V_{IL} V_{IL}				0.8 2	V V	
High-level Input Current ($\overline{PDN}$, OE)	I_{IH} I_{IH}	V_{IH}=2.4V, V_{CC}=5.25V V_{IH}=V_{CC}=5.25V			1 25	µA µA	
Low-level Input Current ($\overline{PDN}$, OE)	I_{IL} I_{IL}	V_{IL}=0, V_{CC}=5.25V V_{IL}=0,V_{CC} = 5.25V	-1 -25			µA µA	
Supply Current (Active) DS1075-100 DS1075-80 DS1075-66 DS1075-60	I_{CC}	C_L =15pF (both outputs) V_{CC}=5.25V			50	mA	
Standby Current	I_{CCQ}	Power-Down Mode		0.8		µA	

AC ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Output Frequency Tolerance	$?f_O$	V_{CC}=5V, T_A=25°C	-0.5	0	+0.5	%	
Combined Freq. Variation	$?f_O$	Over temp and voltage	-1		+1	%	
Long Term Stability	$?f_O$		-0.5		+0.5	%	
Minimum Output Frequency	f_{OUT}	Master = 60MHz M=4, N-513	29.24			KHz	
Power-up Time	$t_{por}+t_{stab}$			0.1	1	ms	1, 2
Enable OUT1 from $\overline{PDN}\uparrow$	t_{stab}			0.1	1	ms	2
Enable OUT0 from $\overline{PDN}\uparrow$	t_{stab}			0.1	1	ms	2, 3
OUT1 Hi-Z from $\overline{PDN}\downarrow$	t_{pdn}				1	ms	
OUT0 Hi-Z from $\overline{PDN}\downarrow$	t_{pdn}				1	ms	
Load Capacitance (OUT1, OUT0)	C_L			15		pF	4
Output Duty Cycle OUT1 OUT0			40		60	%	

NOTES:

1. This is the time from when V_{CC} is applied until the output starts oscillating

2. When the device is initially powered up, or restored from the power-down mode, OE should be asserted (high).Otherwise the start of the t_{stab} interval will be delayed until OE goes high. OE can subsequently be returned to a low level during the t_{stab} interval to force out low after the t_{stab} interval.

3. Although OE does not normally affect OUT0 operation, if OE is held low during power-up the start of the t_{stab} period will be delayed until OE is asserted. If OE remains low, OUT0 will not start.

4. Operation with higher capacitive loads is possible but may impair output voltage swing and maximum operation frequency.

AC ELECTRICAL CHARACTERISTICS-CALCULATED PARAMETERS

The following characteristics are derived from various device operating parameters (frequency, mode etc.). They are not specifically tested or guaranteed and may differ from the min and max limits shown by a small amount due to internal device setup times and propagation delays. However, these equations can be used to derive a more accurate idea of typical device performance than the guaranteed values.

PARAMETER	SYMBOL	CONDITION	MIN	MAX
OUT1$\uparrow$ from OE$\uparrow$	t_{en}		t_M	$2t_M$
OUT1$\downarrow$ from OE $\downarrow$ N = 1 N = 2	 t_{dis} t_{dis}		 t_{OUTH} 0	 $t_{OUTH + t_M}$ t_{OUTH}
$\overline{PDN}\downarrow$ to OUT1 Hi-Z N = 1 N = 2	 t_{pdn} t_{pdn}		 t_{OUTH} 0	 $t_{OUTH + t_M}$ t_{OUTH}
$\overline{PDN}\downarrow$ to OUT0 Hi-Z N = 1 N = 2	 t_{pdn} t_{pdn}		 t_{OUTH} 0	 $t_{OUTH + t_M}$ t_{OUTH}
$\overline{PDN}\uparrow$ to OUT1$\uparrow$	t_{stab}			$256t_M$
$\overline{PDN}\uparrow$ to OUT0 $\uparrow$	t_{stab}			$256t_M$
OUT1$\uparrow$ after Power-up				$256t_M$
OUT0$\uparrow$ after Power-up				$256t_M$