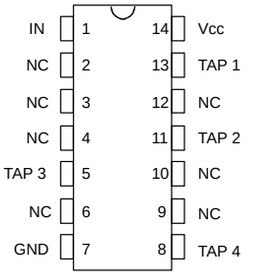
DALLAS SEMICONDUCTOR

DS1003
4-Tap Silicon Delay Line for RISC Applications

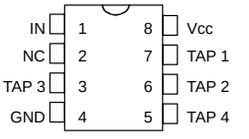
FEATURES

- All-silicon time delay
- Four delayed clock phases from input
- Input frequency independent
- Precise tap-to-tap delays
- Leading and trailing edge precision
- Preserves input symmetry
- Output rise time minimizes ringing
- Economical
- 8- and 14-pin packages available in DIP and surface mount
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays and pinouts available
- Fast turn prototypes

PIN ASSIGNMENT



DS1003 14-PIN DIP
(300 MIL)
See Mech. Drawings Section



DS1003M 8-PIN DIP
(300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

TAP 1 – TAP 4	–	TAP Output Number
V_{CC}	–	+5 Volts
GND	–	Ground
NC	–	No Connection
IN	–	Input

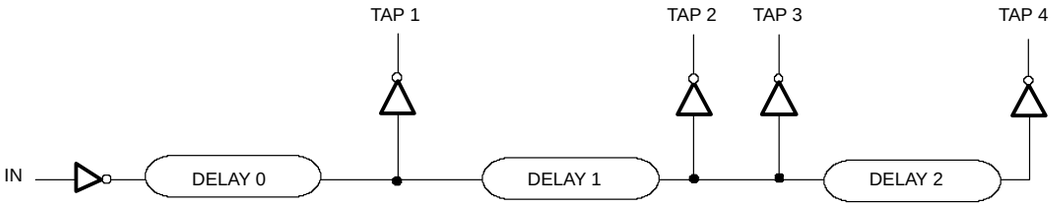
DESCRIPTION

The DS1003 Delay Line has been specifically designed to supply the four independent clock timing phases required by some RISC microprocessors and their related coprocessors. For optimum compatibility, the DS1003 accepts TTL input levels and supplies CMOS and TTL compatible output levels. The DS1003 is offered in 8- and 14-pin DIP packages. Low cost and superior reliability is achieved by the combination of a 100% silicon delay line and industry standard packaging. The DS1003 series of delay lines provides precise tap-to-tap delays while preserving input waveform symmetry.

Since the DS1003 is not based on Phase Locked Loop (PLL) technology, timing is input frequency-independent. Each tap is capable of driving a minimum of four LSTTL or CMOS loads. Tap-to-tap timing accuracy is not affected by the addition of equal capacitive loads (e.g. coprocessors).

Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 371–4348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PLH}) Table 1

PART NO.		DS1003-16	DS1003-20	DS1003-25	DS1003-33	DS1003-40
INPUT - TAP 1	Delay 0	8 ns ± 2 ns	8 ns ± 2 ns	8 ns ± 2 ns	6 ns ± 2 ns	6 ns ± 2 ns
TAP 1 - TAP 2	Delay 1	6 ns ± .75 ns	6 ns ± .75 ns	6 ns ± .5 ns	4.5 ns ± .5 ns	4.0 ns ± .5 ns
TAP 1 - TAP 4	Delay 1+ Delay 2	16 ns ± 1 ns	14 ns ± 1 ns	12 ns ± .75 ns	9 ns ± .75 ns	8 ns ± .75 ns
TAP 2 - TAP 3 (Note 10)	——	0.2 ns ± .2 ns	0.2 ns ± .2 ns	0.2 ns ± .2 ns	0.2 ns ± .2 ns	0.2 ns ± .2 ns
TAP 3 - TAP 4	Delay 2	10 ns ± .75 ns	8 ns ± .75 ns	6 ns ± .5 ns	4.5 ns ± .5 ns	4.0 ns ± .5 ns

PERIOD AND WIDTH TABLE Table 2

PART NO.	PERIOD			t_{WI}		
	MIN	NOM	MAX	MIN	NOM	MAX
DS1003-16	29 ns	30 ns	∞	12 ns	15 ns	∞
DS1003-20	24 ns	25 ns	∞	10 ns	12.5 ns	∞
DS1003-25	19 ns	20 ns	∞	8 ns	10 ns	∞
DS1003-33	14 ns	15 ns	∞	6 ns	7.5 ns	∞
DS1003-40	12 ns	12.5 ns	∞	5 ns	6.25 ns	∞

I_{CC} TABLE Table 3

PART NO.	I_{CC}	
	TYP	MAX
DS1003-16	65 mA	75 mA
DS1003-20	75 mA	85 mA
DS1003-25	85 mA	95 mA
DS1003-33	100 mA	110 mA
DS1003-40	115 mA	125 mA

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

($0°C$ to $70°C$; $V_{CC} = 5.0V \pm 5\%$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC} = Max; Period = Min.		Table 3	Table 3	mA	2
High Level Output Current	I_{OH}	V_{CC} = Min. V_{OH} = 4			-1	mA	
Low Level Output Current	I_{OL}	V_{CC} = Min V_{OH} = 0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$; $V_{CC} = 5.0V \pm 5\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	Table 2	Table 2	Table 2	ns	6
TAP to TAP Delay (leading edge)	t_{PLH}	Table 1	Table 1	Table 1	ns	3,4,5,6,7
TAP to TAP Delay (trailing edge)	t_{PHL}		Note 9		ns	9
Output Symmetry (Input: 50%±5%)		40	50	60	%	3,5
Output Rise Time	t_{OR}		2.0	2.5	ns	8,10
Output Fall Time	t_{OF}		2.0	2.5	ns	8,10
Power-up Time	t_{PU}			100	ms	
Period	Period	Table 2	Table 2	Table 2	ns	

CAPACITANCE

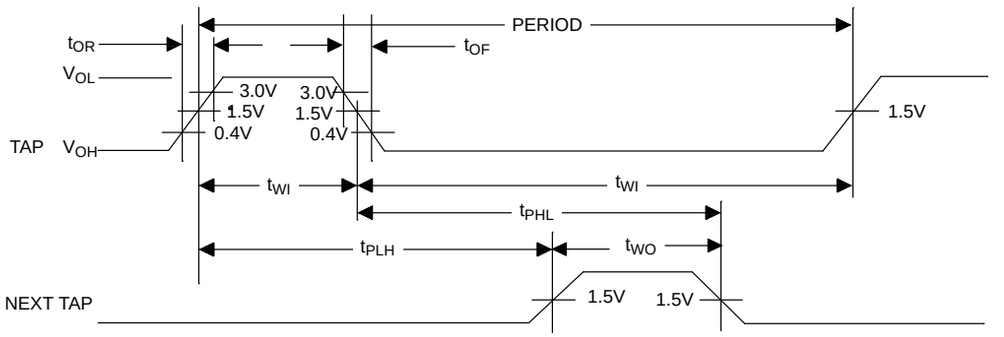
($T_A = 25°C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	10

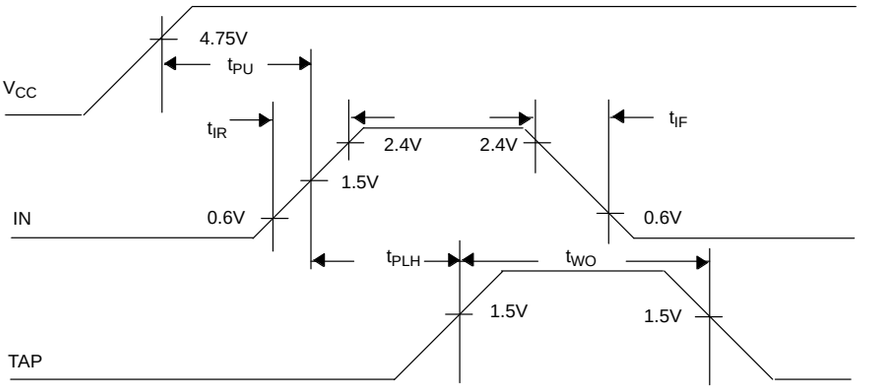
NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open, minimum period.
3. V_{CC} = 5V @ 25°C.
4. Temperature variations from 25°C to 0°C or 70°C may produce an additional tap-to-tap delay shift of ±0.5 ns. Voltage variations from 5.0V to 4.75V or 5.25V produce a worst case tap-to-tap delay shift of 5%.
5. All tap-to-tap delays vary unidirectionally over temperature or voltage range. For example, if the TAP 1 - TAP 2 delay, t_{PLH}, slows down, the TAP2 - TAP 4 delay, $t_{PLH,}$ will also slow down. Since t_{PHL} tracks t_{PLH}, symmetry is preserved.
6. See “Test Conditions” section at the end of this data sheet.
7. Since all four taps have identical output stages, tap-to-tap delays and waveform symmetry will exhibit minimal variation when capacitive loading is increased identically on all taps at the same time (e.g., the addition of one or more RISC coprocessors).
8. V_{CC} = Min; C_L = 30 pF
9. Trailing edge delays, t_{PHL}, are adjusted to maintain waveform symmetry.
10. Guaranteed by design. Periodically tested.

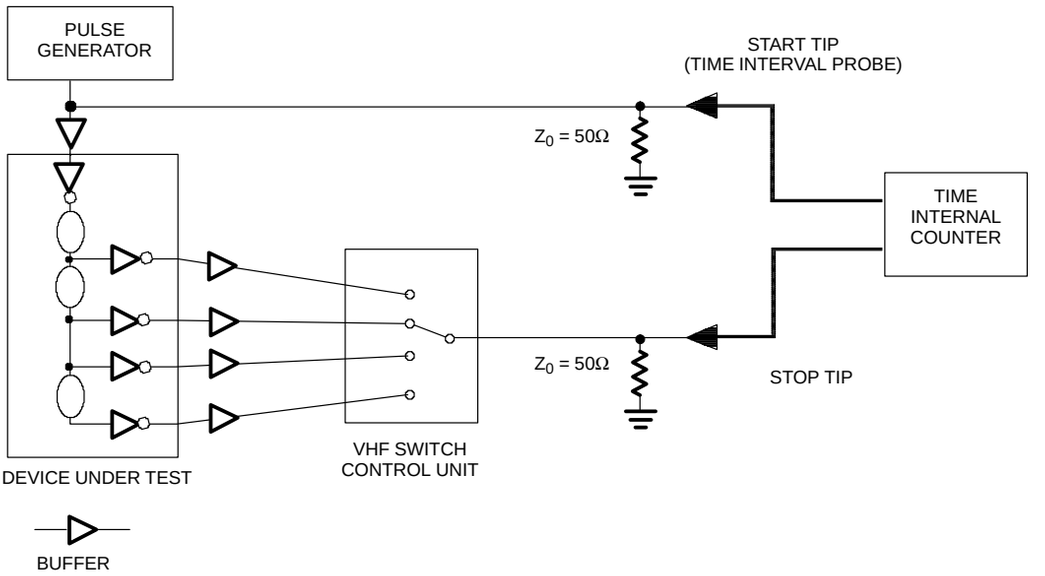
TIMING DIAGRAM: SILICON DELAY LINE Figure 2



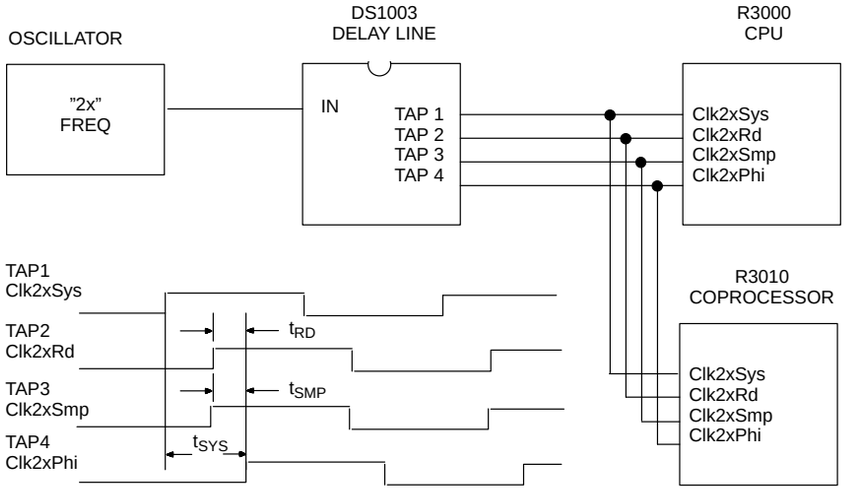
POWER-UP TIMING DIAGRAM Figure 3



TEST CIRCUIT Figure 4



TYPICAL APPLICATION Figure 5



NOTE: TAP 2 can be used for Clk2xSmp with TAP 3 as Clk2xRd.

TERMINOLOGY

Period: The time elapsed between the leading edge of the first trigger pulse and the leading edge of the following pulse.

Symmetry: That percent of the Period when the input or output is above 1.5V.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{IR} (Input Rise Time): The elapsed time between 0.6V and 2.4V on the leading edge of the input pulse.

t_{IF} (Input Fall Time): The elapsed time between 2.4V and 0.6V on the trailing edge of the input pulse.

t_{OR} (Output Rise Rime): The elapsed time between 0.4V and 3.0V on the leading edge of the output pulse.

t_{OF} (Output Fall Time): The elapsed time between 3.0V and 0.4V of the trailing edge output pulse.

t_{PLH} (Time Delay, Rising): Input-to-tap or tap-to-tap delay measured between the 1.5V points on the leading edges.

t_{PHL} (Time Delay, Falling): Input-to-tap or tap-to-tap delay measured between the 1.5V points on the trailing edges.

t_{PU} (Power-up Time): After V_{CC} is valid, the time required before timing specifications are within tolerance.

TEST SETUP DESCRIPTION

Figure 4 illustrates the hardware configuration used for measuring the timing parameters on the DS1003. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution connected between the input and each tap). Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

Input:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V Low = 0.0V ± 0.1
Source Impedance:	50 ohm max.
Rise and Fall Time:	3.0 ns max. (measured between 0.6V and 2.4)
Pulse Width:	500 ns
Period:	1000 ns

Output:

Each output is loaded with the equivalent of one 74F04 input. Delays are measured at the 1.5V level.

Note:

Above conditions are for test only. The adjusted test limits and guardbands used assure operation to data sheet timing specifications.