Software Architecture of NAV-2100

INTRODUCTION

This is an overview of the hardware and software architectures of the NAV-2100. The NAV-2100 is a DSP-based GPS Receiver solution based on ADSP218x family of DSPs developed by Analog Devices and Accord Software & Systems Pvt. Ltd. This solution has a software intensive approach to GPS signal processing with an innovative Soft Correlator. The programmable platform of the NAV-2100 facilitates easy upgrade of systems with better and improved algorithms. The chipset features fast acquisition of satellite signals even when there is no information about satellite location. In addition, the solution has spare computational resources and a modular software architecture that facilitates integration of user-defined application software with the GPS function on the same DSP chip.

SCOPE

The top level design description includes various operational modes of the GPS receiver along with state transitions and integration of user-defined application modules with the GPS function.

FUNCTIONAL DESCRIPTION OF A GPS RECEIVER

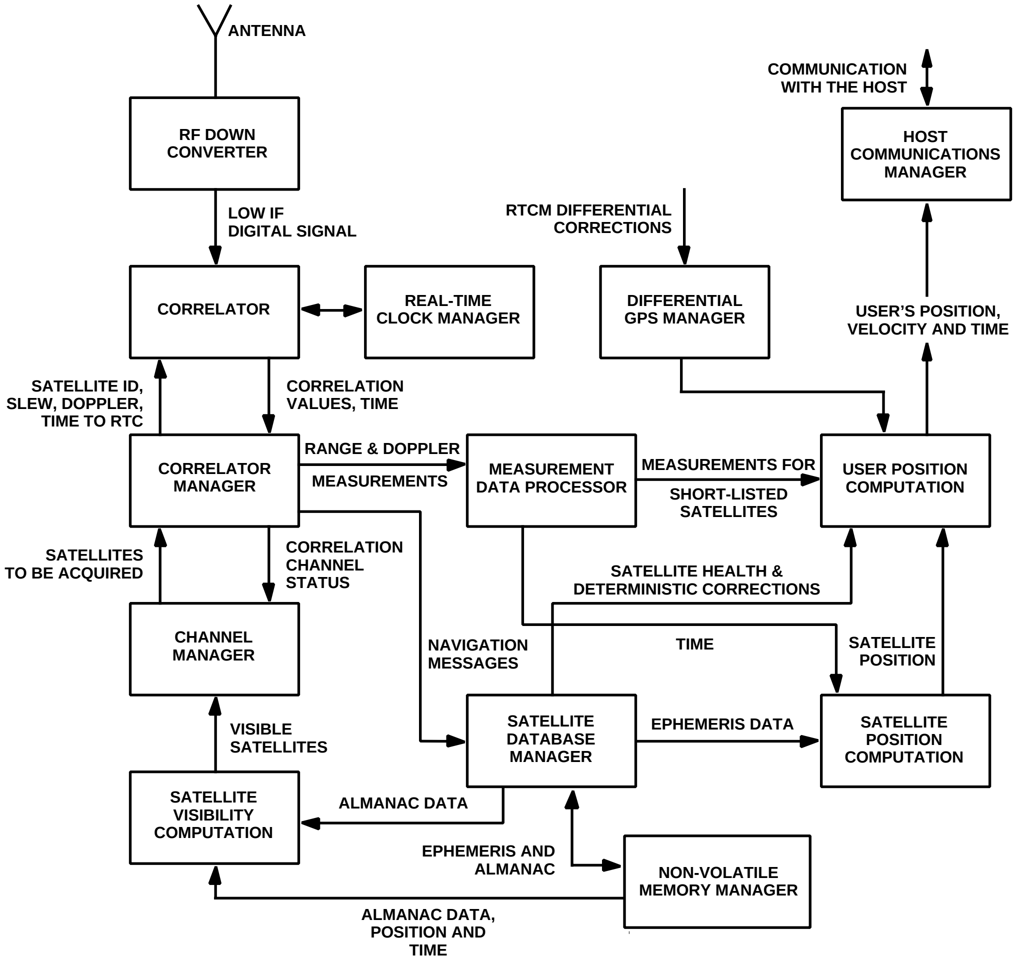

ANTENNA
RF DOWN CONVERTER
LOW IF DIGITAL SIGNAL
CORRELATOR
REAL-TIME CLOCK MANAGER
SATELLITE ID, SLEW, DOPPLER, TIME TO RTC
CORRELATION VALUES, TIME
CORRELATOR MANAGER
RANGE & DOPPLER MEASUREMENTS
MEASUREMENT DATA PROCESSOR
MEASUREMENTS FOR SHORT-LISTED SATELLITES
USER POSITION COMPUTATION
SATELLITES TO BE ACQUIRED
CORRELATION CHANNEL STATUS
CHANNEL MANAGER
VISIBLE SATELLITES
SATELLITE VISIBILITY COMPUTATION
ALMANAC DATA
NAVIGATION MESSAGES
SATELLITE DATABASE MANAGER
EPHEMERIS DATA
SATELLITE POSITION COMPUTATION
SATELLITE HEALTH & DETERMINISTIC CORRECTIONS
TIME
SATELLITE POSITION
EPHEMERIS AND ALMANAC
NON-VOLATILE MEMORY MANAGER
ALMANAC DATA, POSITION AND TIME
RTCM DIFFERENTIAL CORRECTIONS
DIFFERENTIAL GPS MANAGER
USER'S POSITION, VELOCITY AND TIME
HOST COMMUNICATIONS MANAGER
COMMUNICATION WITH THE HOST

Figure 1. Functional Constituents of a GPS Receiver

A typical GPS Receiver consists of the following functional constituents (as shown in Fig. 1).

Antenna
The Antenna receives the L band GPS signal and provides Low Noise Amplification.

RF Down Converter
The RF Down Converter generates a low IF digital signal (2.048 MHz) from the input 1575.42 M Hz signal after three down conversions.

Correlator
Correlator despreads the incoming CDMA GPS signal. It simultaneously acquires and tracks signals from up to 12 satellites, giving the Correlation values as output.

Correlator Manager
Correlator Manager controls and monitors the channels of the Correlator. It carries out range and Doppler measurements. It also extracts Navigation messages.

Satellite Database Manager (SDBM)
SDBM maintains the Satellite Database in the receiver.

Channel Manager
Channel Manager assigns appropriate satellites to all the channels of the Correlator for acquisition.

Measurement Data Processor (MDP)
MDP filters the Pseudorange and Deltarange measurements for all tracking satellites and also validates the measurement data for use in the computation of the User's position.

User Position Computation
User position computation module computes the position and velocity of the receiver.

Scheduler
Scheduler controls the execution of the various modules of the receiver software.

Satellite Visibility Computation and Satellite Selection
Satellite Visibility Computation and Satellite Selection module computes the visibility table using the User's position, time, date and Almanac, and recommends satellites to the Channel Manager.

Satellite Position Computation
Satellite Position Computation module computes the precise position of the satellites for use in the computation of the user's position.

Host Communications Manager
Host Communication module communicates with the Host through RS232 link to provide the User Interface.

Non-Volatile Memory Manager (NVMM)
Non-Volatile Memory module maintains the ephemeris, almanac, position, time and geodetic datum to facilitate HOT START.

Real-Time Clock Manager
Real-Time Clock module is responsible for updating the RTC periodically with the GPS time and to retrieve the GPS time at receiver power-up.

Differential GPS Manager
DGPS module processes the RTCM messages to extract the DGPS corrections.

Operational Modes of the Receiver:
The GPS receiver will be in one of the four operational modes at any given time. The four modes are:

- INIT
- SEARCH
- POS
- IDLE

INIT Mode
When the INIT mode prevails at power-up/reset, the receiver software will do the following:

– initialize the hardware

– initialize the run time environment

– initialize global variables

– enable RS-232C communications

– conduct self-tests

If the self-tests fail, there will be a fatal exception condition. If the self-tests do not fail, the following functions are carried out:

– determine system parameters at power-up

– initialize state machine parameters

– initialize the correlator

At the end of these functions, the receiver operational mode will transit to SEARCH mode.

SEARCH Mode

The receiver will be in the SEARCH mode while it is trying to acquire a number of satellites with good relative geometry with the location of the user, track them and generate measurements for computation of position, speed, heading and time information. When the receiver is able to generate this information continuously, it will exit to the POS mode.

The receiver goes into SEARCH mode when meeting the following conditions:

- after completing INIT
- when the receiver fails to produce continuous fixes for more than ten seconds due to signal channels not tracking as many satellites as required, to find the "fixes" in the prevailing solution mode
- when commanded by the host to SEARCH the SKY
- when commanded by the host to acquire satellites that are not being tracked, thus not achieving a position fix
- while in the IDLE mode, it locates enough visible satellites

The receiver exits from this mode when:

- It is able to continuously track an adequate number of satellites to compute position fixes within acceptable error limits in the prevailing solution mode. (Transition will be to POS mode.)
- In the HOT START, if the receiver discovers that there are not adequate visible satellites to compute position in the prevailing solution mode. (Transition will be to IDLE mode.)
- The SEARCH mode has the objective of proceeding to the POS mode. How quickly it can exit to the POS depends upon the availability of certain parameters in the receiver (i.e., the ephemeris, the almanac, estimate of user's position and estimate of GMT and date).

Based on the availability or otherwise of one or more of these above parameters, the SEARCH mode is further described as:

- **COLD START**
- **AUTONOMOUS COLD START**
- **NORMAL START**
- **HOT START**

COLD START

The SEARCH is attributed with COLD START, if the receiver does not have one or more of the three initialization parameters, viz., position estimate, GMT and date estimate and almanac.

The receiver will exit COLD START to enter NORMAL START when:

- the host sends all three parameters

If the above events do not take place, the receiver proceeds in COLD START.

AUTONOMOUS COLD START

While in the SEARCH mode, if the receiver does not have any of the three parameters, the SEARCH is attributed with Autonomous Cold Start.

NORMAL START

The SEARCH is attributed with NORMAL START, if the receiver has all three parameters. If the receiver does not compute the position within four minutes, the receiver will exit NORMAL START to enter COLD START.

HOT START

HOT START is attributed to the mode in which the receiver has the ephemerides for the satellites in addition to the almanac, GMT and date, and position estimates.

POS Mode

This mode prevails when the receiver is able to continuously track an adequate number of satellites to compute position fixes within acceptable error limits.

The receiver exits from this mode to SEARCH mode, when the receiver doesn't find a fix position for more than ten successive seconds, within the acceptable error limits.

The receiver exits from this mode when, according to the visibility computations, there are not sufficient visible satellites to find fixes within acceptable error limits, into IDLE mode.

IDLE Mode

This mode prevails when, according to the receiver's satellite visibility computations, there are not sufficient visible satellites in the sky at a certain time, given the estimated position of the receiver.

The receiver enters this mode from either the SEARCH or POS modes, when visibility computations indicate that insufficient satellites are visible. The receiver exits into SEARCH mode, when otherwise indicated.

HARDWARE ARCHITECTURE

The NAV-2100 chipset is designed around two fixed point ADSST-NAV-2100 DSPs.

The hardware architecture is as shown in Figure 2.

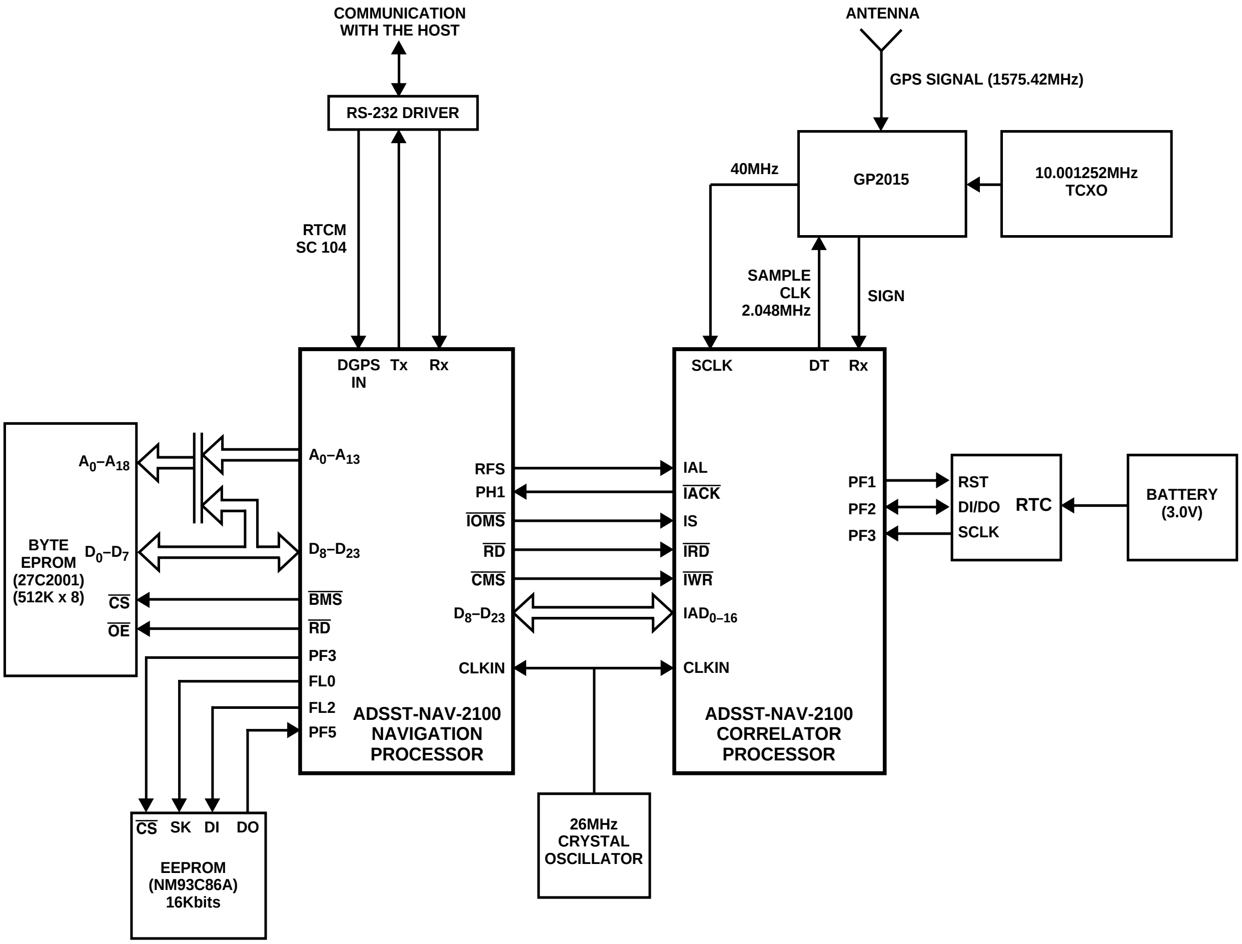


Figure 2. NAV-2100 Hardware Architecture

The Correlator Processor, implemented on one ADSST-NAV-2100 DSP chip, functions as the Correlator, while the Navigation Processor, implemented on the other ADSST-NAV-2100, incorporates all the other functions of the receiver listed above.

The major hardware components of the chipset are as follows:

- GP2015 RF Down converter
- ADSST-NAV-2100 DSPs
- PROM (Boot Program) (512k × 8)
- EEPROM (16K Bits)
- Real-Time Clock

GP 2015 down converts the 1575 MHz GPS signal to 4.10 MHz signal providing a gain of 120 dB.

The two ADSST-NAV-2100 DSPs function as the Correlator and the Navigation Processors respectively.

The EPROM contains the boot programs for both the DSPs.

The EEPROM contains the user position, ephemeris and almanac information.

The RTC maintains time in the absence of main power.

SOFTWARE ARCHITECTURE

The receiver software is designed around a few hardware interrupt service tasks which attend to time critical events, and a timer-based periodic and deterministic Scheduler.

The receiver software has the following types of tasks:

- Initialization
- Interrupt
- Periodically Invoked

Initialization tasks are invoked once on power-up/reset. These tasks initialize the receiver hardware and software and perform the built-in self-test and calibration functions. There will be no need for these to be invoked again.

Interrupt tasks gain control of the DSP asynchronously, any time after the software is initialized by the Initialization tasks. They are activated by hardware events.

Periodically Invoked tasks are invoked at predefined intervals.

The software functions achieved by means of Interrupt tasks are:

- Correlator
- Correlator Manager (CM)
- Exception Handler

The software functions accomplished through Periodically Invoked tasks are:

- Scheduler
- Measurement Data Processor (MDP)
- Satellite Data Base Manager (SDBM)
- Channel Manager (CHM)
- Host Communications Manager (HCOMM)
- Satellite Position Computation (SPC)
- Satellite Selection (SVS)
- User Position Solution (UPS)
- Non-Volatile Memory Manager (NVMM)
- DGPS Manager
- Real-Time Clock (RTC)

The User Application (UAPP) tasks can either be periodically invoked or allotted the time remaining after the GPS tasks are complete. The choice among the two above is entirely dependent on the User.

Upon power-up/reset, the Initialization tasks initialize the receiver hardware and software and perform self-tests and calibration. The interrupt servicing mechanisms are also set up during initialization.

After initialization, the Scheduler is invoked by a timer at the rate of 250 milliseconds. The Scheduler checks for the prevailing operational conditions of the receiver and affects all the state transitions. It also executes all the periodic tasks at the appropriate intervals.

At the topmost level, the GPS software is organized as shown below. The program waits on a software timer that goes off once every 250 milliseconds. The Scheduler is executed at the expiry of each timer interval. All the hardware interrupts occur asynchronously and are not reflected in the pseudocode. The Scheduler and the other periodically invoked tasks communicate, synchronize and exchange data through shared global memory and critical regions.

The organization of software below integrates the user application within the Scheduler. The user application will be invoked at a rate of multiples of 250 milliseconds.

```
main ()
{
     /*
      * assignment of wait states to different blocks, definition
      * of programmable discrete I/Os etc.
      *
      */
     Initialize hardware;

     /*
      * Assignment of interrupt structures, priorities
      * definition of context for task switching,
      * initialization of global data structures etc.
      *
      */
     Initialize software;

     /*
      * perform self tests, calibration etc.
      *
      */
     Perform self tests;

     Enable Interrupts;

     DO FOREVER
     {
          Wait till software timer goes off;
          /* wait for the end of the  of 250  milliseconds interval */
          CALL Scheduler;
     }

}
```

```
      /*
       * assignment of wait states to be different blocks, definition
       * of programmable discrete I/Os etc.
       *
       */
      Initialize hardware;

      /*
       * Assignment of interrupt structures, priorities
       * definition of context for task switching,
       * initialization of global data structures etc.
       *
       */
      Initialize software;

      /*
       * perform self tests, calibration etc.
       *
       */
      Perform self tests;

      Enable Interrupts;

      DO FOREVER
      {
             UserApplication ();
      }
}
```

The relative priority levels of the various tasks are listed in the table below, along with the frequency of their occurrences. H means the highest level of priority, H-1, H-2, etc., mean the second, third etc., levels of priority respectively.

Task	Type	Period	Priority Level	Processor
Exception Handler	SW Int	asynchronous	H-1	NAV Processor
Correlator	HW Int	asynchronous	H	Correlator
Correlator Manager	HW Int	asynchronous	H-2	NAV Processor
Measurement Data Processor	SW Int	20 msec	H-3	NAV Processor
Satellite Database Manager	Timer Invoked	250 msec	H-4	NAV Processor
Host Communications Manager	Timer Invoked	250 msec	H-4	NAV Processor
Channel Manager	Timer Invoked	250 msec	H-4	NAV Processor
Scheduler	Timer Invoked	250 msec	H-4	NAV Processor
Satellite Position Computation	Timer Invoked	1000 msec	H-4	NAV Processor
Position Solution	Timer Invoked	1000 msec	H-4	NAV Processor
Satellite Selection	Timer Invoked	80 seconds	H-4	NAV Processor
Non-Volatile Memory Manager	Timer Invoked	1000 msec	H-4	NAV Processor
Real-Time Clock Manager	Timer Invoked	1000 msec	H-4	NAV Processor
DGPS Manager	Timer Invoked	1000 msec	H-4	NAV Processor
User Application	Timer Invoked	1000 msec	H-4	NAV Processor

VARIOUS TASKS OF THE GPS SOFTWARE

Scheduler

The ADSST-NAV-2100 Digital Signal Processor has 16K of internal program memory. This address space is sufficient for the software modules that reside in the Correlator Processor. However, the program memory requirements of the software modules in the Navigation Processor stretch up to 64K words and so all the software cannot reside simultaneously in the on-chip program memory. To overcome this problem, the Navigation Processor uses BDMA to load the required program into internal memory from Byte Memory.

In the Navigation processor, the internal memory is divided into upper and lower banks. Software modules are also classified into Resident and Dynamically Loadable modules. The Correlator Manager, Scheduler and Floating-Point library are all resident modules and they reside in the lower 12.8K bank of the program memory. The upper 3.2K program memory is periodically loaded by the Scheduler, once every 250 milliseconds with different dynamically loadable software modules using BDMA. The Scheduler ensures that these modules are invoked at the required periods. The Scheduler itself is executed once every 250 milliseconds. Each such interval is called a minor cycle and four minor cycles make one major cycle, which is one second.

Among the dynamically loadable modules, some are to be executed in all minor cycles of the Scheduler. These are grouped into one segment.

All other dynamically loadable modules are divided into different segments based on the minor cycle in which they will be executed.

All of the above segments are loaded into a Boot EPROM.

On reset, the lower 12.8K of internal memory is loaded with resident modules, viz., Exception Handler, Correlator Manager, Scheduler, Floating-Point Library, and the execution starts.

At every minor cycle, the Scheduler dynamically loads the required modules by loading the required memory segment from the Boot EPROM to upper 3.2K bank of Internal Program Memory using BDMA.

After execution, the next segment is loaded and so forth.

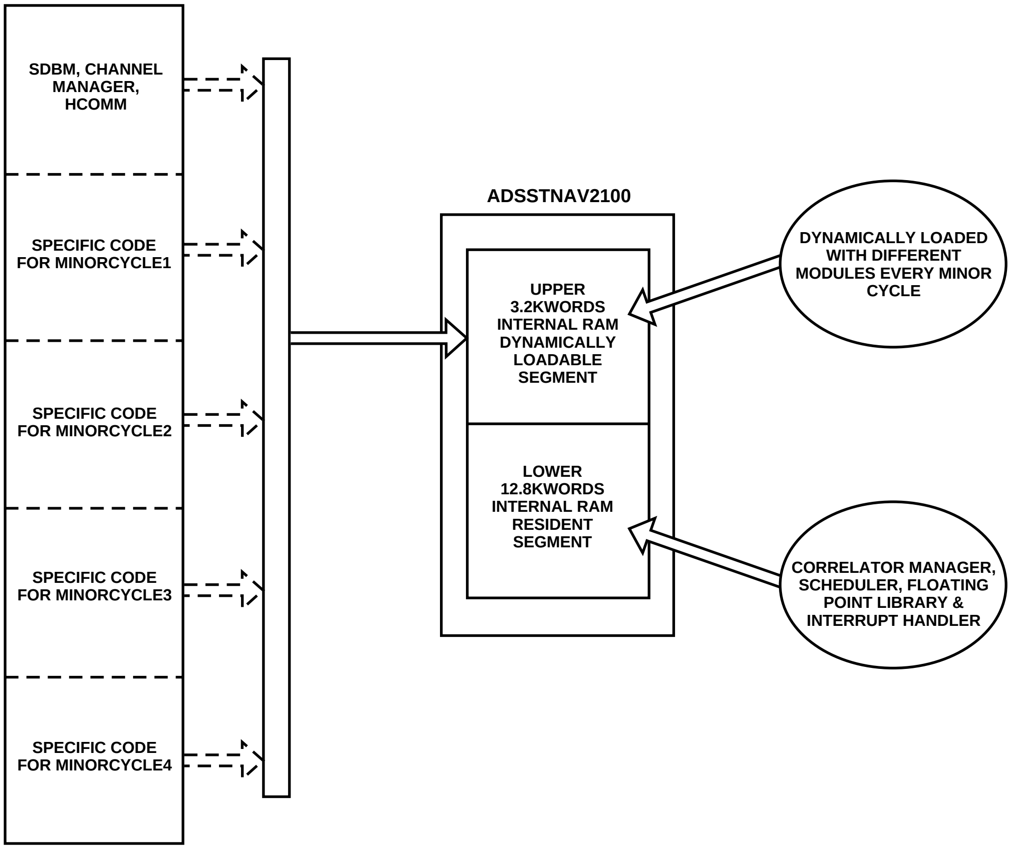

SDBM, CHANNEL MANAGER, HCOMM
SPECIFIC CODE FOR MINORCYCLE1
SPECIFIC CODE FOR MINORCYCLE2
SPECIFIC CODE FOR MINORCYCLE3
SPECIFIC CODE FOR MINORCYCLE4
ADSSTNAV2100
UPPER 3.2KWORDS INTERNAL RAM DYNAMICALLY LOADABLE SEGMENT
LOWER 12.8KWORDS INTERNAL RAM RESIDENT SEGMENT
DYNAMICALLY LOADED WITH DIFFERENT MODULES EVERY MINOR CYCLE
CORRELATOR MANAGER, SCHEDULER, FLOATING POINT LIBRARY & INTERRUPT HANDLER

Figure 3. Program Memory Configuration for the Navigation Processor

The Scheduler operates based on the prevailing operational modes of the receiver and the minor cycle count. It checks for the prevailing operational conditions of the receiver and affects state transitions. It also conditionally invokes all the periodically invoked tasks. The Scheduler is activated as soon as the receiver successfully exits the INIT mode.

A typical allocation of periodically invoked tasks to the four minor cycles is shown in the table below. Here, the User Application is accorded an entire minor cycle. If the alternate architecture is selected, the User Application will be given the remaining time in every minor cycle.

Minorcycle1	Minorcycle2	Minorcycle3	Minorcycle4
CHM	CHM	CHM	CHM
SDBM	SDBM	SDBM	SDBM
HCOMM	HCOMM	HCOMM	HCOMM
UAPP	SPC	UPS	SVS

Correlator

This is the Soft-Correlator, implemented as a hardware interrupt, which occurs asynchronously at an approximate frequency of 1000 cycles per second. Correlator generates correlation values for prompt and dither arms for 12 satellites at the programmed chip shift and Doppler.

Correlator Manager

This is the Acquisition/Tracking software to manage the 12-channel correlator. It is implemented by using a hardware interrupt, asynchronously occurring approximately once every millisecond. Extraction of 50 bps navigation messages, generation of measurements for pseudorange and deltarange are the main objectives of the Correlator Manager.

Exception Handler

This task is a software interrupt that handles all the exception conditions. This occurs aperiodically and asynchronously.

Satellite Database Manager

Synchronization with the navigation data from twelve satellites, extraction of ephemeris, almanac, health and other data are the main functions performed by the Satellite Data Base Manager. It is invoked once every 250 milliseconds.

Channel Manager

Channel Manager programs the various channels with the satellite signals to be acquired dynamically. This task is also invoked once every 250 milliseconds.

Measurement Data Processor

Measurement Data Processor averages measurements, determines the time at which measurements are generated and shortlists satellites for which the receiver has measurements. This task is periodically executed, once every 20 milliseconds.

Satellite Selection

This task determines the list of visible satellites and their azimuth and elevation angles at user's estimated position and time, making use of almanac data. Channel Manager makes use of the list of visible satellites while dynamically assigning them to channels. Satellite Selection task is executed once every 80 seconds by the scheduler.

Satellite Position Computation

This task computes precise satellite position coordinates making use of ephemeris data. This is executed once every second.

Host Communications Manager

This task processes all the messages from the host that come through the Soft UART. It also generates all the messages to the host. This task is executed once every 250 milliseconds.

User Position Solution

This task computes user's position, speed, heading and time once every second.

Non-Volatile Memory Manager

This task is responsible for loading the various estimates such as ephemeris, almanac, GMT, date, position, datum reference etc., to facilitate HOT START. This task also verifies the age of the estimates for use and periodically refreshes the estimates. This task is invoked once every second.

Real-Time Clock Manager

This task is responsible for storing time into and reading time from the Real-Time Clock. The read is performed once during receiver initialization while the write is periodically performed every 3600 seconds.

Differential GPS Manager

This module is responsible for collecting the raw RTCM SC-104 DGPS messages from the modem and processing the collected messages every second.

MIPs Usage in Correlator Processor

The consumption of MIPs for 12-channel configuration is as given below.

Channels	Total	Peak	Average	Spare
12	52	50	50	2

Memory Usage in Correlator Processor

The memory usage in the 12-channel configuration will be as given below.

Channels	Memory	Configured	Used	Spare
12	PM	16K words	7K words	9K words
12	DM	16K words	7K words	9K words

MIPS Usage in NAV Processor

The consumption of MIPs is as given below:

Channels	Total	Peak	Average	Spare
12	52	35	20	32

Memory Usage in NAV Processor

The memory usage is as given below:

				Spare	
Channels	Memory	Configured	Used	Resident	Nonresident
12	PM	16K words	14K words	2K words	3.2K words
12	DM	16K words	15K words	1K words	Not Applicable

Note: Nonresident memory refers to the portion of the memory that is dynamically loaded into the on-chip program memory by the Scheduler.

PROGRAMMATIC INTERFACE TO THE GPS CORE ON ADSST-NAV-2100 CHIP

Introduction

The ADI NAV-2100 chipset has a unique programmatic interface to the application developer. Using this interface, the developer can integrate his/her application with the GPS core library on the same DSP, without having to use another microcontroller.

The interface enables the application developer to:

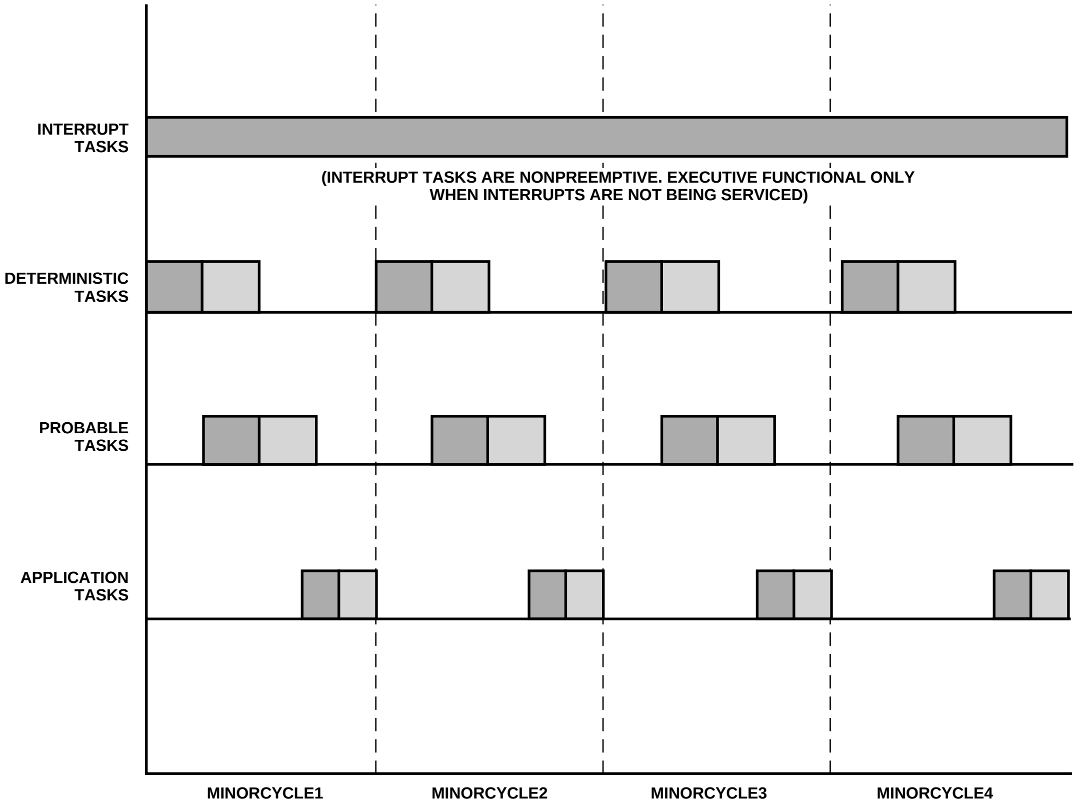
- Access the necessary data structures
- Make use of the real-time GPS outputs
- Link the application software to the GPS core engine library

How Does it Work?

The GPS Engine Core software has a real-time executive that manages the resources of the DSP and provides the interface to the application developer.

The mobilization of computational assets by the DSP can be described using time intervals called Minor Cycles. A Minor Cycle is typically a time interval of 250 milliseconds and every second is divided into four minor cycles. The figure below shows how the DSP resources are used during every second.

The Interrupt tasks are nonpreemptive. When these are not being serviced, the executive will be providing the resources to complete tasks on a priority basis in a cyclic manner.



The Deterministic Tasks are strictly periodic in nature.

Probable Tasks are not necessarily periodic and are invoked conditionally.

Application Tasks are programs developed by the developer conforming to the defined programmatic interface. These are attended to by the executive after servicing the Deterministic and Probable tasks scheduled for the Minor Cycle.

The executive operates on a basic assumption that the worst case execution time of the Deterministic, Probable and Application tasks together does not exceed the minor cycle boundary. This imposes an execution time limit on the Application Task. This limit is governed by the GPS receiver core specifications.

How To Use the Interface

The developer can write his own code either in gnu C (ANSI C compatible from Free Software Foundation) or ADSST-NAV-2100 assembler. He can access, if necessary, all the real-time GPS outputs through data structures. The application should have an entry function called “MyApp ( ).” The user’s object code should be linked with the GPS core library to generate the executable file. A programmer reference manual will be provided to guide the developer through the process.

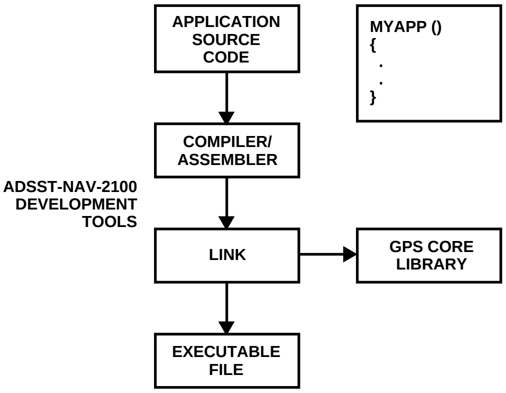


Figure 4. Application Development on ADSST-NAV-2100-based GPS Core Library

G3433–5–10/98

EUROPE HEADQUARTERS
Am Westpark 1–3
D-81373 München, Germany
Tel: +89 76903 551; Fax: +89 76903 557

JAPAN HEADQUARTERS
New Pier Takeshiba, South Tower Building
1-16-1 Kaigan, Minato-ku, Tokyo 105, Japan
Tel: (3) 5402-8200; Fax: (3) 5402-1063

SOUTHEAST ASIA HEADQUARTERS
4501 Nat West Tower, Times Square
Causeway Bay, Hong Kong
Tel: (852) 506-9336; Fax: (852) 506-4755

WORLDWIDE HEADQUARTERS
One Technology Way, P.O. Box 9106
Norwood, MA 02062-9106, USA
Tel: 781-461-3060; Fax: 781-461-4360
email: systems.solutions@analog.com

PRINTED IN U.S.A.