HIGH-SPEED DIGITAL ISOLATOR

PRELIMINARY TECHNICAL DATA ADuM1100A/ADuM1100B

FEATURES

- High Data Rate: DC – 100 MBd
- Compatible with 3.3V or 5V Operation
- Low Power Operation
  - 5V Operation: 0.7 mA @1 MBd,
    6.3 mA @25 MBd,
    24 mA @100 MBd
  - 3.3V Operation: 0.5 mA @1 MBd,
    4.1 mA @25 MBd,
    16 mA @100 MBd
- Small Footprint: Standard 8 Lead SO package
- High Common Mode Transient Immunity: >25kV/μS
- No Long Term Wearout
- Safety and Regulatory Approvals (Pending)
  - UL Recognized
    2500 Vrms for 1 min. per UL 1577
  - CSA Component Acceptance Notice #5
  - VDE 0884
    V_{IORM} = 560 Vpeak

APPLICATIONS

- Digital Fieldbus Isolation
- Opto-Isolator Replacement
- Computer-Peripheral Interface
- Microprocessor System Interface
- General Instrumentation and Data Acquisition Applications

DESCRIPTION

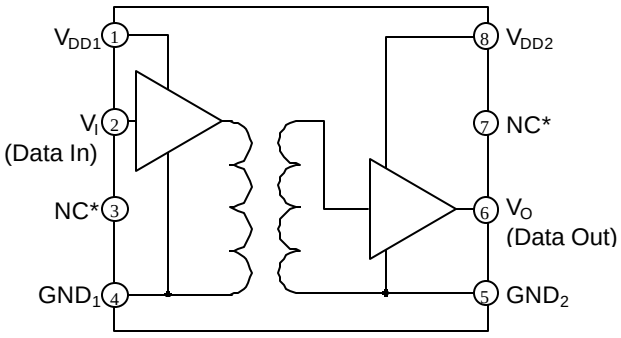
The ADuM1100A and ADuM1100B are digital isolators based on Analog Devices' *mm*Isolation (micromachined isolation) technology. Combining high-speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to optocoupler devices.

Configured as pin-compatible replacements for existing high-speed optocouplers, the ADuM1100A and ADuM1100B support data rates as high as 25 MBd and 100 MBd, respectively.

Both the ADuM1100A and ADuM1100B operate at either 3.3V or 5V supply voltages, boast propagation delay of <10ns and edge asymmetry of <2 ns. They operate at very low power, less than 0.65 mA of quiescent current (sum of both sides) and an additional current of 460 μA per MHz of signal frequency (230 μA per Mbd). Unlike common transformer implementations, the ADuM1100A/B provides DC correctness with a patented refresh feature which continuously updates the output signal.

PRELIMINARY TECHNICAL DATA

FUNCTIONAL BLOCK DIAGRAM



* Pin 3 and Pin 7 on the ADuM1100A are not connected internally.

TRUTH TABLE (POSITIVE LOGIC)

V_I, Input	V_{DD1} State	V_{DD2} State	V_O, Output	Note
H	Powered	Powered	H	
L	Powered	Powered	L	
X	Unpowered	Powered	H	V_O returns to V_I state within 2 μsec of power restoration
X	Powered	Unpowered	X	V_O returns to V_I state within 2 μsec of power restoration

Protected by U.S. patent 5,952,849. Additional patents are pending.

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Solder Reflow Thermal Profile

TBD

Regulatory Information

(pending)

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Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(I01)	4.90	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	4.35	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.016	mm	Insulation distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	> 175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

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VDE 0884 Insulation Characteristics

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110 for rated mains voltage <= 150Vrms for rated mains voltage <= 300Vrms		 I- IV I- III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110, Table 1)		2	
Maximum Working Insulation Voltage	V_{IORM}	560	Vpeak
Input to Output Test Voltage, Method b V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1sec, Partial Discharge < 5pC	V_{PR}	1050	Vpeak
Input to Output Test Voltage, Method a V_{IORM} x 1.5 = V_{PR}, Type and Sample Test, t_m = 60 sec, Partial Discharge < 5pC	V_{PR}	840	Vpeak
Highest Allowable Over-voltage (Transient Over-voltage, t_{TR} =10 sec)	V_{TR}	4000	Vpeak
Safety-limiting values (Maximum value allowed in the event of a failure) Case Temperature Input Current Output Power	 T_S $I_{S, INPUT}$ $P_{S,OUTPUT}$	 TBD TBD TBD	 °C mA mW
Insulation Resistance at Ts, V_{IO} = 500V	Rs	$>10^9$	Ω

PRELIMINARY TECHNICAL DATA

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-55	125	°C
Ambient Operating Temperature	T_A	-40	85	°C
Supply Voltages	$V_{DD1,2}$	0	6.5	V
Input Voltage	V_I	-0.5	$V_{DD1+0.5}$	V
Output Voltage	V_O	-0.5	$V_{DD2+0.5}$	V
Average Output Current	I_O		25	mA
ESD (Human Body Model)			2.0	KV
Lead Solder Temperature	TBD			
Solder Reflow Temperature Profile	TBD			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Operating Temperature	T_A	-40	85	°C	
Supply Voltages	$V_{DD1,2}$	3.0	5.5	V	1
Logic High Input Voltages	V_{IH}	$0.8+0.24V_{DD1}$	V_{DD1}	V	
Logic Low Input Voltage	V_{IL}	0.0	0.8	V	
Input Signal Rise and Fall Times			1.0	ms	2
Ambient Magnetic Field			10	KGauss	3

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Electrical Specifications, 5V Operation

4.5V≤ V_{DD1}, V_{DD2} ≤ 5.5V. Test conditions that are not specified can be anywhere within the recommended operating range. All typical specifications are at T_A = 25 °C, V_{DD1} = V_{DD2} = +5V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
DC Specifications								
Input Supply Current	$I_{DD1(Q)}$		0.15	0.40	mA	V_I = 0V or V_{DD1}		
Output Supply Current	$I_{DD2(Q)}$		0.15	0.25	mA	V_I = 0V or V_{DD1}		
Input Supply Current (25 MBd)	$I_{DD1(25)}$		3.9	4.6	mA	12.5 MHz logic signal freq.	1	
Output Supply Current (25 MBd)	$I_{DD2(25)}$		1.4	1.7	mA	12.5 MHz logic signal freq.	2	
Input Supply Current (100 MBd)	$I_{DD1(100)}$		15	18	mA	50 MHz logic signal freq., ADuM1100B only	1	
Output Supply Current (100 MBd)	$I_{DD2(100)}$		5.2	6	mA	50 MHz logic signal freq., ADuM1100B only	2	
Input Current	I_I	-10	0.01	10	µA	0 ≤ V_{IN} ≤ V_{DD1}		
Logic High Output Voltage	V_{OH}	4.4	5.0		V	I_O = -20 µA, V_I = V_{IH}		
		4.0	4.6			I_O = -4 mA, V_I = V_{IH}		
Logic Low Output Voltage	V_{OL}		0.0	0.1	V	I_O = 20 µA, V_I = V_{IL}		
			0.04	0.1	V	I_O = 400 µA, V_I = V_{IL}		
			0.4	0.8	V	I_O = 4 mA, V_I = V_{IL}		
Switching Specifications								
For ADuM1100A:								
Minimum Pulse Width	PW			40	ns	C_L= 15pF, CMOS signal levels		4
Maximum Data Rate		25			MBd			
For ADuM1100B:								
Minimum Pulse Width	PW		6.7	10	ns			5
Maximum Data Rate		100	150		MBd			
For ADuM1100A and ADuM1100B:								
Propagation Delay Time to Logic Low Output	t_{PHL}	3	6	9	ns			6
Propagation Delay Time to Logic High Output	t_{PLH}	3	6	9	ns			
Pulse Width Distortion, $\|t_{PHL}-t_{PLH}\|$	PWD		1	2	ns			
Propagation Delay Skew	t_{PSK1}			3	ns			7
Propagation Delay Skew (at constant temp. and supply voltages)	t_{PSK2}			2	ns			
Output Rise Time (10-90%)	t_R		2		ns			
Output Fall Time (90-10%)	t_F		2		ns			
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35		kV/µS	V_I = V_{DD1}, V_O > 0.8V_{DD1}, V_{CM} = 1000V, transient magnitude = 800V		8
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35		kV/µS	V_I = 0, V_O < 0.8V, V_{CM} = 1000V, transient magnitude = 800V		
Input Dynamic Power Dissipation Capacitance	C_{PD1}		60		pF			9
Output Dynamic Power Dissipation Capacitance	C_{PD2}		20		pF			

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Electrical Specifications, 3.3V Operation

3.0V≤ V_{DD1}, V_{DD2} ≤ 3.6V. Test conditions that are not specified can be anywhere within the recommended operating range. All typical specifications are at T_A = 25 °C, V_{DD1} = V_{DD2} = +3.3V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
DC Specifications								
Input Supply Current	$I_{DD1(Q)}$		0.10	0.26	mA	V_I = 0V or V_{DD1}		
Output Supply Current	$I_{DD2(Q)}$		0.10	0.17	mA	V_I = 0V or V_{DD1}		
Input Supply Current (25 MBd)	$I_{DD1(25)}$		2.6	3.0	mA	12.5 MHz logic signal freq.	1	
Output Supply Current (25 MBd)	$I_{DD2(25)}$		0.9	1.1	mA	12.5 MHz logic signal freq.	2	
Input Supply Current (100 MBd)	$I_{DD1(100)}$		10	12	mA	50 MHz logic signal freq., ADuM1100B only	1	
Output Supply Current (100 MBd)	$I_{DD2(100)}$		3.4	4.0	mA	50 MHz logic signal freq., ADuM1100B only	2	
Input Current	I_I	-10	0.01	10	µA	0 ≤ V_{IN} ≤ V_{DD1}		
Logic High Output Voltage	V_{OH}	2.9	3.3		V	I_O = -20 µA, V_I = V_{IH}		
		2.6	3.0			I_O = -4 mA, V_I = V_{IH}		
Logic Low Output Voltage	V_{OL}		0.0	0.1	V	I_O = 20 µA, V_I = V_{IL}		
			0.03	0.04	V	I_O = 400 µA, V_I = V_{IL}		
			0.3	0.4	V	I_O = 4 mA, V_I = V_{IL}		
Switching Specifications								
For ADuM1100A:								
Minimum Pulse Width	PW			40	ns	C_L= 15pF, CMOS signal levels		4
Maximum Data Rate		25			MBd			
For ADuM1100B:								
Minimum Pulse Width	PW		6.7	10	ns			5
Maximum Data Rate		100	150		MBd			
For ADuM1100A and ADuM1100B:								
Propagation Delay Time to Logic Low Output	t_{PHL}	5	8	11	ns			6
Propagation Delay Time to Logic High Output	t_{PLH}	5	8	11	ns			
Pulse Width Distortion, $\|t_{PHL}-t_{PLH}\|$	PWD		1	2	ns			
Propagation Delay Skew	t_{PSK1}			4	ns			7
Propagation Delay Skew (at constant temp. and supply voltages)	t_{PSK2}			3	ns			
Output Rise Time (10-90%)	t_R		2		ns			
Output Fall Time (90-10%)	t_F		2		ns			
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35		KV/µS	V_I = V_{DD1}, V_O > 0.8V_{DD1}, V_{CM} = 1000V, transient magnitude = 800V		8
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35		KV/µS	V_I = 0, V_O < 0.8V, V_{CM} = 1000V, transient magnitude = 800V		
Input Dynamic Power Dissipation Capacitance	C_{PD1}		40		pF			9
Output Dynamic Power Dissipation Capacitance	C_{PD2}		13		pF			

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Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min., T_A = 25°C	10, 11
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω		10
Capacitance (Input-Output)	C_{I-O}		2		pF	f = 1 MHz	
Input Capacitance	C_I		4.0		pF		12
Input IC Junction-to-Case Thermal Resistance	θ_{jci}		TBD		°C/W	Thermocouple located at center underside of package	
Output IC Junction-to-Case Thermal Resistance	θ_{jco}		TBD		°C/W		
Package Power Dissipation	P_{PD}			TBD	mW		

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Notes:

1. V_{DD1} and V_{DD2} must be kept within 1V of each other.
2. Output transitions are triggered based on input thresholds having 300 mV of hysteresis.
3. 10 KGauss of external magnetic field can be tolerated up to a frequency of 100KHz. Beyond 100 KHz, the maximum recommended magnetic field decreases by 20 dB/decade.
4. The minimum pulse width is the shortest pulsewidth at which the specified pulse width distortion is guaranteed.
5. The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
6. t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_I signal to the 50% level of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_I signal to the 50% level of the rising edge of the V_O signal.
7. t_{PSK1} is the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be measured between units at any given temperature within the recommended operating conditions. t_{PSK2} is the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be measured between units at any given temperature and any given supply voltage within the recommended operating conditions.
8. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 0.8V_{DD2}$. CM_L is the maximum common mode voltage slew rate than can be sustained while maintaining $V_O < 0.8V$. The common mode voltage slew rates apply to both rising and falling common mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
9. The total unloaded supply current consumption (in µA) at a given frequency (f) is calculated as follows: $(I_{DD1}+I_{DD2}) = C_{PD} * V_{DD} * f + I_{DD\text{-}idle}$, where f frequency in MHz.
10. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
11. In accordance with UL1577, each ADuM1100 is proof testing by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ µA).
12. Input capacitance is measured at pin 2 (V_I).

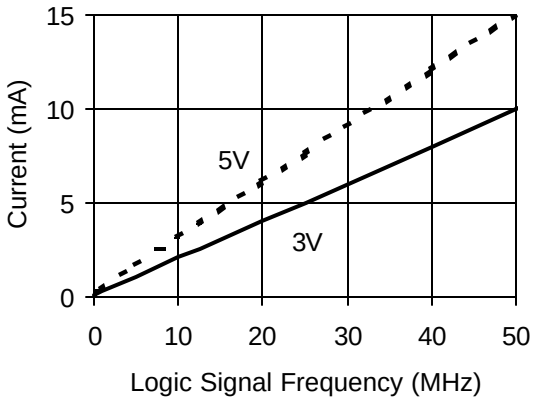

Figure 1. Typical Input Supply Current vs. Logic Signal Frequency for 5V and 3.3V Operation.

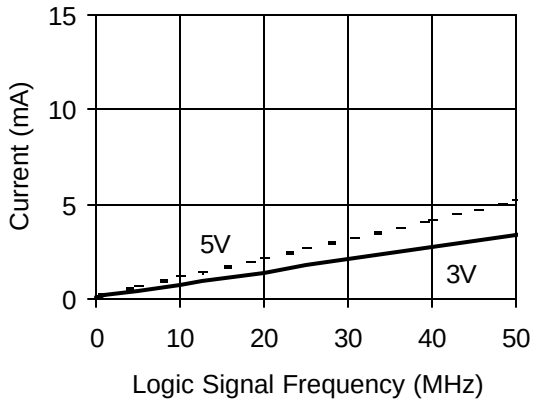

Figure 2. Typical Output Supply Current vs. Logic Signal Frequency for 5V and 3.3V Operation.

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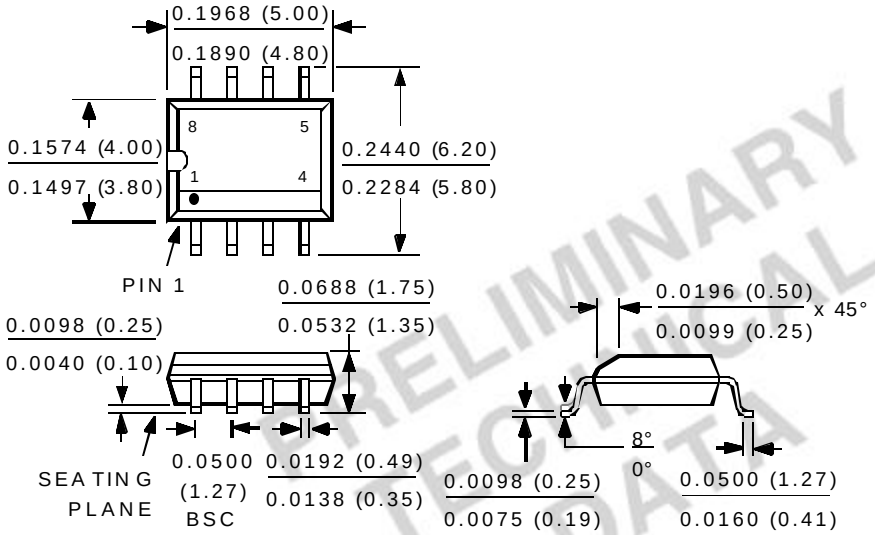
Package Outline Drawing:

8-Lead Small Outline
(R-8)



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Application Information

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