MicroConverter™, Dual-Channel 16&24 bit ADCs with Embedded MCU

Preliminary Technical Data — ADuC824

FEATURES

HIGH RESOLUTION SIGMA DELTA ADCS
- 2 Independent Channels (16 and 24-bit resolution)
- Programmable Gain Front End
- 24-bit No Missing Codes - Main ADC
- 13-bit Pk-Pk Resolution @ 20Hz, 20mV Range
- 18-bit Pk-PK Resolution @ 20Hz, 2.56V Range

MEMORY
- 8K Bytes On-Chip Flash/EE Program Memory
- 640 Bytes On-Chip Flash/EE Data Memory
- 256 Bytes On-Chip Data RAM

8051 BASED CORE
- 8051 Compatible Instruction Set (12.58MHz Max)
- 32kHz External Crystal with on board PLL
- Three 16 bit Timer/Counters
- 26 Programmable I/O lines
- 12 interrupt sources, two priority levels

POWER
- Specified for 3V and 5V operation
- Normal : 3mA @ 3V (Core CLK=1.5MHz)
- Powerdown : 20uA (32kHz Crystal Running)

On-Chip PERIPHERALS
- On-Chip Temperature Sensor
- 12-bit Voltage Output DAC
- Dual Excitation Current Sources
- Reference Detect Circuit
- Timer Interval Counter (TIC)
- UART Serial I/O
- 2 Wire(I2C® Compatible) and SPI® Serial I/O
- Watchdog Timer (WDT)
- Power Supply Monitor (PSM)

GENERAL DESCRIPTION

The ADuC824 is a complete smart transducer front-end incorporating dual high-resolution sigma delta ADCs, temperature sensor, PGA, 8-bit MCU, Flash Memory, RAM and timer/counters. The device accepts low-level signals directly from a transducer.

The device operates from a 32kHz crystal with an on-board PLL generating the required internal operating frequency. The output data rate from the part is programmable as is the MCU core operating frequency. The output resolution from the part varies with the programmed gain and output data rate.

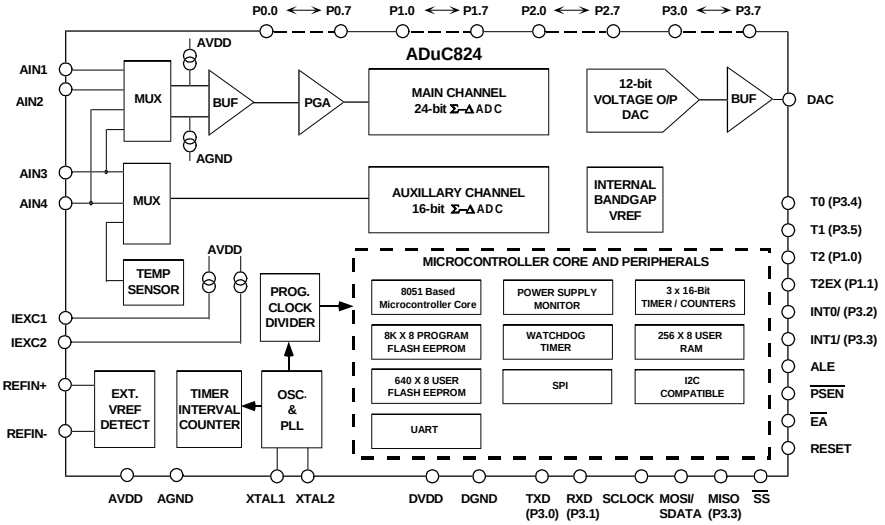
The microcontroller core is 8051 instruction set compatible. On-Chip peripherals include an SPI and I2C compatible serial ports, multiple digital input/output ports, watchdog timer, power supply monitor and timer interval counter. 8K bytes of Flash/EE program memory are provided on-chip. 640 bytes of Flash/EE data memory and 256 bytes RAM are also incorporated on-chip.

The part operates from a single +3V or +5V supply. When operating from +3V supplies, the power dissipation for the part is 10mW. The ADuC824 is housed in a 52-pin PQFP package.

APPLICATIONS

Intelligent Sensors (IEEE1451.2 Compatible)
Weigh Scales
Portable Instrumentation
Pressure Measurements
4-20mA transmitters

FUNCTIONAL BLOCK DIAGRAM



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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

ADuC824–SPECIFICATIONS[1,2]

(AV_{DD} = +3V or +5.0V , DV_{DD} = +3V or +5.0V, REFIN(+) = +2.5V; REFIN(-) = AGND; AGND = DGND = 0V; XTAL1/XTAL2 = 32 kHz Crystal; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	ADuC824BS	Units	Test Conditions
ADC CHANNEL SPECIFICATIONS			
Conversion Rate	5.4Hz min.	Hz	On both Channels
	105Hz max.	Hz	0.021Hz (0.732msec.) increments
Main Channel			
No Missing Codes	24	bits min.	20Hz Update Rate
Resolution	13	bits pk-pk	±20mV range, 20Hz Update Rate
	18	bits pk-pk	±2.56V range, 20Hz Update Rate
Output Noise and Update Rates	See Tables Below in ADC Description		
Integral Nonlinearity	15	ppm of FSR max.	
Offset Error	TBD		
Offset Error Drift	10	nV/°C typ.	
Gain Error	TBD		
Gain Error Drift	1	ppm/°Ctyp.	
Power Supply Rejection(PSR)	90	dBs min.	Input Range = ±20mV
	90	dBs min.	Input Range = ±2.56V
Common Mode Rejection(CMR)			
On AIN	90	dBs min.	At DC, Range = ±20mV
On AIN	90	dBs min.	At DC, Range = ±2.56V
On REFIN	90	dBs min.	At DC, Range = ±20mV
Analog Input Current			
DC Bias Current	1	nA max.	
DC Bias Current Drift	TBD	nA typ.	
DC Offset Current	TBD	nA typ.	
DC Offset Current Drift	TBD	nA typ.	
Auxiliary Channel			
No Missing Codes	16	bits min.	
Resolution	16	bits pk-pk	±2.5V range, 20Hz Update Rate
Output Noise and Update Rates	See Tables Below in ADC Description		
Integral Nonlinearity	60	ppm of FSR max.	
Offset Error	TBD		
Offset Error Drift	10	nV/°C typ.	
Gain Error	TBD		
Gain Error Drift	1	ppm/°Ctyp.	
Power Supply Rejection(PSR)	90	dBs min.	Input Range = ±2.5V
Common Mode Rejection(CMR)			
On AIN	90	dBs min.	At DC, Input Range = ±2.5V
On REFIN	90	dBs min.	At DC, Input Range = ±2.5V
Analog Input Current			
DC Bias Current	TBD	nA max.	
DC Bias Current Drift	TBD	nA typ.	
DC Offset Current	TBD	nA typ.	
DC Offset Current Drift	TBD	nA typ.	
INTERNAL/EXTERNAL REFERENCE			
Internal Reference			
ADC Reference			
Reference Voltage	1.25±1%	V min/max.	
Power Supply Rejection	TBD	dBs typ.	
Reference Tempco	40	ppm/°C typ.	
DAC Reference			
Reference Voltage	2.5±1%	V min/max.	
Power Supply Rejection	TBD	dBs typ.	
Reference Tempco	40	ppm/°C typ.	
External Reference Input			
REFIN(+) to REFIN(-) Voltage	+2.5	V nom.	
REFIN(+) to REFIN(-) Range	+1	V min.	
	AV_{DD}	V max.	
'NO Ext. REF' Trigger Voltage	0.3	V min.	NOXREF bit active if VREF<0.3V
	0.65	V max.	NOXREF bit inactive if VREF>0.65V

PARAMETER	ADuC824BS	Units	Test Conditions
DAC CHANNEL PERFORMANCE			
DC Specifications			
Resolution	12	bits	
Relative Accuracy	±3	LSB typ.	
Differential Nonlinearity	±0.5	LSB max.	Guaranteed 12-Bit Monotonic
Offset Error	±50	mV max.	
Full-Scale Error	±25	mV max.	
AC Specifications			
Voltage Output Settling Time	15	µsec typ.	Settling Time to 1 LSB of Final Value.
Digital to Analog Glitch Energy	10	nVsec typ.	1 LSB change at major carry
ANALOG INPUTS/REFERENCE INPUTS			
Main Channel			
Normal Mode 50Hz/60Hz Rejection	60	dBs min.	50/60Hz ±1Hz , 20Hz Update Rate
Common Mode 50/60Hz Rejection	90	dBs min.	50/60Hz ±1Hz, Range = ±20mV
	90	dBs min.	50/60Hz ±1Hz, Range = ±2.56V
Differential Input Voltage Ranges			RN2, RN1, RN0 of ADOCON set to
	±20	mV nom.	0 0 0
	±40	mV nom.	0 0 1
	±80	mV nom.	0 1 0
	±160	mV nom.	0 1 1
	±320	mV nom.	1 0 0
	±640	mV nom.	1 0 1
	±1.28	V nom.	1 1 0
	±2.56	V nom.	1 1 1
ADC Range Matching	5	uV typ.	
Absolute Ain Voltage Limits	AGND+50mV	V min.	
	AV_{DD}-50mV	V max.	
Aux Channel			
Normal Mode 50Hz/60Hz Rejection	60	dBs min.	50/60Hz rejection, 20Hz Update Rate
Input Voltage Range	±2.5	V nom.	
Absolute Ain Voltage Limits	AGND-30mV	V min.	
	AV_{DD}+30mV	V max.	
External Reference Input			
Common Mode 50/60Hz Rejection	TBD	dBs min.	50/60Hz ±1Hz, Range = ±20mV
Reference DC Input Current	TBD	µA typ.	
LOGIC INPUTS			
All Inputs Except SCLOCK and XTAL1			
V_{INL}, Input Low Voltage	0.8	V max.	DV_{DD} = 5V
V_{INL}, Input Low Voltage	0.4	V max.	DV_{DD} = 3V
V_{INH}, Input High Voltage	2.0	V min.	
SCLOCK Only (Schmitt Triggered Input)			
V_{T+}	1.4/3	V min/V max	DV_{DD} = 5V
V_{T+}	0.95/2.5	V min/V max	DV_{DD} = 3V
V_{T-}	0.8/1.4	V min/V max	DV_{DD} = 5V
V_{T-}	0.4/1.1	V min/V max	DV_{DD} = 3V
V_{T+}	0.4/0.85	V min/V max	DV_{DD} = 5V
V_{T+}	0.4/0.85	V min/V max	DV_{DD} = 3V
XTAL1 Only			
V_{INL}, Input Low Voltage	0.8	V max.	DV_{DD} = 5V
V_{INL}, Input Low Voltage	0.4	V max.	DV_{DD} = 3V
V_{INH}, Input High Voltage	3.5	V min.	DV_{DD} = 5V
V_{INH}, Input High Voltage	2.5	V min.	DV_{DD} = 3V
Input Currents			
Input Leakage Current (Port 0, $\overline{EA}$)	±10	µA max.	V_{IN} = 0V or V_{DD}
Logic 1 Input Current	±10	µA max.	V_{IN} = V_{DD}, All Digital Inputs
Logic 1-0 Transition Current	-700	µA max.	V_{IN} = 2V, P1.0, P1.1, Ports 2 & 3
Logic 0 Input Current	-80	µA max.	V_{IN} = 450mV, P1.0, P1.2, Ports 2 & 3
Input Capacitance	10	pF typ.	All Digital Inputs

PARAMETER	ADuC824BS	Units	Test Conditions
ANALOG (DAC) OUTPUTS			
Voltage Range	0 to V_{REF}	V typ.	DACRN = 0 in DACCON SFR
	0 to AV_{DD}	V typ.	DACRN = 1 in DACCON SFR
Resistive Load	10	KΩ typ.	
Capacitive Load	100	pF typ.	
Output Impedance	0.5	Ω typ.	
I_{SINK}	50	uA typ.	
LOGIC OUTPUTS (Not Including XTAL2)			
V_{OH}, Output High Voltage	2.4	V min.	V_{DD} = 5V, I_{SOURCE} = 80µA
V_{OH}, Output High Voltage	2.4	V min.	V_{DD} = 3V, I_{SOURCE} = 20µA
V_{OL}, Output Low Voltage	0.4	V max.	I_{SINK} = 8mA, SCLOCK,SDATA/MOSI
V_{OL}, Output Low Voltage	0.4	V max.	I_{SINK} = 10mA, P1.0 and P1.1
V_{OL}, Output Low Voltage	0.4	V max.	I_{SINK} = 1.6mA, All Other Outputs
Floating State Leakage Current	±10	uA max.	
Floating State Output Capacitance	±10	pF typ.	
TEMPERATURE SENSOR			
Accuracy	±2	°C typ.	
Thermal Impedance (θ_{JA})	90	°C/W typ.	
TRANSDUCER BURNOUT			
AIN1 Current	-100	nA typ.	
AIN2 Current	100	nA typ.	
Initial Tolerance @ 25°C	±10	% typ.	
Drift	0.1	%/°C typ.	
EXCITATION CURRENT SOURCES (IEXC1 and IEXC2)			
Output Current	200	µA nom.	
Initial Tolerance at 25°C	±10	% typ.	
Drift	20	ppm/°C typ.	
Initial Current Matching at 25°C	±0.1	%	Matching between IEXC1 and IEXC2
Drift Matching	1	ppm/°C typ.	
Line Regulation (AV_{DD})	TBD	nA/V max.	AV_{DD} = 5V
Load Regulation	TBD	nA/V max.	
Output Compliance	AV_{DD}-0.5	V max.	
SYSTEM CALIBRATION			
Full-Scale Calibration Limit	1.05 X FS	V max.	
Zero-Scale Calibration Limit	-1.05 X FS	V min.	
Input Span	0.8 X FS	V min.	
	2.1 X FS	V max.	
WATCHDOG TIMER			
Timeout Period	0	ms min.	9 timeout periods in this range
	2000	ms max.	programmed via PRE3-0 in WDCON
POWER SUPPLY MONITOR			
AV_{DD} Trip Point Selection Range	2.63	V min.	4 trip points selectable in this range
	4.63	V max.	programmed via TPA1-0 in PSMCON
AV_{DD} Power Supply Trip Point Accuracy	±2.5	% max.	
DV_{DD} Trip Point Selection Range	2.63	V min.	4 trip points selectable in this range
	4.63	V max.	programmed via TPD1-0 in PSMCON
DV_{DD} Power Supply Trip Point Accuracy	±2.5	% max.	

PARAMETER	ADuC824BS	Units	Test Conditions
FLASH/EE MEMORY PERFORMANCE			
Endurance	10,000	Cycles min.	JEDEC Specification A117
Data Retention	25	Years min.	JEDEC Specification A103
MCU CORE CLOCK RATE			Clock rate generated via on-chip PLL
MCU Clock Rate	98.3	kHz min.	Programmable via CD2-0 in PLLCON
	12.58	MHz max.	
START UP TIME			
From Power-On	500	msec typ.	
From Idle Mode	1	msec. typ.	
From Power-Down Mode	1	msec. typ.	Osc. not powered down via OSCEN bit
	500	msec. typ.	Osc. powered down via OSCEN bit
From WDT Reset	1	msec typ.	Controlled via WDCON SFR
POWER REQUIREMENTS			DV_{DD} and AV_{DD} can be set independently
Power Supply Voltages			
AV_{DD} - AGND	2.7	V min.	AV_{DD} = 3V nom.
	3.3	V max.	AV_{DD} = 3V nom.
	4.5	V min.	AV_{DD} = 5V nom.
	5.5	V max.	AV_{DD} = 5V nom.
DV_{DD} - DGND	2.7	V min.	DV_{DD} = 3V nom.
	3.3	V max.	DV_{DD} = 3V nom.
	4.5	V min.	DV_{DD} = 5V nom.
	5.5	V max.	DV_{DD} = 5V nom.
Power Supply Currents			Core CLK=1.573MHz
DV_{DD} Current (Normal Mode)	2	mA max.	DV_{DD}=3V
DV_{DD} Current (Normal Mode)	4	mA max.	DV_{DD}=5V
AV_{DD} Current (Normal Mode)	1	mA max.	AV_{DD}=3V or 5V
DV_{DD} Current (Idle Mode)	750	µA max.	DV_{DD}=3V
DV_{DD} Current (Idle Mode)	1	mA max.	DV_{DD}=5V
AV_{DD} Current (Idle Mode)	200	µA max.	AV_{DD}=3V or 5V
DV_{DD} Current (Power-Down Mode)	20	µA max.	DV_{DD}=3V, 32.768kHz Osc. Running
DV_{DD} Current (Power-Down Mode)	30	µA max.	DV_{DD}=5V, 32.768kHz Osc. Running
AV_{DD} Current (Power-Down Mode)	5	µA max.	AV_{DD}=3V or 5V
Power Supply Currents			Core CLK= 12.582912MHz
DV_{DD} Current (Normal Mode)	TBD	mA	DV_{DD}=3V
DV_{DD} Current (Normal Mode)	TBD	mA	DV_{DD}=5V
AV_{DD} Current (Normal Mode)	TBD	mA	AV_{DD}=3V or 5V
DV_{DD} Current (Idle Mode)	TBD	mA	DV_{DD}=3V
DV_{DD} Current (Idle Mode)	TBD	mA	DV_{DD}=5V
AV_{DD} Current (Idle Mode)	TBD	mA	AV_{DD}=3V or 5V
DV_{DD} Current (Power-Down Mode)	20	µA max.	DV_{DD}=3V, 32.768kHz Osc. Running
DV_{DD} Current (Power-Down Mode)	30	µA max.	DV_{DD}=5V, 32.768kHz Osc. Running
AV_{DD} Current (Power-Down Mode)	5	µA max.	AV_{DD}=3V or 5V

NOTES
[1] Specifications apply after calibration.
[2] Temperature Range -40'C to +85'C.
Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

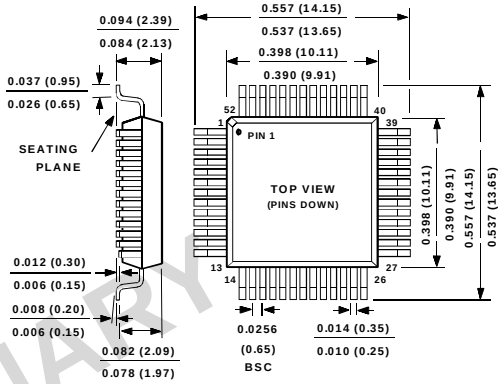
AV_{DD} to AGND.....-0.3V to +7V
AV_{DD} to DGND.....-0.3V to +7V
DV_{DD} to AGND.....-0.3V to+7V
DV_{DD} to DGND.....-0.3V to +7V
AGND to DGND.....-5V to +0.3V
AV_{DD} to DV_{DD}.....-2V to +5V
Analog Input Voltage to AGND.....-0.3V to AV_{DD} +0.3V
Reference Input Voltage to AGND...-0.3V to AV_{DD} +0.3V
AIN/REFIN Current (Indefinite).....30mA
Digital Input Voltage to DGND.....-0.3V to DV_{DD} +0.3V
Digital Output Voltage to DGND...-0.3V to DV_{DD} +0.3V
Operating Temperature Range.....-40°C to 85°C
Storage Temperature Range.....-65°C to 150°C
Junction Temperature.....+150°C
52PQFP Power Dissipation.....TBD mW
θ_{JA} Thermal Impedance.....90°C/W
Lead Temperature, Soldering
Vapor Phase (60sec).....+215°C
Infrared (15 sec).....+220°C

[1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

52-Lead Plastic Quad Flatpack
(S-52)



CAUTION

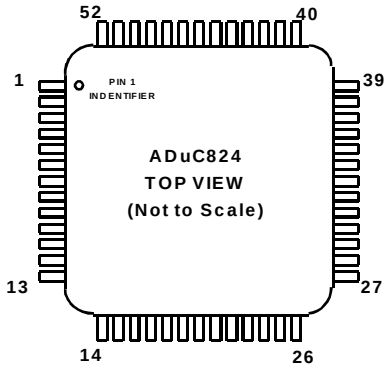
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the XX0000 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADuC824BS	-40°C to +85°C	52-Lead Plastic Quad Flatpack	S-52

QuickStart Development System Model	Description
Eval-ADuC824QS	Development System for the ADuC824 MicroConverter, containing: - Evaluation Board - Serial Port Cable - Plugin Power Supply - Serial Downloader - Debugger - Assembler and Evaluation C-Compiler - Example Code - Documentation

PIN CONFIGURATION



52 PIN PQFP

52 PQFP	Pin Name
1	P1.0/T2
2	P1.1/T2EX
3	P1.2/IEXC1
4	P1.3/IEXC2
5	AV_{DD}
6	AGND
7	REFIN(-)
8	REFIN(+)
9	P1.4/AIN1
10	P1.5/AIN2/DAC
11	P1.6/AIN3/IEXC*
12	P1.7/AIN4/DAC
13	$\overline{SS}$
14	MISO
15	RESET
16	P3.0/RxD
17	P3.1/TxD
18	P3.2/$\overline{INT0}$
19	P3.3/$\overline{INT1}$
20	DV_{DD}
21	DGND
22	P3.4/T0
23	P3.5/T1
26	P3.6/$\overline{WR}$
25	P3.7/RD
26	SCLOCK

52 PQFP	Pin Name
27	SDATA/MOSI
28	P2.0/A8/A16
29	P2.1/A9/A17
30	P2.2/A10/A18
31	P2.3/A11/A19
32	XTAL1 (Input)
33	XTAL2 (Output)
34	DV_{DD}
35	DGND
36	P2.4/A12/A20
37	P2.5/A13/A21
38	P2.6/A14/A22
39	P2.7/A15/A23
40	$\overline{EA}/V_{PP}$
41	$\overline{PSEN}$
42	ALE
43	P0.0/AD0
44	P0.1/AD1
45	P0.2/AD2
46	P0.3/AD3
47	DGND
48	DV_{DD}
49	P0.4/AD4
50	P0.5/AD5
51	P0.6/AD6
52	P0.7/AD7

* Any combination of IEXC1 and IEXC2 can be switched to this pin.

ADUC824 ARCHITECTURE, MAIN FEATURES

The ADuC824 is a complete smart transducer front-end incorporating dual high-resolution sigma delta ADCs, temperature sensor, PGA, 8-bit MCU, Flash Memory, RAM and timer/counters. The device accepts low-level signals directly from a transducer.

The device operates from a 32kHz crystal with an on-board PLL generating the required internal core operating frequency. The output data rate from the part is programmable as is the MCU core operating frequency. The output resolution from the part varies with the programmed gain and output rate.

The microcontroller core is 8051 instruction set compatible. On-Chip peripherals include an SPI-compatible serial port, multiple digital input/output ports, watchdog timer, power supply monitor and interval counter. 8K bytes of non-volatile program FLASH memory are provided on-chip. 640 bytes of non-volatile data FLASH memory and 256 bytes RAM are also incorporated on-chip.

ADUC824 MEMORY ORGANIZATION

As with all 8051-compatible devices, the ADuC824 has separate address spaces for Program and Data memory as shown in Figure 1 and Figure 2 below. If the user applies power or resets the device while the EA pin is pulled low then the part will execute code from the external program space, otherwise the part defaults to code execution from its internal 8K Byte Flash/EE program memory. This internal code space can be downloaded while the device is in-circuit.

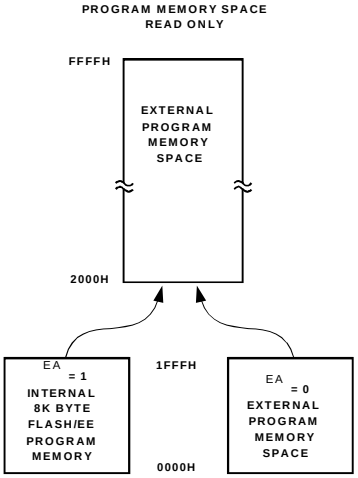


Figure 1. ADuC824 Program Memory Map

Also shown in Figure 2, an additional 640 Bytes of Flash/EE Data Memory are available to the user. This Flash/EE Data Memory area is accessed indirectly via a group of control registers mapped in the Special Function Register (SFR) area.

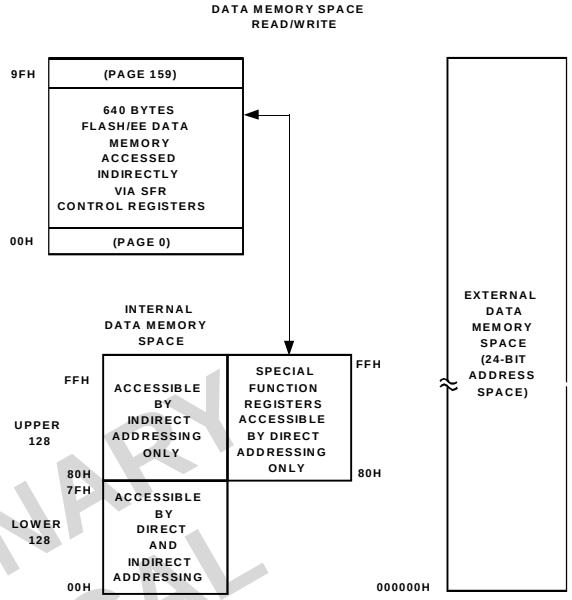


Figure 2. ADuC824 Data Memory Map

The lower 128 bytes of internal data memory are mapped as shown in Figure 3. The lowest 32 bytes are grouped into four banks of eight registers addressed as R0 through R7. The next 16 bytes (128 bits) above the register banks form a block of bit addressable memory space at bit addresses 00H through 7FH.

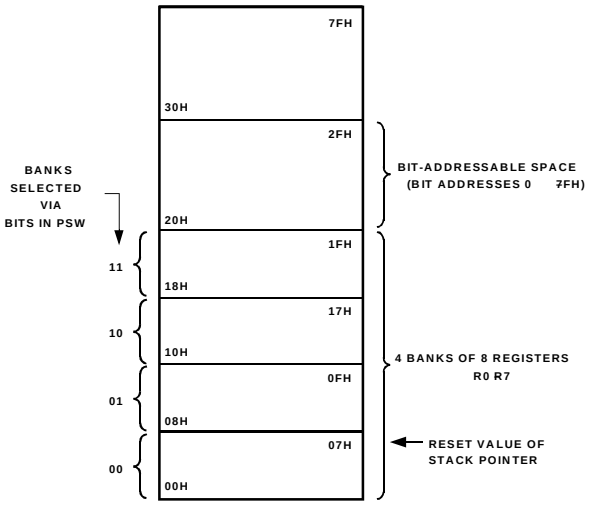


Figure 3. ADuC824 Lower 128 Bytes of Internal Data Memory

The SFR space is mapped to the upper 128 bytes of internal data memory space and is accessed by direct addressing only. It provides an interface between the CPU and all on-chip peripherals. A block diagram showing the programming model of the ADuC824 via the SFR area is shown in Figure 4. A complete SFR map is shown in Figure 5 overleaf.

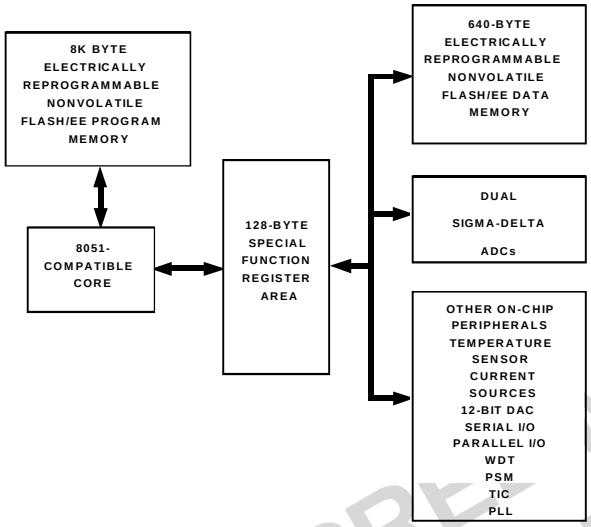


Figure 4. ADuC824 Lower 128 Bytes of Internal Data Memory

OVERVIEW OF MCU RELATED SFRS

Accumulator SFR

ACC is the Accumulator register and is used for math operations including addition, subtraction, integer multiplication and division, and Boolean bit manipulations. The mnemonics for Accumulator specific instructions refer to the Accumulator as A.

B SFR

The B register is used with the ACC for multiplication and division operations. For other instructions it can be treated as a general purpose scratchpad register.

Stack Pointer SFR

The SP register is the stack pointer and is used to hold an internal RAM address that is called the ′ top of the stack′. The SP register is incremented before data is stored during PUSH and CALL executions. While the Stack may reside anywhere in on-chip RAM, the SP register is initialized to 07 after a reset. This causes the stack to begin at location 08H.

Data Pointer

The DPTR register is the Data Pointer and is made up of three 8 bit registers, named DPP (page byte), DPH (high byte) and DPL (low byte). These are used to provide memory addresses for internal and external code access and external data access. It may be manipulated as a 24 bit register (DPTR) or as three independent 8 bit registers (DPP, DPH, DPL).

Program Status Word SFR

The PSW register is the Program Status Word which contains several bits reflecting the current state of the CPU as detailed in Table 1 below.

SFR Address D0H
Power ON Default Value 00H
Bit Addressable Yes

CY	AC	F0	RS1	RS0	OV	F1	P

Table I. PSW SFR Bit Designations

Bit Location	Bit Mnemonic	Description
PSW.7	CY	Carry Flag
PSW.6	AC	Auxiliary Carry Flag
PSW.5	F0	General Purpose Flag
PSW.4	RS1	Register Bank Select Bits
PSW.3	RS0	**RS1 RS0 Selected Bank** 0 0 0 0 1 1 1 0 2 1 1 3
PSW.2	OV	Overflow Flag
PSW.1	F1	General Purpose Flag
PSW.0	P	Parity Bit

Power Control SFR

The Power Control (PCON) register contains bits for power saving options and general purpose status flags as shown in table 2.

SFR Address 87H
Power ON Default Value 00H
Bit Addressable No

SMOD	SERIPD	INT0PD	ALEOFF	GF1	GF0	PD	IDL

Table II. PCON SFR Bit Designations

Bit Location	Bit Mnemonic	Description
PCON.7	SMOD	Double UART Baud Rate
PCON.6	SERIPD	I2C/SPI Power Down Interrupt Enable.
PCON.5	INT0PD	INT0 Power Down Interrupt Enable.
PCON.4	ALEOFF	Disable ALE Output
PCON.3	GF1	General Purpose Flag Bit
PCON.2	GF0	General Purpose Flag Bit
PCON.1	PD	Power Down Mode Enable
PCON.0	IDL	IDLE Mode Enable

SPECIAL FUNCTION REGISTERS

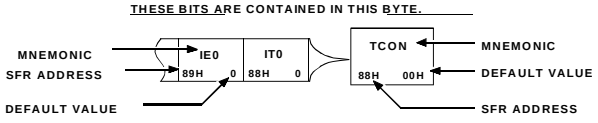
All registers except the program counter and the four general purpose register banks, reside in the special function register (SFR) area. The SFR registers include control, configuration and data registers that provide an interface between the CPU and other on-chip peripherals.

Figure 4 shows a full SFR memory map and SFR contents on Reset; NOT USED indicates unoccupied SFR locations. Unoccupied locations in the SFR address space are not implemented; i.e., no register exists at this location. If an unoccupied location is read, an unspecified value is returned. SFR locations reserved for on-chip testing are shaded (RESERVED) and should not be accessed by user software.

ISPI FFH 0	WCOL FEH 0	SPE FDH 0	SPIM FCH 0	CPOL FBH 0	CPHA FAH 0	SPR1 F9H 0	SPR0 F8H 0	BITS
F7H 0	F6H 0	F5H 0	F4H 0	F3H 0	F2H 0	F1H 0	F0H 0	BITS
MDO EFH 0	MDE EEH 0	MCO EDH 0	MDI ECH 0	I2CM EBH 0	I2CRS EAH 0	I2CTX E9H 0	I2CI E8H 0	BITS
E7H 0	E6H 0	E5H 0	E4H 0	E3H 0	E2H 0	E1H 0	E0H 0	BITS
RDY0 DFH 0	RDY1 DEH 0	CAL DDH 0	NOXREF DCH 0	ERR0 DBH 0	ERR1 DAH 0	D9H 0	D8H 0	BITS
CY D7H 0	AC D6H 0	F0 D5H 0	RSI D4H 0	RS0 D3H 0	OV D2H 0	FI D1H 0	P D0H 0	BITS
TF2 CFH 0	EXF2 CEH 0	RCLK CDH 0	TCLK CCH 0	EXEN2 CBH 0	TR2 CAH 0	CNT2 C9H 0	CAP2 C8H 0	BITS
PRE3 C7H 0	PRE2 C6H 0	PRE1 C5H 0	PRE0 C4H 0	WDIR C3H 0	WDS C2H 0	WDE C1H 0	WDWR C0H 0	BITS
PS1 BFH 0	PADC BEH 0	PT2 BDH 0	PS BCH 0	PT1 BBH 0	PX1 BAH	PT0 B9H 0	PX0 B8H 0	BITS
RD B7H 1	WR B6H 1	T1 B5H 1	T0 B4H 1	INT1 B3H 1	INT0 B2H 1	TxD B1H 1	RxD B0H 1	BITS
EA AFH	EADC AEH	ET2 ADH	ES ACH 0	ET1 ABH 0	EX1 AAH	ET0 A9H 0	EX0 A8H 0	BITS
A7H	A6H	A5H 1	A4H 1	A3H 1	A2H 1	A1H 1	A0H 1	BITS
SM0 9FH 0	SM1 9EH 0	SM2 9DH 0	REN 9CH 0	TB8 9BH 0	RB8 9AH 0	T1 99H 0	R1 98H 0	BITS
97H 0	96H 0	95H 0	94H 0	93H 0	92H 0	T2EX 91H 0	T2 90H 0	BITS
TF1 8FH 0	TR1 8EH 0	TF0 8DH 0	TR0 8CH 0	IE1 8BH 0	IT1 8AH 0	IE0 89H 0	IT0 88H 0	BITS
87H 1	86H 1	85H 1	84H 1	83H 1	82H 1	81H 1	80H 1	BITS

SPICON[1] F8H 04H	RESERVED	RESERVED	DACL FBH 00H	DACH FCH 00H	DACCON FDH 00H	RESERVED	RESERVED
B[1] F0H 00H	RESERVED	RESERVED	NOT USED	RESERVED	RESERVED	RESERVED	SPIDAT F7H 00H
I2CCON[1] E8H 00H	GNOL[4] E9H 55H	GNOM[4] EAH 55H	GNOH[4] EBH 53H	GN1L[4] ECH 55H	GN1H[4] EDH 55H	RESERVED	RESERVED
ACC[1] E0H 00H	OF0L[4] E1H 00H	OF0M[4] E2H 00H	OF0H[4] E3H 80H	OF1L[4] E4H 00H	OF1H[4] E5H 80H	RESERVED	RESERVED
ADSTAT[1] D8H 00H	AD0L D9H 00H	AD0M DAH 00H	AD0H DBH 00H	AD1L DCH 00H	AD1H DDH 00H	RESERVED	PSMCON DFH DEH
PSW[1] D0H 00H	ADMODE D1H 00H	AD0CON D2H 07H	AD1CON D3H 00H	SF D4H 45H	ICON D5H 00H	RESERVED	PLLCON D7H 03H
T2CON[1] C8H 00H	RESERVED	RCAP2L CAH 00H	RCAP2H CBH 00H	TL2 CCH 00H	TH2 CDH 00H	RESERVED	RESERVED
WDCON[1] C0H 00H	RESERVED	CHIPID[3] C2H 02H	RESERVED	RESERVED	RESERVED	EADRL C6H 00H	RESERVED
IP[1] B8H 00H	ECON B9H 00H	RESERVED	RESERVED	EDATA1 BCH 00H	EDATA2 BDH 00H	EDATA3 BEH FFH	EDATA4 BFH FFH
P3[1] B0H FFH	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	NOT USED
IE[1] A8H 00H	IEIP2 A9H A0H	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
P2[1] A0H FFH	TIMECON A1H 00H	HTHSEC A2H 00H	SEC A3H 00H	MIN A4H 00H	HOUR A5H 00H	INTVAL A6H 00H	NOT USED
SCON[1] 98H 00H	SBUF 99H 00H	I2CDAT 9AH 00H	I2CADD 9BH 55H	NOT USED	NOT USED	NOT USED	NOT USED
P1[1,2] 90H FFH	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED
TCON[1] 88H 00H	TMOD 89H 00H	TL0 8AH 00H	TL1 8BH 00H	TH0 8CH 00H	TH1 8DH 00H	RESERVED	RESERVED
P0[1] 80H FFH	SP 81H 07H	DPL 82H 00H	DPH 83H 00H	DPP 84H 00H	RESERVED	RESERVED	PCON 87H 00H

SFR MAP KEY :



SFR NOTES :

1 SFRs WHOSE ADDRESS ENDS IN 0H OR 8H ARE BIT ADDRESSABLE.

2 ONLY P1.0 AND P1.1 CAN OPERATE AS DIGITAL I/O PINS. P1.2 - P1.7 CAN BE CONFIGURED AS ANALOG INPUTS (I.E. ADC INPUTS) OR DIGITAL INPUTS.

3 THE CHIPID SFR CONTAINS THE SILICON REVISION ID BYTE AND MAY CHANGE FOR FUTURE SILICON REVISIONS.

4 THESE REGISTERS ARE RECONFIGURED AT POWER-ON WITH FACTORY CALCULATED CALIBRATION COEFFICIENTS, WHICH CAN BE OVERWRITTEN BY USER CODE. SEE CALIBRATION OPTIONS IN ADMODE SFR.

Figure 4. ADuC824 Special Function Register Locations and Reset Values

DUAL CHANNEL ADC CIRCUIT INFORMATION

Overview

The ADuC824 incorporates two independent Sigma-Delta ADC channels (Main and Auxiliary) with on-chip digital filtering intended for the measurement of wide dynamic range, low frequency signals such as those in weigh-scale, strain-gauge, pressure transducer or temperature measurement applications.

Main Channel :

This channel is intended to convert the primary sensor input. The channel is buffered and can be programmed for one of 8 input ranges from ±20mV to ±2.56V being driven from one of two differential inputs Ain1/2 or Ain3/4. Buffering the input channel means that the part can handle significant source impedances on the analog input and that R, C filtering (for noise rejection or RFI reduction) can be placed on the analog inputs if required. Sensor burnout currents can also be turned on. These currents can be used to check that a transducer is still operational before attempting to take measurements.

The ADC employs a sigma-delta conversion technique to realize up to 24 bits of no missing codes performance. The sigma-delta modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. A Sinc^3 programmable low pass filter is then employed to decimate the modulator output data stream to give a valid data conversion result at programmable output rates from 5.35Hz (186.77mS) to 105.03Hz (9.52mS). A Chopping scheme is also employed to minimize ADC channel offset errors. A block diagram of the Main ADC input channel is shown in Figure 5 below.

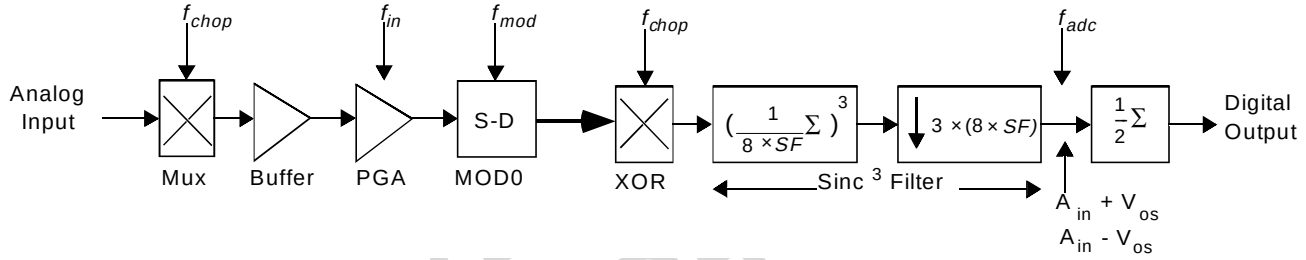


Figure 5. ADuC824 Main ADC Channel Block Diagram

Auxiliary Channel :

The Auxiliary (Aux) channel is intended to convert supplementary inputs such as from a cold junction diode or thermistor. This channel is not buffered and has a fixed input range of ±2.5V. The single-ended inputs can be driven from Ain3 or Ain4 pins or directly from the on-chip temperature sensor voltage output. A block diagram of the Auxillary ADC channel is shown in Figure 6 below.

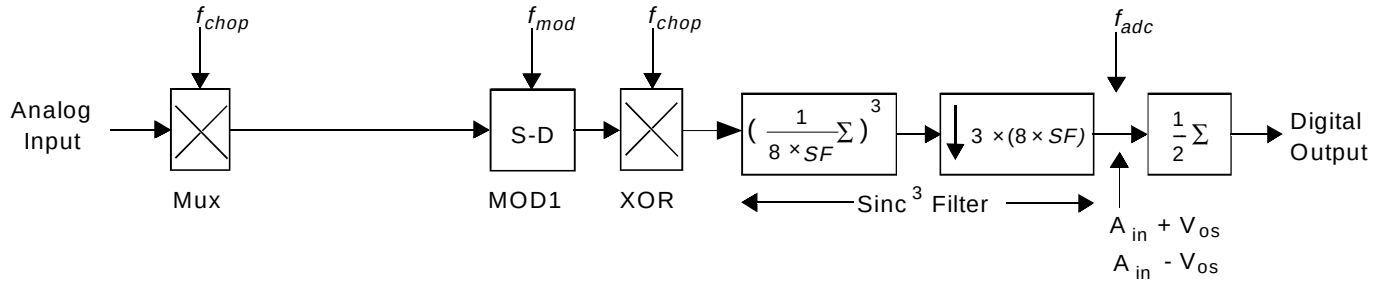


Figure 6. ADuC824 Auxillary ADC Channel Block Diagram

MAIN AND AUXILIARY ADC NOISE PERFORMANCE

Tables III and IV below show the output rms noise and output peak-to-peak resolution in bits (rounded to the nearest 0.5LSB) for some typical output update rates on both the Main and Aux. ADCs. The numbers are typical and generated at a differential input voltage of 0V. The output update rate is selected via the SF7-SF0 bits in the Sinc Filter (SF) SFR. It is important to note that the peak-to-peak resolution figures represent the resolution for which there will be no code flicker within a six-sigma limit.

Typical Output RMS Noise vs. Input Range and Update Rate
Output RMS Noise in µV

SF Word	Data Update Rate (Hz)	Input Range ±20mV	±40mV	±80mV	±160mV	±320mV	±640mV	±1.24V	±2.56V
13	105.3	1.50	1.50	1.60	1.75	3.50	4.50	6.70	11.75
69	19.79	0.60	0.65	0.65	0.65	0.65	0.95	1.40	2.30
255	5.35	0.35	0.35	0.37	0.37	0.37	0.51	0.82	1.25

Peak-to-Peak Resolution vs. Input Range and Update Rate
Peak-to-Peak Resolution in Bits

SF Word	Data Update Rate (Hz)	Input Range ±20mV	±40mV	±80mV	±160mV	±320mV	±640mV	±1.24V	±2.56V
13	105.3	12	13	14	15	15	15.5	16	16
69	19.79	13	14	15	16	17	17.5	18	18.5
255	5.35	14	15	16	17	18	18.5	18.8	19.2

Table III. MAIN ADC

Typical Output RMS Noise vs. Update Rate
Output RMS Noise in µV

SF Word	Data Update Rate (Hz)	Input Range ±2.5V
13	105.3	10.75
69	19.79	2.00
255	5.35	1.15

Peak-to-Peak Resolution vs. Update Rate
Peak-to-Peak Resolution in Bits

SF Word	Data Update Rate (Hz)	Input Range ±2.5V
13	105.3	16
69	19.79	18.5
255	5.35	19.5

Table IV. Auxiliary ADC

Notes :

- In the following descriptions, ***SET*** implies a logic 1 state and ***CLEARED*** implies a logic 0 state unless otherwise stated.
- In the following descriptions, ***SET*** and ***CLEARED*** also imply that the bit is set or cleared automatically by the ADuC824 hardware unless otherwise stated.
- User software ***should not*** write '1's to reserved or un-implemented bits as they may be used in future products.

SFR INTERFACE TO THE ADC CHANNELS

Both ADC channels are controlled and configured via a number of SFRs which are mentioned here and described in more detail in the following pages.

ADSTAT: ADC Status Register, holds general status of the Main and Aux ADCs.
ADMODE: ADC Mode Register, controls general modes of operation for Main and Aux ADCs.
AD0CON: Main ADC Control Register, controls specific configuration of Main ADC.
AD1CON: Aux ADC Control Register, controls specific configuration of Aux ADC.
SF : Sinc Filter Register, Configures the decimation factor for the $Sinc^3$ filter and thus the Main and Aux ADC update rates.
ICON: Current Source Control Register, Allows user control of the various on-chip current source options.
AD0L/M/H: Main ADC 24-bit conversion result held in these three 8-bit registers.
AD1L/H: Aux ADC 16-bit conversion result held in these two 8-bit registers.
OF0L/M/H: Main ADC 24-bit Offset Calibration Coefficient held in these three 8-bit registers.
OF1L/H: Aux ADC 16-bit Offset Calibration Coefficient held in these two 8-bit registers.
GN0L/M/H: Main ADC 24-bit Gain Calibration Coefficient held in these three 8-bit registers.
GN1L/H: Aux ADC 16-bit Gain Calibration Coefficient held in these two 8-bit registers.

ADSTAT - (ADC Status Register):

This SFR reflects the status of both channels including data ready, calibration and various (ADC related) error conditions including reference detect and conversion overflow/underflow errors.

SFR Address	D8H
Power-On Default Value	00H
Bit Addessable	Yes

RDY0	RDY1	CAL	NOXREF	ERR0	ERR1	-	-

Table V. ADSTAT SFR Bit Designations

Bit Location	Bit Mnemonic	Description
ADS.7	RDY0	Ready bit for Main ADC ***Set*** when data is written to Main ADC data registers or on completion of calibration cycle. ***Cleared*** directly by the user or indirectly by a write to the mode bits to start another Main ADC conversion or calibration. The Main ADC is inhibited from writing further results to its data or calibration registers until the RDY0 bit is cleared.
ADS.6	RDY1	Ready bit for Aux ADC Same definition as RDY1 referred to the Aux ADC
ADS.5	CAL	Calibration Status Bit ***Set*** to indicate completion of calibration. ***Cleared*** indirectly by a write to the mode bits to start another ADC conversion or calibration.
ADS.4	NOXREF	No External Reference Bit *(Only active if Main or Aux ADC is active)* ***Set*** to indicate that one or both of the REFIN pins is floating or the applied voltage is below a specified threshold. When Set conversion results are clamped to all ones, if using ext. reference. ***Cleared*** to indicate valid Vref
ADS.3	ERR0	Main ADC Error Bit ***Set*** to indicate that the result written to the Main ADC data registers has been clamped to all zeros or all ones. After a calibration this bit also flags error conditions that caused the calibration registers not to be written. ***Cleared*** by a write to the mode bits to initiate a conversion or calibration.
ADS.2	ERR1	Aux. ADC Error Bit Same definition as RDY1 referred to the Aux ADC
ADS.1	-	Reserved for future use
ADS.0	-	Reserved for future use

ADMODE (ADC Mode Register):
Used to control the operational mode of both channels.

SFR Address	D1H
Power-On Default Value	00H
Bit Addressable	No

-	-	AD0EN	AD1EN	-	MD2	MD1	MD0

Table VI. ADMODE SFR Bit Designations

Bit Location	Bit Mnemonic	Description
ADM.7	-	Reserved for future use
ADM.6	-	Reserved for future use
ADM.5	AD0EN	Main ADC Enable ***Set*** by the user to enable the Main ADC and place it in the mode selected in MD2-MD0 below ***Cleared*** by the user to place the Main ADC in power-down mode.
ADM.4	AD1EN	Aux ADC Enable ***Set*** by the user to enable the Aux ADC and place it in the mode selected in MD2-MD0 below ***Cleared*** by the user to place the Aux ADC in power-down mode.
ADM.3	-	Reserved for future use
ADM.2 ADM.1 ADM.0	MD2 MD1 MD0	Main and Aux ADC Mode bits These bits select the operational mode of the enabled ADC as follows **MD2 MD1 MD0** 0 0 0 Power-down Mode (Power-On Default) 0 0 1 Idle Mode In Idle Mode the ADC filter and modulator are held in a reset state although the modulator clocks are still provided. 0 1 0 Single Conversion Mode In Single Conversion Mode, a single conversion is performed on the enabled channels. On completion of the conversion the ADC data registers (AD0L/H/M and/or AD1L/H) are updated, the relevant flags in the ADSTAT SFR are written and powerdown is re-entered with the MD2-MD0 being written accordingly to 000. 0 1 1 Continuous Conversion In continuous conversion mode the ADC data registers are up dated regularly at the selected update rate (see SF register) 1 0 0 Internal Zero-Scale Calibration Internal short automatically connected to the enabled channel(s) 1 0 1 Internal Full-Scale Calibration Internal or External Vref (as determined by XREF0 and XREF1 bits in AD0/1CON is connected automatically to the ADC input for this calibration. 1 1 0 System Zero-Scale Calibration User should connect system zero-scale input to the channel input pins as selected by CH1/CH0 and ACH1/ACH0 bits in the AD0/1CON register. 1 1 1 System Full-Scale Calibration User should connect system full-scale input to the channel input pins as selected by CH1/CH0 and ACH1/ACH0 bits in the AD0/1CON register.

Special Notes on the use of the ADMODE Register :

1. Any change to the MD bits will immediately reset both ADCs. A write to the MD2-0 bits with no change is also treated as a reset. (See exception to this in note 3 overleaf).

2. If AD0CON is written when AD0EN=1, or if AD0EN is changed from 0 to 1 then both ADC's are also immediately reset. In other words the Main ADC is given priority over the Aux ADC and any change requested on main is immediately responded to.

3. On the other hand if AD1CON is written or if AD1EN is changed from 0 to 1 then only the Aux ADC is reset. For example if the Main ADC is continuously converting when the Aux ADC change or enable occurs. The main ADC continues undisturbed. Rather than allow the Aux ADC operate with a phase difference from the Main ADC, the Aux ADC will fall into step with the outputs of the main ADC. The result is that the first conversion time for the Aux channel will be up to 3 outputs delayed while the Aux ADC update rate is synchronized to the Main ADC.

4. Once AMODE has been written with a calibration mode, the RDY0/1 bits (ADSTAT) are immediately reset and the calibration commences. On completion the appropriate calibration registers are written, the relevant bits in ADSTAT are written and the MD2-0 bits are reset to 000 to indicate the ADC is back in powerdown mode.

5. Any calibration request of the Aux ADC while the temperature sensor is selected will fail to complete.

6. Calibrations are performed with the maximum allowable SF value. SF register is reset to user configuration after calibration.

AD0CON Main ADC Control Registers :
Used to configure the Main ADC for range, channel selection, external Ref enable and unipolar or bipolar coding.

SFR Address	D2H
Power-On Default Value	07H
Bit Addessable	No

-	XREF0	CH1	CH0	UNI0	RN2	RN1	RN0

Table VII. AD0CON SFR Bit Designations

Bit Location	Bit Mnemonic	Description
AD0C.7	-	Reserved for future use
AD0C.6	XREF0	Main ADC External Reference Bit. ***Set*** by user to enable the Main ADC to use the external reference via REFIN(+)/REFIN(-). ***Cleared*** by user to enable the Main ADC to use the internal bandgap reference.
AD0C.5 AD0C.4	CH1 CH0	Main ADC Channel Selection Bits. Written by the user to select the differential input pairs used by the Main ADC as follows : **CH1 CH0 Positive Input Negative Input** 0 0 AIN1 AIN2 0 1 AIN3 AIN4 1 0 AIN2 AIN2 (External Short) 1 1 AIN4 AIN4 (External Short)
AD0C.3	UNI0	Main ADC Unipolar Bit. Set by user to enable unipolar coding i.e. Zero differential input will result in 000000hex output Cleared by user to enable bipolar coding, Zero differential input will result in 800000hex output
AD0C.2 AD0C.1 AD0C.0	RN2 RN1 RN0	Main ADC Range bits Written by the user to select the Main ADC input range as follows **RN2 RN1 RN0 Selected Main ADC Input Range (Vref=2.5V)** 0 0 0 ±20mV 0 0 1 ±40mV 0 1 0 ±80mV 0 1 1 ±160mV 1 0 0 ±320mV 1 0 1 ±640mV 1 1 0 ±1.28V 1 1 1 ±2.56V

AD1CON Aux ADC Control Registers :
Used to configure the Aux ADC for channel selection, external Ref enable and unipolar or bipolar coding. It should be noted that the Aux ADC only operates on a fixed input range of $\pm V_{REF}$.

SFR Address D3H
Power-On Default Value 00H
Bit Addessable No

-	XREF1	ACH1	ACH0	UNI1	-	-	-

Table VIII. AD1CON SFR Bit Designations

Bit Location	Bit Mnemonic	Description
AD1C.7	-	Reserved for future use
AD1C.6	XREF1	Aux ADC External Reference Bit. ***Set*** by user to enable the Aux ADC to use the external reference via REFIN(+)/REFIN(-). ***Cleared*** by user to enable the Aux ADC to use the internal bandgap reference.
AD1C.5 AD1C.4	ACH1 ACH0	Aux ADC Channel Selection Bits. Written by the user to select the single-ended input pins used to drive the Aux ADC as follows :

ACH1	ACH0	Positive Input	Negative Input	
0	0	AIN3	AGND	
0	1	AIN4	AGND	
1	0	Temp Sensor	AGND	(Temp. Sensor routed to the ADC inputs)
1	1	AGND	AGND	(External Short)

Notes : When the temperature sensor is selected, user code must select internal reference via XREF bit above or use an external 1.25V refernce input.
The temperature sensor is factory calibrated to yield conversion results 8000H at 0°C
A +1°C change in temperature will result in a +1LSB change in the AD1H register ADC conversion result.

AD1C.3	UNI1	Aux ADC Unipolar Bit. ***Set*** by user to enable unipolar coding i.e. Zero differential input will result in 0000hex output ***Cleared*** by user to enable bipolar coding, Zero differential input will result in 8000hex output
AD1C.2	-	Reserved for future use
AD1C.1	-	Reserved for future use
AD1C.0	-	Reserved for future use

SF (Sinc Filter Register):
The number in this register is used to set the decimation factor and thus the output update rate for the Main and Aux ADCs. This SFR cannot be written bu user software while either ADC is active. The update rate is used for both Main and Aux ADCs and is calculated as follows :

$$f_{adc} = \frac{1}{3} X \frac{1}{8.SF} X f_{mod}$$

Where : fadc = ADC Output Update Rate
fmod = Modulator Clock Frequency= 32.768KHz (Main and Aux ADC)
SF = Decimal Value written to SF Register

SFR Address D4H
Power-On Default Value 45H
Bit Addessable No

SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0

The allowable range for SF is 13dec to 255dec. Examples of SF values and corresponding conversion rate (f_{adc}) and time (t_{adc}) are shown in table IX below. It should also be noted that both ADC input channels are chopped to minimise offset errors. This means that the time for a single conversion or the time to the first conversion result is 2 X t_{adc}.

SF(dec)	SF(hex)	f_{adc} (Hz)	t_{adc} (ms)
13	0D	105.3	9.52
69	45	19.79	50.34
255	FF	5.35	186.77

Table IX. SF SFR Bit Designations

ICON Current Source Control Registers :

Used to control and configure the various excitation and burnout current source options available on-chip.

SFR Address	D5H
Power-On Default Value	00H
Bit Addessable	No

-	BO	AD1IC	AD0IC	I2PIN	I1PIN	I2EN	I1EN

Table X. ICON SFR Bit Designations

Bit Location	Bit Mnemonic	Description
ADI.7	-	Reserved for future use
ADI.6	BO	Burnout Current Enable Bit. ***Set*** by user to enable both transducer burnout current sources in the main ADC signal paths. ***Cleared*** by user to disable both transducer burnout current sources.
ADI.5	AD1IC	Aux ADC Current Correction Bit ***Set*** by user to allow scaling of the Aux ADC by an internal current source calibration word.
ADI.4	AD0IC	Main ADC Current Correction Bit ***Set*** by user to allow scaling of the Main ADC by an internal current source calibration word.
ADI.3	I2PIN	IEXC2 Current Source Direction Bit ***Set*** by user to enable IEXC2 current source to external pin 11 ***Cleared*** by user to enable IEXC2 current source to external pin 4
ADI.2	I1PIN	IEXC1 Current Source Direction Bit ***Set*** by user to enable IEXC1 current source to external pin 11 ***Cleared*** by user to enable IEXC1 current source to external pin 3
ADI.1	I2EN	IEXC2 Current Source Enable Bit ***Set*** by user to turn on the IEXC2 excitation current source ***Cleared*** by user to turn off the IEXC2 excitation current source
ADI.0	I1EN	IEXC1 Current Source Enable Bit ***Set*** by user to turn on the IEXC1 excitation current source ***Cleared*** by user to turn off the IEXC1 excitation current source

AD0H/AD0M/AD0L Main ADC Data Result Registers :

These three 8-bit registers hold the 24-bit data conversion result from the Main ADC.

SFR Address	AD0H	High Data Byte	DBH
	AD0M	Middle Data Byte	DAH
	AD0L	Low Data Byte	D9H
Power-On Default Value	00H	All three registers	
Bit Addessable	No	All three registers	

AD1H/AD1L Aux ADC Data Result Registers :
These two 8-bit registers hold the 16-bit data conversion result from the Aux ADC.

SFR Address	AD1H	High Data Byte	DDH
	AD1L	Low Data Byte	DCH
Power-On Default Value	00H	Both registers	
Bit Addessable	No	Both registers	

OF0H/OF0M/OF0L Main ADC Offset Calibration Coefficient Registers :
These three 8-bit registers hold the 24-bit data offset calibration coefficient for the Main ADC. These registers are configured at power-on with factory calculated internal zero-scale calibration coefficients. Every device will have different coefficients. However, these bytes will be automatically overwritten if an internal or system zero-scale calibration is initiated by the user via MD2-0 bits in the ADMODE register.

SFR Address	OF0H	Main ADC Offset Coefficient High Byte	E3H
	OF0M	Main ADC Offset Coefficient Middle Byte	E2H
	OF0L	Main ADC Offset Coefficient Low Byte	E1H
Power-On Default Value	-	Configured at factory final test, see notes above	
Bit Addessable	No	All three registers	

OF1H/OF1L Aux ADC Offset Calibration Coefficient Registers :
These two 8-bit registers hold the 16-bit data offset calibration coefficient for the Aux ADC. These registers are configured at power-on with factory calculated internal zero-scale calibration coefficients. Every device will have different coefficients. However, these bytes will be automatically overwritten if an internal or system zero-scale calibration is initiated by the user via the MD2-0 bits in the ADMODE register.

SFR Address	OF1H	Aux ADC Offset Coefficient High Byte	E4H
	OF1L	Aux ADC Offset Coefficient Low Byte	E5H
Power-On Default Value	-	Configured at factory final test, see notes above	
Bit Addessable	No	All three registers	

GN0H/GN0M/GN0L Main ADC Gain Calibration Coefficient Registers :
These three 8-bit registers hold the 24-bit data gain calibration coefficient for the Main ADC. These registers are configured at power-on with factory calculated internal full-scale calibration coefficients. Every device will have different coefficients. However, these bytes will be automatically overwritten if an internal or system full-scale calibration is initiated by the user via MD2-0 bits in the ADMODE register.

SFR Address	GN0H	Main ADC Gain Coefficient High Byte	EBH
	GN0M	Main ADC Gain Coefficient Middle Byte	EAH
	GN0L	Main ADC Gain Coefficient Low Byte	E9H
Power-On Default Value	-	Configured at factory final test, see notes above	
Bit Addessable	No	Both registers	

GN1H/GN1L Aux ADC Gain Calibration Coefficient Registers :
These two 8-bit registers hold the 16-bit data gain calibration coefficient for the Aux ADC. These registers are configured at power-on with factory calculated internal full-scale calibration coefficients. Every device will have different coefficients. However, these bytes will be automatically overwritten if an internal or system full-scale calibration is initiated by the user via MD2-0 bits in the ADMODE register.

SFR Address	GN1H	Aux ADC Gain Coefficient High Byte	EDH
	GN1L	Aux ADC Gain Coefficient Low Byte	ECH
Power-On Default Value	-	Configured at factory final test, see notes above	
Bit Addessable	No	Both registers	

NONVOLATILE FLASH MEMORY

Flash Memory Overview

The ADuC824 incorporates Flash memory technology on-chip to provide the user with a nonvolatile, in-circuit reprogrammable, code and data memory space.

Flash memory is the newest type of nonvolatile memory technology and is based on a single transistor cell architecture.

This technology is basically an outgrowth of EPROM technology and was developed through the late 1980s. Flash memory takes the flexible in-circuit reprogrammable
features of EEPROM and combines them with the space efficient/density features of EPROM (see Figure 7).

Because Flash technology is based on a single transistor cell architecture, a Flash memory array, like EPROM can be implemented to achieve the space efficiencies or memory densities required by a given design.

Like EEPROM, Flash memory can be programmed in-system at a byte level, although it must be erased first; the erase being performed in sector blocks. Thus, Flash memory is often and more correctly referred to as Flash/EE memory.

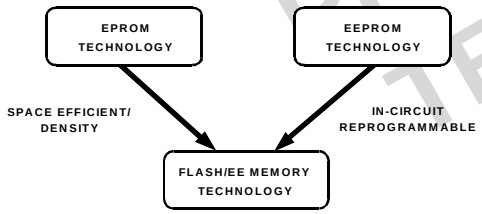


Figure 7. Flash Memory Development

Overall, Flash/EE memory represents a step closer towards the ideal memory device that includes nonvolatility, in-circuit programmability, high density and low cost. Incorporated in the ADuC824, Flash/EE memory technology allows the user to update program code space in-circuit without the need to replace one-time programmable (OTP) devices at remote operating nodes.

Flash/EE Memory and the ADuC824

The ADuC824 provides two arrays of Flash/EE memory for user applications. 8K bytes of Flash/EE Program space are provided on-chip to facilitate code execution without any external discrete ROM device requirements. The program memory can be programmed using conventional third party memory programmers. This array can also be programmed in-circuit, using the serial download mode provided.

A 640-Byte Flash/EE Data Memory space is also provided on-chip. This may be used by the user as a general purpose non-volatile scratchpad area. User access to this area is via a group of six SFRs. This space can be programmed at a byte level, although it must first be erased in 4-byte sectors.

Using the Flash/EE Program Memory

This 8K Byte Flash/EE Program Memory array is mapped into the lower 8K bytes of the 64K bytes program space addressable by the ADuC824 and will be used to hold user code in typical applications.

The program memory array can be programmed in one of two modes, namely:

Serial Downloading (In-Circuit Programming)
As part of its factory boot code, the ADuC824 facilitates serial code download via the standard UART serial port. Serial download mode is automatically entered on power-up if the external pin, PSEN, is pulled low through an external resistor as shown in Figure 8. Once in this mode, the user can download code to the program memory array while the device is sited in its target application hardware. A PC serial download executable is provided as part of the ADuC824 QuickStart development system. The Serial Download protocol is detailed in a MicroConverter Applications Note uC004 available from the ADI MicroConverter Website at www.analog.com/microconverter.

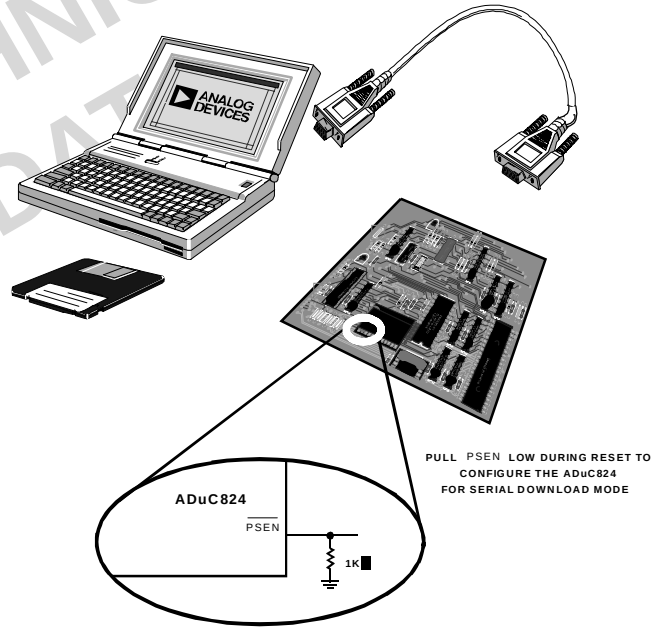


Figure 8. Flash/EE Memory Serial Download Mode Programming

Parallel Programming

The parallel programming mode is fully compatible with conventional third party Flash or EEPROM device programmers. A block diagram of the external pin configuration required to support parallel programming is shown in Figure 9. In this mode Ports P0, P1 and P2 operate as the external data and address bus interface, ALE operates as the Write Enable strobe and Port P3 is used as a general configuration port that configures the device for various program and erase operations during parallel programming.

The high voltage (12 V) supply required for Flash/EE programming is generated using on-chip charge pumps to supply the high voltage program lines.

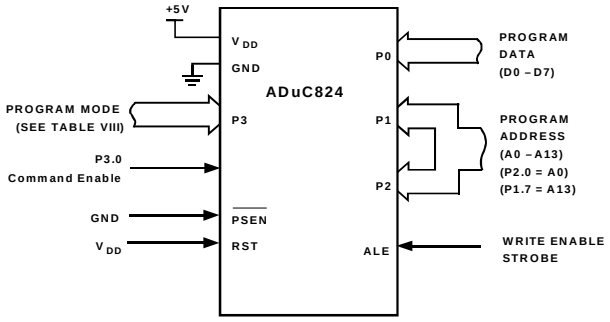


Figure 9. Flash/EE Memory Parallel Programming

Table VIII shows the normal parallel programming modes that can be configured using Port 3 bits.

Table XI. Flash/EE Data Memory Parallel Programming Modes.

Port Pins .7	.6	.5	.4	P3.1 to P3.7 .3	.2	.1	Programming Mode
X	X	X	X	0	0	0	Erase Flash/EE Program and Data
X	X	X	X	0	0	1	Read Signature
X	X	X	0	0	1	0	Program Code Byte
X	X	X	1	0	1	0	Program Data Byte
X	X	X	0	0	1	1	Read Code Byte
X	X	X	0	0	1	1	Read Data Byte
X	X	X	X	1	0	0	Reserved
X	X	X	X	1	0	1	Reserved
All other codes							Redundant

Using the Flash/EE Data Memory

The user Flash/EE data memory array consists of 640 bytes that are configured into 160 (00H to 9FH), 4-byte pages as Figure 10.

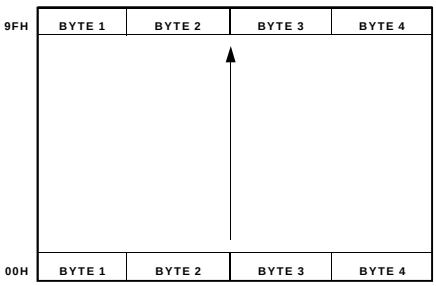


Figure 10. Flash/EE Data Memory Configuration

As with other ADuC824 user peripheral circuits the interface to this memory space is via a group of registers mapped in the SFR space. A group of four data registers (EDATA1-4) are used to hold the 4-byte page data just accessed. EADRL is used to hold the 8-bit address of the page to be accessed. Finally, ECON is an 8-bit control register that may be written with one of five Flash/EE memory access commands to enable various read, write, erase and verify modes. These registers can be summarized as follows :

ECON : SFR Address: B9H
Function: Controls access to 640 Bytes Flash/EE Data Space.
Default: 00H

EADRL : SFR Address: C6H
Function: Holds the Flash/EE Data Page Address. (640 Bytes => 160 Page Addresses.)
Default: 00H

EDATA 1 - 4 :
SFR Address: BCH to BFH respectively
Function : Holds Flash/EE Data memory page write or page read data bytes.
Default : EDATA1-2 -> 00H
EDATA3-4 -> FFH

A block diagram of the SFR registered interface to the Flash/EE Data Memory array is shown in Figure 11.

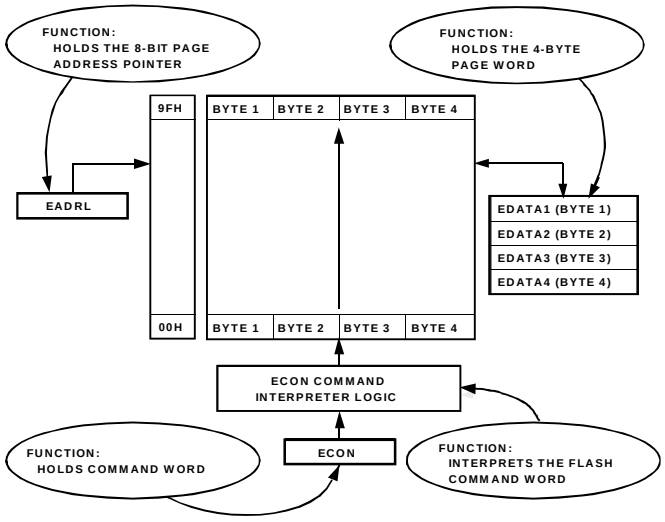


Figure 11. Flash/EE Data Memory Control and Configuration

ECON—Flash/EE Memory Control SFR
This SFR acts as a command interpreter and may be written with one of five command modes to enable various read, program and erase cycles as detailed in Table XII:

Table XII. ECON–Flash/EE Memory Control Register Command Modes

Command Byte	Command Mode
01H	READ COMMAND
	Results in four bytes being read into EDATA 1–4 from memory page location contained in EADRL .
02H	WRITE COMMAND Results in four bytes (EDATA 1–4) being written to memory page location in EADRL.This write command assumes the designated "write" page has been pre-erased.
03H	ERASE-WRITE COMMAND Results in four bytes (EDATA 1–4) being written to memory page location in EADRL. These 4 bytes locations are pre-erased before the write sequence as part of this cycle.
04H	VERIFY COMMAND Allows the user to verify if data in EDATA1–4 is contained in page location designated by EADRL. A subsequent read of the ECON SFR will result in a "zero" being read if the verification is valid, a nonzero value will be read to indicate an invalid verification.
05H	ERASE COMMAND Results in an erase of the 4-byte page designated in EADRL.
06H	ERASE-ALL COMMAND Results in erase of the full Flash/EE Data memory 160-page (640 bytes) array.
07H to FFH	RESERVED COMMANDS Commands reserved for future use.

Flash/EE Memory Write and Erase Times
The typical program/erase times for the User Flash/EE Memory are:
Erase Full Array (640 Bytes) – 20 ms
Erase Single Page (4 Bytes) – 20 ms
Program Page (4 Bytes) – 250 µs
Read Page (4 Bytes) – Within Single Instruction Cycle

Using the Flash/EE Memory Interface
As with all Flash/EE memory architectures, the array can be programmed in system at a byte level, although it must be erased first; the erasure being performed in page blocks (4-byte pages in this case).

A typical access to the Flash/EE array will involve setting up the page address to be accessed in the EADRL SFR, configuring the EDATA1-4 with data to be programmed to the array (the EDATA SFRs will not be written for read accesses) and finally writing the ECON command word which initiates one of the six modes shown in Table XII.

It should be noted that a given mode of operation is initiated as soon as the command word is written to the ECON SFR. At this time the core microcontroller operation on the ADuC824 is idled until the requested Program/Read or Erase mode is completed.
In practice, this means that even though the Flash/EE memory mode of operation is typically initiated with a 2 machine cycle MOV instruction (to write to the ECON SFR), the next instruction will not be executed until the Flash/EE operation is complete (250 µs or 20 ms later). This means that the core will not respond to Interrupt requests until the Flash/EE operation is complete, although the core peripheral functions like Counter/Timers will continue to count and time as configured throughout this pseudo-idle period.

ERASE-ALL
Although the 640-byte User Flash/EE array is shipped from the factory pre-erased, i.e., Byte locations set to FFH, it is nonetheless good programming practice to include an erase-all routine as part of any configuration/ setup code running on the ADuC824. An "ERASE-ALL" command consists of writing "06H" to the ECON SFR, which initiates an erase of all 640 byte locations in the Flash/EE array. This command coded in 8051 assembly would appear as:

```
MOV ECON, #06H          ; Erase all Command
                        ; 20 ms Duration
```

PROGRAM A BYTE
In general terms, a byte in the Flash/EE array can only be programmed if it has previously been erased. To be more specific, a byte can only be programmed if it already holds the value FFH. Because of the Flash/EE architecture this erasure must happen at a page level, therefore a minimum of four bytes (1 page) will be erased when an erase command is initiated.

A more specific example of the Program-Byte process is shown below. In this example the user will writes F3H into the second byte on Page 03H of the Flash/EE Data Memory space while preserving the other 3 bytes already in this page. As the user is only required to modify one of the page bytes, the full page must be first read so that this page can then be erased without the existing data being lost.

This example coded in 8051 assembly would appear as :

```
MOV  EADRL,#03H    ; Set Page Address Pointer
MOV  ECON,#01H     ; Read Page
MOV  EDATA2,#0F3H  ;Write New Byte
MOV  ECON,#03H     ; Erase-Write Page
```

USER INTERFACE TO OTHER ON-CHIP ADUC824 PERIPHERALS :

The following section gives a brief overview of the various secondary peripherals also available on-chip. A summary of the SFRs used to control and configure these peripherals is also given.

DAC :

The ADuC824 incorporates a 12-bit, voltage output DAC on-chip. It has a rail-to-rail voltage output buffer capable of driving 10kΩ/100pF. It has two selectable ranges, 0V to V_{REF} (the internal bandgap 2.5V reference) and 0V to AV_{DD}. It can operate in 12-bit or 8-bit mode. The DAC has a control register DACCON, and two data registers DACL/H. The DAC output can be programmed to appear at pin 10 or pin 12.

DACCON : DAC Control Register:

SFR Address	FDH
Power-On Default Value	00H
Bit Addessable	No

-	-	-	DACPIN	DAC8	DACRN	$\overline{DACCLR}$	$\overline{DACPD}$

Table XIII. DACCON SFR Bit Designations

Bit Location	Bit Mnemonic	Description
DACC.7	-	Reserved for future use
DACC.6	-	Reserved for future use
DACC.5	-	Reserved for future use
DACC.4	DACPIN	DAC Output Pin Select ***Set*** by the user to direct the DAC output to pin 12 (AIN4), (assuming the DACPD bit is high). ***Cleared*** by user to direct the DAC output to pin 10 (AIN2).
DACC.3	DAC8	DAC 8-bit Mode Bit ***Set*** by user to enable 8-bit DAC operation. In this mode the 8-bits in DACL SFR are routed to the 8 MSBs of the DAC and the 4 LSBs of the DAC are set to zero. ***Cleared*** by user to operate the DAC in its normal 12-bit mode of operation.
DACC.2	DACRN	DAC Output Range Bit ***Set*** by user to configure DAC range of 0 - AV_{DD} ***Cleared*** by user to configure DAC range of 0 - 2.5V
DACC.1	$\overline{DACCLR}$	DAC Clear Bit ***Set*** to '1' by user to enable normal DAC operation ***Cleared*** to '0' by user to reset DAC data registers DACl/H to 'zero'
DACC.0	$\overline{DACPD}$	DAC Powerdown Bit ***Set*** to '1' by user to enable normal DAC operation ***Cleared*** to '0' by user to powerdown the DAC.

DACL/H : DAC Data Registers:

Function: Dac Data Registers, written by user to update the DAC output.

SFR Address	DACL (DAC Data Low Byte)	->FBH
	DACH (DAC Data Low Byte)	->FCH
Power-On Default Value	00H	->Both Registers
Bit Addessable	No	->Both Registers

ON-CHIP PLL :
The ADuC824 is intended for use with a 32.768kHz watch crystal. A PLL locks onto a multiple (32 times 12) of this to provide a stable 12.582912MHz clock for the system. The core can operate at this frequency or at binary sub-multiples of it to allow power saving in cases where maximum core performance is not required. The default core clock is the PLL clock divided-by-8 or 1.572864MHz. The ADC clocks are also derived from the PLL clock, with the modulator rate being the same as the crystal oscillator frequency. The above choice of frequencies ensures that the modulators and the core will be in synchronism, regardless of the core clock rate. The PLL control register is PLLCON.

PLLCON: PLL Control Register:

SFR Address	D7H
Power-On Default Value	03H
Bit Addessable	No

OSC_PD	LOCK	-	-	FINT	CD2	CD1	CD0

Table XIV. PLLCON SFR Bit Designations

Bit Location	Bit Mnemonic	Description
PLL.7	OSC_PD	Oscillator Powerdown Bit ***Set*** by user to halt the 32kHz oscillator in powerdown mode. ***Cleared*** by user to enable the 32kHz oscillator in powerdown mode. This feature allows the TIC to continue counting even in powerdown mode.
PLL.6	LOCK	PLL Lock Interrupt Bit This is a read only bit. ***Set*** to indicate the PLL loop is correctly tracking the crystal clock. ***Cleared*** to indicate the PLL is not correctly tracking the crystal clock. This may be due to the absence of a crystal clock or an external cyrstal that is initially present but becomes disconnected or damaged on the board. In both these cases the PLL loop is placed in an open loop condition with the VCO oscillating at it's nominal frequency and providing system clocks. If LOCK goes low it will generate an interrupt if enabled via the interrupt register (IEIP2)
PLL.5	-	Reserved for future use.
PLL.4	-	Reserved for future use.
PLL.3	FINT	Fast Interrupt Response Bit ***Set*** by user enabling the response to any interrupt to be executed at the fastest core clock frequency, regardless of the configuration of the CD2-0 buts (see below). Once user code has returned from an interrupt the core resumes code execution at the core clock selected by the CD2-0 bits. ***Cleared*** by user to disable the fast interrupt response feature.
PLL.2 PLL.1 PLL.0	CD2 CD1 CD0	CPU (Core Clock) Divider Bits This number determines the frequency at which the microcontroller core will operate.

CD2	CD1	CD0	Core Clock Frequency (MHz)
0	0	0	12.582912
0	0	1	6.291456
0	1	0	3.145728
0	1	1	1.572864 (Default Core Clock Frequency)
1	0	0	0.786432
1	0	1	0.393216
1	1	0	0.196608
1	1	1	0.098304

TIMER INTERVAL COUNTER (TIC) :
A timer interval counter is provided on-chip for counting longer intervals than the standard 8051 compatible timers are capable of. Furthermore this counter is clocked by the crystal oscillator rather than the PLL and thus has the ability to remain active in power-down and time long power-down intervals. This has obvious application for remote battery powered sensors where regular widely-spaced readings are required. There are six SFR's associated with the time interval counter, TIMECON being it's control register. Essentially, the TIC will generate an active output when selected timebase counter reaches the value written by user code to the INTVAL SFR. The active output can trigger an interrupt or set a bit in the TIMECON SFR. The timebase SFRs described overleaf can be written initially with the current time, the active *clock* can then be read at any time later by user software.

TIMECON: TIC Control Register:

SFR Address	A1H
Power-On Default Value	00H
Bit Addessable	No

-	TFH	ITS1	ITS0	STI	TII	TIEN	TCEN

Table XV. TIMECON SFR Bit Designations

Bit Location	Bit Mnemonic	Description
TIME.7	-	Reserved for future use.
TIME.6	TFH	Twenty four hour select bit ***Set*** by user to enable 24 hour count in the HOUR SFR ***Cleared*** by user to allow the HOUR counter to count 0-255 hours.
TIME.5 TIME.4	ITS1 ITS0	Interval Timebase Selection Bits Written by user to determine the interval counter update rate. ITS1 ITS0 Interval Timebase 0 0 1/128 second 0 1 1 second 1 0 1 minute 1 1 1 hour
TIME.3	STI	Single Time Interval Bit ***Set*** by user to generate a single interval timeout. ***Cleared*** by user to allow the interval counter to be automatically reloaded and start counting again at each interval timeout.
TIME.2	TII	TIC Interrupt Bit This is a read only bit, normally '0' ***Set*** when the Time Interval Counter matches the value in the INTVAL SFR.
TIME.1	TIEN	Time Interval Enable Bit ***Set*** by user to enable the 8-bit time interval counter. Cleared by user to disable and clear the contents of the interval counter
TIME.0	TCEN	Time Clock Enable Bit ***Set*** by user to enable the time clock to the time interval counters ***Cleared*** by user to disable the clock to the time interval counters

INTVAL : User Interval Count Select Register

Function: User code writes the required time interval to this register. The TIC times out when the count in the selected time interval registers equals the value written to this register.

SFR Address	A6H
Power-On Default Value	00H
Bit Addessable	No
Valid Value	0 to 255 decimal

HTHSEC: **Hundreths Seconds Time Register**

Function: This register is incremented in (1/128) second intervals once TCEN in TIMECON is active. The register counts from 0 to 127 before rolling over to increment the SEC time register.

SFR Address	A2H
Power-On Default Value	00H
Bit Addessable	No
Valid Value	0 to 127 decimal

SEC: **Seconds Time Register**

Function: This register is incremented in 1 second intervals once TCEN in TIMECON is active. The register counts from 0 to 59 before rolling over to increment the MIN time register.

SFR Address	A3H
Power-On Default Value	00H
Bit Addessable	No
Valid Value	0 to 59 decimal

MIN: **Minutes Time Register**

Function: This register is incremented in 1 minute intervals once TCEN in TIMECON is active. The register counts from 0 to 59 before rolling over to increment the HOUR time register.

SFR Address	A4H
Power-On Default Value	00H
Bit Addessable	No
Valid Value	0 to 59 decimal

HOUR: **Hours Time Register**

Function: This register is incremented in 1 hour intervals once TCEN in TIMECON is active. If TFH in TIMECON is set this register counts from 0 to 24 otherwise the hours time register will count from 0 to 255.

SFR Address	A5H
Power-On Default Value	00H
Bit Addessable	No
Valid Value	0 to 23 decimal - TFH = 1 0 to 255 decimal - TFH = 0

WATCHDOG TIMER

The purpose of the watchdog timer is to generate a device reset or interrupt within a reasonable amount of time if the ADuC824 enters an erroneous state, possibly due to a programming error, electrical noise or RFI. The Watchdog function can be permanently disabled by clearing WDE (Watchdog Enable) bit in the Watchdog Control (WDCON) SFR. When enabled the watchdog circuit will generate a system reset or interrupt (WDIR Bit) if the user program fails to clear the watchdog (WDE bit) within a predetermined amount of time.

The watchdog timer itself is a 16-bit counter, which is clocked directly by the PLL clock (f_{pll} = 32.768kHz). The watchdog timeout interval can be adjusted via the PRE3-0 bits in WDCON. Full Control and Status of the watchdog timer function may be controlled via the watchdog timer control SFR (WDCON).

WDCON: Watchdog Timer Control Register:

SFR Address	C0H
Power-On Default Value	10H
Bit Addessable	Yes

PRE3	PRE2	PRE1	PRE0	WDIR	WDS	WDE	WDWR

Table XVI. WDCON SFR Bit Designations

Bit Location	Bit Mnemonic	Description
WDC.7 WDC.6 WDC.5 WDC.4	PRE3 PRE2 PRE1 PRE0	Watchdog Timer Prescale Bits. The Watchdog timeout period is given by the equation : $t_{WD} = (2^{PRE} \times (2^9 / f_{pll}))$ (PRE>0; fpll=32.768kHz)

PRE3	PRE2	PRE1	PRE0	Timout Period (ms)	Action
0	0	0	0	15.6	Reset or Interrupt
0	0	0	1	31.2	Reset or Interrupt
0	0	1	0	62.5	Reset or Interrupt
0	0	1	1	125	Reset or Interrupt
0	1	0	0	250	Reset or Interrupt
0	1	0	1	500	Reset or Interrupt
0	1	1	0	1000	Reset or Interrupt
0	1	1	1	2000	Reset or Interrupt
1	0	0	0	0.0	Immediate Reset
1	0	0	1	-	Reserved
PRE3-0 > 1001				-	Redundant

WDC.3	WDIR	Watchdog Interrupt Response Enable Bit If this bit is set by the user the watchdog will generate a interrupt response instead of a system reset when the watchdog timeout period has expired. This interrupt is not disabled by the CLR EA instruction and it is also a fixed high priority interrupt. If the watchdog is not being used to monitor the system it can be alternatively be used as a timer, the prescaler is used to set the timeout period in which a interrupt will be generated.
WDC.2	WDS	Watchdog Status Bit ***Set*** by the Watchdog Controller to indicate that a watchdog timeout has occurred. ***Cleared*** by writing a '0' or by an external hardware reset. It is not cleared by a watchdog reset.
WDC.1	WDE	Watchdog Enable Bit ***Set*** by user to enable the watchdog and clear its counters. If this bit is not set by the user within the watchdog timeout period, then the watchdog will generate a reset or interrupt depending on WDIR. Cleared under the following conditions, User writes '0', Watchdog Reset (WDIR='0'); Hardware Reset; PSM Interrupt; LOCK Interrupt.
WDC.0	WDWR	Watchdog Write Enable Bit To write data into the WDCON SFR involves a double instruction sequence. The WDWR bit must be set and the following instruction must be a write instruction to the WDCON SFR.

POWER SUPPLY MONITOR

The Power Supply Monitor generates an interrupt when either power supply (AV_{DD} or DV_{DD}) to the ADuC824 drops below one of four user selectable voltage trip points from 2.63V to 4.63V. The interrupt bit will not be cleared until the power supply has returned above the trip point for at least 256mS. This monitor function ensures the user can save working registers so as to avoid possible data corruption due to the low supply condition and that code execution will not resume until a 'safe' supply level has been well established. The supply monitor is also protected against spurious glitches triggering the interrupt circuit.

The Power Supply Monitor function is controlled via the PSMCON SFR.

PSMCON: Power Supply Monitor Control Register:

SFR Address	DFH
Power-On Default Value	DEH
Bit Addessable	No

CMPD	CMPA	PSMI	TPD1	TPD0	TPA1	TPA0	$\overline{PSMPD}$

Table XVII. PSMCON SFR Bit Designations

Bit Location	Bit Mnemonic	Description
PSM.7	CMPD	DV_{DD} Comparator Bit This is a read only bit and directly reflects the state of the DV_{DD} comparator. Read '1' indicates the DV_{DD} supply is above its selected trip point Read '0' indicates the DV_{DD} supply is below its selected trip point
PSM.6	CMPA	AV_{DD} Comparator Bit This is a read only bit and directly reflects the state of the AV_{DD} comparator. Read '1' indicates the AV_{DD} supply is above its selected trip point Read '0' indicates the AV_{DD} supply is below its selected trip point
PSM.5	PSMI	Power Supply Monitor Interrupt Bit This bit will be set high by the MicroConverter if either CMPA or CMPD are low, indicating low analog or digital supply. The PSMI bit can be used to interrupt the processor. Once CMPD and/or CMPA return (and remain) high, a 250ms counter is started. When this counter times out the PSMI interrupt is cleared. PSMI can also be written by the user. However if either comparator output is low then it is not possible for the user to clear PSMI.
PSM.4 PSM.3	TPD1 TPD0	DV_{DD} Trip Point Selection Bits These bits select the DV_{DD} trip-point voltage as follows : TPD1 TPD0 Selected DV_{DD} Trip-Point (V) 0 0 4.63 0 1 3.08 1 0 2.93 1 1 2.63
PSM.2 PSM.1	TPA1 TPA0	AV_{DD} Trip Point Selection Bits These bits select the AV_{DD} trip-point voltage as follows : TPD1 TPD0 Selected AV_{DD} Trip-Point (V) 0 0 4.63 0 1 3.08 1 0 2.93 1 1 2.63
PSM.0	$\overline{PSMPD}$	Power Supply Monitor Power-Down Bit ***Set*** to '1' by the user to power up the Power Supply Monitor Circuit ***Cleared*** to '0' by the user to power down the Power Supply Monitor Circuit

SERIAL PERIPHERAL INTERFACE

The ADuC824 integrates a complete hardware Serial Peripheral Interface (SPI) interface on-chip. SPI is an industry standard synchronous serial interface which allows eight bits of data to be synchronously transmitted and received simultaneously. It should be noted that the SPI physical interface is shared with the I2C interface and therefore the user can only enable one or other interface at any given time (see SPE in SPICON below). The system can be configured for Master or Slave operation and typically consists of four pins, namely :

MISO (Pin#14) :Master In, Slave Out Data I/O Pin
MOSI (Pin#27) :Master Out, Slave In Pin
SCLOCK (Pin#26) :Serial Clock I/O Pin
$\overline{SS}$ (Pin#13) :Slave Select I/O Pin

The following SFR registers are used in control of the SPI interface.

SPICON: **SPI Control Register:**
SFR Address F8H
Power-On Default Value 04H
Bit Addessable Yes

ISPI	WCOL	SPE	SPIM	CPOL	CPHA	SPR1	SPR0

Table XVIII. SPICON SFR Bit Designations

Bit Location	Bit Mnemonic	Description
SPIC.7	ISPI	SPI Interrupt Bit ***Set*** by MicroConverter at the end of each SPI transfer. ***Cleared*** directly by user code or indirectly by reading the SPIDAT SFR
SPIC.6	WCOL	Write Collision Error Bit ***Set*** by MicroConverter if SPIDAT is written to while an SPI transfer is in progress.
SPIC.5	SPE	SPI Interface Enable Bit ***Set*** by user to enable the SPI interface. ***Cleared*** by user to enable the I2C interface.
SPIC.4	SPIM	SPI Master/Slave Mode Select Bit ***Set*** by user to enable Master Mode operation (SCLOCK is an output). ***Cleared*** by user to enable Slave Mode operation (SCLOCK is an input).
SPIC.3	CPOL	Clock Polarity Select Bit ***Set*** by user to idle SCLOCK high. ***Cleared*** by user to idle SCLOCK low.
SPIC.2	CPHA	Clock Phase Select Bit ***Set*** by user to enable leading SCLOCK edge to transmit data ***Cleared*** by user to enable trailing SCLOCK edge to transmit data
SPIC.1 SPIC.0	SPR1 SPR0	SPI Bit-Rate Select Bits These bits select the SCLOCK rate (bit-rate) in Master Mode as follows : SPIC.1 SPIC.0 Selected Bit Rate 0 0 f_{core} / 2 0 0 f_{core} / 4 0 0 f_{core} / 8 0 0 f_{core} / 16

SPIDAT: **SPI Data Register**
Function: The SIDAT SFR is written by the user to transmit data over the SPI interface or read by user code to read data just received by the SPI interface

SFR Address F7H
Power-On Default Value 00H
Bit Addessable No

I2C COMPATIBLE INTERFACE

The ADuC824 supports a 2 wire serial interface mode which is I2C compatible. The I2C compatible interface shares its pins with the on-chip SPI interface and therefore the user can only enable one or other interface at any given time (see SPE in SPICON previously). An Application Note describing the operation of this interface as implemented on the ADuC824 is available from the MicroConverter Web-Site at **'www.analog.com/microconverter'**. This interface can be configured to be a Software Master or Hardware Slave and uses two pins in the interface :

SDATA (Pin#27)	Serial data I/O Pin
SCLOCK (Pin#26)	Serial Clock

Three SFR's are used to control this interface, these are described below:
The following SFR registers are used in control of the SPI interface.

I2CCON:	**I2C Control Register:**
SFR Address	E8H
Power-On Default Value	00H
Bit Addessable	Yes

MDO	MDE	MCO	MDI	I2CM	I2CRS	I2CTX	I2CI

Table XIV. I2CCON SFR Bit Designations

Bit Location	Bit Mnemonic	Description
I2CC.7	MDO	I2C Software Master Data Output Bit This data bit is used to implement a master I2C transmitter interface in software. Data written to this bit will be outputted on the SDATA pin if the data output enable (MDE) bit is set
I2CC.6	MDE	I2C Software Master Data Output Enable Bit ***Set*** by user to enable the SDATA pin as an output (TX) ***Cleared*** by the user to enable SDATA pin as an input (RX)
I2CC.5	MCO	I2C Software Master Clock Output Bit This data bit is used to implement a master I2C transmitter interface in software. Data written to this bit will be outputted on the SCLOCK pin
I2CC.4	MDI	I2C Software Master Data Input Bit This data bit is used to implement a master I2C receiver interface in software. Data on the SDATA pin is latched in this bit on SCLOCK if the Data Output Enable (MDE) bit is '0'
I2CC.3	I2CM	I2C Master/Slave Mode Bit ***Set*** by user to enable I2C software master mode ***Cleared*** by user to enable I2C hardware slave mode
I2CC.2	I2CRS	I2C Reset Bit ***Set*** by user to reset the I2C interface.
I2CC.1	I2CTX	I2C Direction Transfer Bit ***Set*** by the MicroConverter if the interface is transmitting ***Cleared*** by the MicroConverter if the interface is receiving
I2CC.0	I2CI	I2C Interrupt Bit ***Set*** by the MicroConverter after a byte has been transmitted or received ***Cleared*** by user code writing '0' to this bit

I2CADD: I2C Address Register

Function: Holds the I2C peripheral address for the part. It may be overwritten by user code.

SFR Address	9BH
Power-On Default Value	55H
Bit Addessable	No

I2CDAT: I2C Data Register

Function: The I2CDAT SFR is written by the user to transmit data over the I2C interface or read by user code to read data just received by the I2C interface

SFR Address	9AH
Power-On Default Value	00H
Bit Addessable	No

8051 Compatible On-Chip Peripherals :
This Section gives a brief overview of the various secondary peripheral circuits which are also available to the user on-chip. These remaining functions are fully 8051- compatible and are controlled via standard 8051 SFR bit definitions. A brief overview of these registers and bit definitions is given in Figures 12 and 13 below.

Parallel I/O Ports 0 - 3
The ADuC824 uses four input/output ports to exchange data with external devices. In addition to performing general purpose I/O, some ports are capable of external memory operations; others are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Ports 0,2 and 3 are bidirectional while only P1.0 and P1.1 pins on Port 1 are bidirectional. All ports contain an output latch and input buffer, the I/O Ports will also contain an output driver. Unlike Port 2 and 3 (which have internal pull-up resistors), Port 0 pins are open drain in digital I/O mode and will require external pull-up resistors. Read and Write accesses to Port 0-3 pins are performed via their corresponding special function registers. Each Port I/O line may be independently configured as an input or output via the corresponding individual Port SFR bits in one of four Port SFR's (PO - P3).

The remaining Port 1 pins (P1.2 - P1.7) can only be configured as Analog or Digital Input pins. By (power-on) default these pins are configured as Analog Inputs i.e. '1' written in the corresponding Port 1 register bit. To configure any of these pins as digital inputs the user should write a '0' to these port bits to configure the corresponding pin as a digital input.

UART Serial Interface
The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. However if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost.

The physical interface to the serial data network is via Pins RXD(P3.0) and TXD(P3.1) while the SFR interface to the UART comprises of the following registers.

SBUF The serial port receive and transmit registers are both accessed through Special Function Register SBUF. Writing to SBUF loads the transmit register and reading SBUF accesses a physically separate receive register.

SCON This SFR controls UART serial data communication.

Timers/Counters
The ADuC824 has three 16-bit Timer/Counters, namely : Timer 0, Timer 1 and Timer 2. The Timer/Counter hardware has been included on-chip to relieve the processor core of the overhead inherent in implementing timer/counter functionality in software. Each Timer/Counter consists of two 8-bit registers THx and TLx (x = 0, 1 and 2). All three can be configured to operate either as timers or event counters.

In 'Timer' function, the TLx register is incremented every machine cycle. Thus one can think of it as counting machine cycles. Since a machine cycle consists of 12 oscillator periods, the maximum count rate is 1/12 of the oscillator frequency.

In 'Counter' function, the TLx register is incremented by a 1 to 0 transition at its corresponding external input pin, T0, T1 or T2. In this function the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes two machine cycles (24 oscillator periods) to recognize a 1 to 0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal but to ensure that a given level is sampled at least once before it changes, it must be held for at least on full machine cycle.

User configuration and control of all Timer operating modes is achieved via three SFR's, namely :

TMOD, TCON Control and configuration for Timers 0 and 1.
T2CON: Control and configuration for Timer 2.

SBUF	SERIAL PORT BUFFER REGISTER
PCON	POWER CONTROL REGISTER
PCON.7	DOUBLE BAUD RATE CONTROL
PCON.6	ENABLE SPI / I2C POWERDOWN INTERRUPT
PCON.5	ENABLE INT0 POWERDOWN INTERRUPT
PCON.4	ALE DISABLE (0 = NORMAL, 1 = FORCES ALE HIGH)
PCON.3	GENERAL PURPOSE FLAG
PCON.2	GENERAL PURPOSE FLAG
PCON.1	POWER-DOWN CONTROL BIT (RECOVERABLE WITH INTERRUPTS OR HARD RESET)
PCON.0	IDLE-MODE CONTROL (RECOVERABLE WITH ENABLED INTERRUPT)
PSW	PROGRAM STATUS WORD
CY	CARRY FLAG
AC	AUXILIARY CARRY FLAG
F0	GENERAL PURPOSE FLAG 0
RS1	REGISTER BANK SELECT CONTROL BITS
RS0	ACTIVE REGISTER BANK = [0, 1, 2, 3]
OV	OVERFLOW FLAG
F1	GENERAL PURPOSE FLAG 1
P	PARITY OF ACC
DPP	DATA POINTER PAGE
DPH, DPL (DPTR)	DATA POINTER
ACC	ACCUMULATOR
B	
SP	STACK POINTER

Figure 12. ADuC824 Core Registers

TCON	TIMER CONTROL REGISTER
TF1	TIMER1 OVERFLOW FLAG (AUTO CLEARED ON VECTOR TO ISR)
TR1	TIMER1 RUN CONTROL (0 = OFF, 1 = RUN)
TF0	TIMER0 OVERFLOW FLAG (AUTO CLEARED ON VECTOR TO ISR)
TR0	TIMER0 RUN CONTROL (0 = OFF, 1 = RUN)
IE1	EXTERNAL INT1 FLAG (AUTO CLEARED ON VECTOR TO ISR)
IT1	IE1 TYPE (0 = LEVEL TRIG, 1 = EDGE TRIG)
IE0	EXTERNAL INT0 FLAG (AUTO CLEARED ON VECTOR TO ISR)
IT0	IE0 TYPE (0 = LEVEL TRIG, 1 = EDGE TRIG)
TH0, TL0	TIMER0 REGISTERS
TH1, TL1	TIMER1 REGISTERS
T2CON	TIMER2 CONTROL REGISTER
TF2	OVERFLOW FLAG
EXF2	EXTERNAL FLAG
RCLK	RECEIVE CLOCK ENABLE (0 = TIMER1 USED FOR RxD CLK)
TCLK	TRANSMIT CLOCK ENABLE (0 = TIMER1 USED FOR TxD CLK)
EXEN2	EXTERNAL ENABLE (0 = IGNORE T2EX, 1 = CAP/RL)
TR2	RUN CONTROL (0 = STOP, 1 = RUN)
CNT2	TIMER/COUNTER SELECT (0 = TIMER, 1 = COUNTER)
CAP2	CAPTURE/RELOAD SELECT (0 = RELOAD, 1 = CAPTURE)
TH2, TL2	TIMER2 REGISTER
RCAP2H, RCAP2L	TIMER2 CAPTURE/RELOAD

P0	PORT0 REGISTER (ALSO A 0–A7 & D0 – D7)
P1	PORT1 REGISTER (ANALOG & DIGITAL INPUTS)
T2EX	TIMER/ COUNTER 2 CAPTURE/ RELOAD TRIGGER
T2	TIMER/ COUNTER 2 EXTERNAL INPUT
P2	PORT2 REGISTER (ALSO A 8–A15 & A16 – A23)
P3	PORT3 REGISTER
RD	EXTERNAL DATA MEMORY READ STROBE
WR	EXTERNAL DATA MEMORY WRITE STROBE
T1	TIMER/ COUNTER 1 EXTERNAL INPUT
T0	TIMER/ COUNTER 0 EXTERNAL INPUT
INT1	EXTERNAL INTERRUPT 1
INT0	EXTERNAL INTERRUPT 0
TxD	SERIAL PORT TRANSMIT DATA LINE
RxD	SERIAL PORT RECEIVE DATA LINE
SCON	SERIAL COMMUNICATIONS CONTROL REGISTER
SM0	UART MODE CONTROL BITS — BAUD RATE:
SM1	00 - 8 BIT SHIFT REGISTER — $F_{CORE}/12$
	01 - 8 BIT UART — TIMER OVERFLOW RATE/32 (X 2)
	10 - 9 BIT UART — $F_{CORE}/64$ (X 2)
	11 - 9 BIT UART — TIMER OVERFLOW RATE/32 (X 2)
SM2	IN MODES 2&3, ENABLES MULTIPROCESSOR COMMUNICATION
REN	RECEIVE ENABLE CONTROL BIT
TB8	IN MODES 2&3, 9TH BIT TRANSMITTED
RB8	IN MODES 2&3, 9TH BIT RECEIVED
TI	TRANSMIT INTERRUPT FLAG
RI	RECEIVE INTERRUPT FLAG

Figure 13. ADuC824 Core Registers

INTERRUPT SYSTEM

The ADuC824 provides a total of twelve interrupt sources with two priority levels. The control and configuration of the interrupt system is carried out through three Interrupt related SFRs, namely :

IE : Interrupt Enable Register.
IP : Interrupt Priority Register.
IEIP2 : Secondary Interrupt Priority-Interrupt Register.

IE : Interrupt Enable Register.

SFR Address A8H
Power-On Default Value 00H
Bit Addessable Yes

EA	EADC	ET2	ES	ET1	EX1	ET0	EX0

Table XX. IE SFR Bit Designations

Bit Location	Bit Mnemonic	Description
IE.7	EA	Written by user to Enable '1' or Disable '0' all Interrupt Sources
IE.6	EADC	Written by user to Enable '1' or Disable '0' ADC Interrupt
IE.5	ET2	Written by user to Enable '1' or Disable '0' Timer2 Interrupt
IE.4	ES	Written by user to Enable '1' or Disable '0' UART Serial Port Interrupt
IE.3	ET1	Written by user to Enable '1' or Disable '0' Timer1 Interrupt
IE.2	EX1	Written by user to Enable '1' or Disable '0' External Interrupt 1
IE.1	ETO	Written by user to Enable '1' or Disable '0' Timer0 Interrupt
IE.0	EX0	Written by user to Enable '1' or Disable '0' External Interrupt 0

IP: Interrupt Priority Register.

SFR Address B8H
Power-On Default Value 00H
Bit Addessable Yes

-	PADC	PT2	PS	PT1	PX1	PT0	PX0

Table XXI. IP SFR Bit Designations

Bit Location	Bit Mnemonic	Description
IP.7	-	Reserved for future use
IP.6	PADC	Written by user to select ADC Interrupt priority ('1' = High ; '0' = Low)
IP.5	PT2	Written by user to select Timer2 Interrupt priority ('1' = High ; '0' = Low)
IP.4	PS	Written by user to select UART Serial Port Interrupt priority ('1' = High ; '0' = Low)
IP.3	PT1	Written by user to select Timer1 Interrupt priority ('1' = High ; '0' = Low)
IP.2	PX1	Written by user to select External Interrupt priority 1 ('1' = High ; '0' = Low)
IP.1	PTO	Written by user to select Timer0 Interrupt priority ('1' = High ; '0' = Low)
IP.0	PX0	Written by user to select External Interrupt 0 priority ('1' = High ; '0' = Low)

IEIP2: **Secondary Interrupt Enable and Priority Register.**

SFR Address A9H
Power-On Default Value A0H
Bit Addessable No

PLOCK	PTI	PPSM	PSI	ELOCK	ETI	EPSM	ESI

Table XXII. IEIP2 SFR Bit Designations

Bit Location	Bit Mnemonic	Description
IEIP.7	PLOCK	Written by user to select PLL LOCK Interrupt priority (‘1’ = High ; ‘0’ = Low)
IEIP.6	PTI	Written by user to select TIC Interrupt priority (‘1’ = High ; ‘0’ = Low)
IEIP.5	PPSM	Written by user to select Power Supply Monitor Interrupt priority (‘1’ = High ; ‘0’ = Low)
IEIP.4	PSI	Written by user to select SPI/I2C Serial Port Interrupt priority (‘1’ = High ; ‘0’ = Low)
IEIP.3	ELOCK	Written by user to Enable ‘1’ or Disable ‘0’ PLL LOCK Interrupt
IEIP.2	ETI	Written by user to Enable ‘1’ or Disable ‘0’ TIC Interrupt
IEIP.1	EPSM	Written by user to Enable ‘1’ or Disable ‘0’ Power Supply Monitor Interrupt
IEIP.0	ESI	Written by user to Enable ‘1’ or Disable ‘0’ SPI/I2C Serial Port Interrupt

Interrupt Priority :
The Interrupt Enable registers are written by the user to enable individual interrupt sources. While the Interrupt Priority registers allow the user to select one of two priority levels for each interrupt. An interrupt of a high priority may interrupt the service routine of a low priority interrupt, and if two interrupts of different priority occur at the same time the higher level interrupt will be serviced first. An interrupt cannot be interrupted by another interrupt of the same priority level. If two interrupts of the same priority level occur simultaneously, a polling sequence is observed as shown in Table XXVIII below:

Source	Priority	Description
IPSM	1 (highest)	Power Supply Monitor Interrupt
LOCK	2	PLL lock Interrupt
WDS	3	Watchdog Interrupt
IE0	4	External Interrupt 0
IADC	5	ADC Interrupt
TF0	6	Timer/counter 0 Interrupt
IE1	7	External Interrupt 1
TF1	8	Timer/Counter 1 Interrupt
II2C + ISPI	9	I2C/SPI Interrupt
RI + TI	10	Serial Interrupt
TF2 + EXF2	11	Timer/Counter 2 Interrupt
TII	12 (lowest)	Timer Interval Counter Interrupt

Table XXIII. Priority within an Interrupt Level

Interrupt Vectors :
When an interrupt occurs the program counter is pushed onto the stack and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are shown below in Table XXIV.

Source	Vector Address
IE0	0003 Hex
TF0	000B Hex
IE1	0013 Hex
TF1	001B Hex
RI + TI	0023 Hex
TF2 + EXF2	002B Hex
IADC	0033 Hex
II2C + ISPI	003B Hex
IPSM	0043 Hex
LOCK	004B Hex
TII	0053 Hex
WDS (WDIR = 1)[1]	005B Hex

Table XXIV. Interrupt Vector Addresses

Notes :
[1] The watchdog can be set up to generate an interrupt instead of a reset when it times out, this is used for logging errors or to examine the internal status of the micro like the PC, stack, etc. to try figure out why a watchdog timeout occurred. The watchdog interrupt is slightly different to the normal interrupts in that its priority level is always set to 1 and it is not possible to disable the interrupt via the global disable bit (EA) in the IE SFR. This is done to ensure that the interrupt will be responded to if a watchdog timeout occurs. Note that the watchdog will only produce an interrupt if the watchdog timeout is greater than zero.

ADuC824 QuickStart DEVELOPMENT SYSTEM

The QuickStart Development System is a full featured, low cost development tool suite supporting the ADuC824 The system consists of the following PC-based (Win95-compatible) hardware and software development tools.

Hardware :	ADuC824 Evaluation Board, Plug-in Power Supply and Serial Port Cable
Code Development :	8051 Assembler C Compiler (2K Code Limited)
Code Functionality :	ADSIM, Windows MicroConverter Code Simulator
In-Circuit Code Download :	FLASH/EE UART-Serial Downloader
Windows Debugger :	Serial Port Debugger
Misc. Other :	CD-ROM Documentation and 2 additional Prototype Devices

Figures 14 below shows the typical components of a QuickStart Development System while Figure 15 shows a typical debug session. A brief description of some of the software tools' components in the QuickStart Development System is given below.

Figure 14. Components of the QuickStart Development System

Figure 15. Typical Debug Session

Download - In-Circuit Serial Downloader
The Serial Downloader is a software program that allows you to serially download an assembled program (Intel Hex format file) to the on-chip program FLASH memory via the serial COM1 port on a standard PC. An Application Note (uC004) detailing this serial download protocol is available from the www.analog.com/microconverter.

DeBug - Windows Debugger
The Debugger is a Windows application that allows the user to debug code execution on silicon using the MicroConverter UART serial port. The debugger provides access to all on-chip peripherals during a typical debug session as well as single-step and break-point code execution control.

ADSIM - Windows Simulator
The Simulator is a Windows application that fully simulates all the MicroConverter functionality including ADC and DAC peripherals. The simulator provides an easy to use, intuitive interface to the MicroConverter functionality and integrates many standard debug features including multiple breakpoints, single stepping and code execution trace capability. This tool can be used both as a tutorial guide to the part as well as an efficient way to prove code functionality before moving to a hardware platform.

The QuickStart software development tool-suite is freely available at the Analog Devices MicroConverter Web-Site :
www.analog.com/microconverter