Multiport Internet Gateway Processor

ADSP-21mod970

FEATURES

PERFORMANCE

Complete Single-Chip Multiport Internet Gateway Processor (No External Memory Required)

Implements Six Modem Channels in One Package

Each Processor Can Implement V.34/V.90 Data/Fax Modem (Includes Datapump and Controller)

312 MIPS Sustained Performance, 19 ns Instruction Time @ 3.3 V

Open Architecture Extensible to Voice Over IP and Other Applications

Low Power Dissipation, 100 mW (Typical) per Digital Modem Processor

Power-Down Mode Featuring Low CMOS Standby Power Dissipation

INTEGRATION

ADSP-2100 Family Code Compatible, with Instruction Set Extensions

960K Bytes of On-Chip RAM, Configured as 576K Bytes of Program Memory and 384K Bytes of Data Memory

Dual Purpose Program Memory for Both Instruction and Data Storage

304-Ball PBGA with a 1.45 Square Inch (961 sq. mm) Footprint

SYSTEM CONFIGURATION

16-Bit Internal DMA Port for High Speed Access to On-Chip Memory (Mode Selectable)

Programmable Multichannel Serial Port Supports 24 Channels/32 Channels

Two Double-Buffered Serial Ports with Companding Hardware and Automatic Data Buffering

Separate RESET Pins for Each Internal Processor

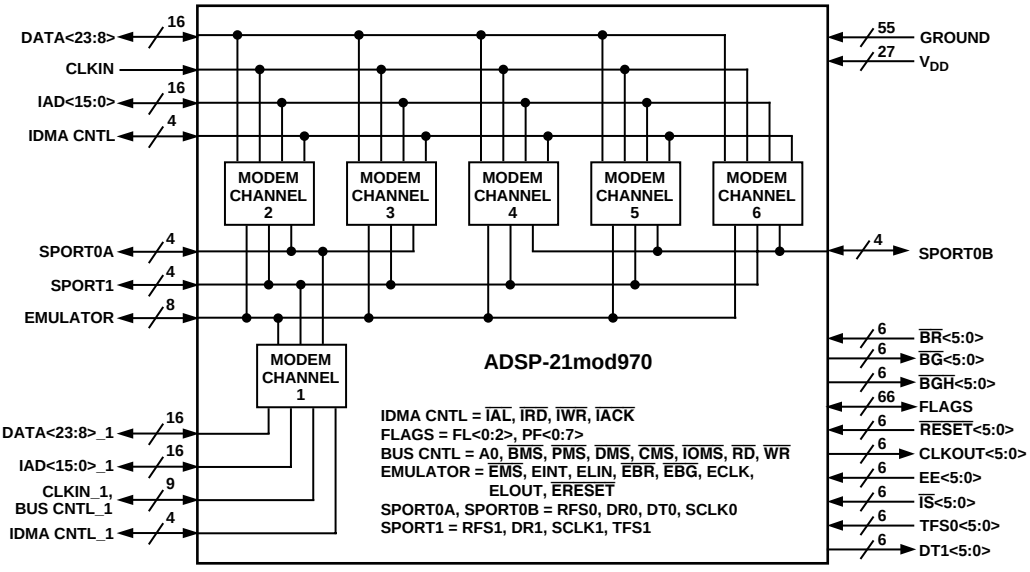
GENERAL DESCRIPTION

The ADSP-21mod970 is a Multiport Internet Gateway Processor optimized for implementation of a complete V.34/56K modem. All data pump and controller functions can be implemented on a single device, offering the lowest power consumption and highest possible modem port density.

The ADSP-21mod970 combines the ADSP-2100 family base architecture (three computational units, data address generators and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, Flag I/O, extensive interrupt capabilities and on-chip program and data memory.

The ADSP-21mod970 integrates 960 bytes of on-chip memory, configured as 192K words (24-bit) of program RAM, and 192K words (16-bit) of data RAM. Power-down circuitry is also provided to meet the low power needs of battery operated portable equipment. The ADSP-21mod970 is available in a 31 sq-mm., 304-lead PBGA package.

FUNCTIONAL BLOCK DIAGRAM



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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

Fabricated in a high speed, low power, CMOS process, the ADSP-21mod970 operates with a 19 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSP-21mod970's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle, the ADSP-21mod970 can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

This takes place while the processor continues to:

- Receive and transmit data through the two serial ports
- Receive and/or transmit data through the internal DMA port
- Receive and/or transmit data through the byte DMA port
- Decrement timer

Modem Software
The modem software executes general modem control, command sets, error correction and data compression, data modulations (for example, V.90 and V.34), and host interface functions. The host interface allows system access to modem statistics such as call progress, connect speed, retrain count, symbol rate and other modulation parameters.

The modem data pump and controller software reside in on-chip SRAM and do not require additional memory. The user can configure the ADSP-21mod970 dynamically by downloading software from the host through the 16-bit DMA interface. This SRAM-based architecture provides a software upgrade path to future standards and applications, such as voice over IP.

The modem software is available as object code.

DEVELOPMENT SYSTEM

The ADSP-2100 Family Development Software, a complete set of tools for software and hardware system development, supports the ADSP-21mod970. The System Builder provides a high level method for defining the architecture of systems under development. The Assembler has an algebraic syntax that is easy to program and debug. The Linker combines object files into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface to display different portions of the hardware environment.

A PROM Splitter generates PROM programmer compatible files. The C Compiler, based on the Free Software Foundation's GNU C Compiler, generates ADSP-21mod970 assembly source code. The source code debugger allows programs to be corrected in the C environment. The Runtime Library includes over 100 ANSI-standard mathematical and DSP-specific functions.

The ADSP-218x EZ-ICE® Emulator aids in the hardware debugging of an ADSP-21mod970 system. The EZ-ICE, in conjunction with the required processor selection hardware, lets you independently debug code on individual modem processors. The emulator consists of hardware, host computer resident software, and the target board connector. The ADSP-21mod970 integrates on-chip emulation support with a 14-pin ICE-Port™ interface. The ADSP-21mod970 device need not be removed from the target system when using the EZ-ICE, nor are any adapters needed. Due to the small footprint of the EZ-ICE connector, emulation can be supported in final board designs.

The EZ-ICE performs a full range of functions, including:

- In-target operation
- Up to 20 breakpoints
- Single-step or full-speed operation
- Registers and memory values can be examined and altered
- PC upload and download functions
- Instruction-level emulation of program booting and execution
- Complete assembly and disassembly of instructions
- C source-level debugging

See "Designing An EZ-ICE-Compatible Target System" in the *ADSP-2100 Family EZ-Tools Manual* (ADSP-2181 sections) as well as the Designing an EZ-ICE Compatible System section of this data sheet for the exact specifications of the EZ-ICE target board connector.

Additional Information
This data sheet provides a general overview of ADSP-21mod970 functionality. For specific information about the modem processors, refer to the ADSP-21mod870 data sheet. For additional information on the architecture and instruction set of the modem processors, refer to the *ADSP-2100 Family User's Manual, Third Edition*. For more information about the development tools, refer to the ADSP-2100 Family Development Tools Data Sheet.

ARCHITECTURE OVERVIEW

Figure 1 is an overall block diagram of the ADSP-21mod970 modem pool. The modem pool contains six independent digital modem processors.

Each individual modem processor has a DSP core, 160K bytes of RAM, two serial ports, and a DMA port. The signals for a single processor are shown in Figure 2. The signals of each modem processor are accessed through the external pins of the ADSP-21mod970. Some signals are bused with the signals of the other processors and are accessed through a single external pin. Other signals remain separate and they are accessed through separate external pins for each processor.

The arrangement of the six modem processors in the ADSP-21mod970 makes two basic configurations possible: a master configuration and a slave configuration. In both configurations, the control and data pins of five of the six processors connect to a single bus structure. The control and data pins of the one modem processor (Modem Processor 1) are separate from the other modem processors and accessed through external pins.

In Slave Mode, all six modem processors have identical functions and have equal status. Each modem processor is connected to a common DMA bus and each modem processor is configured to operate in the same mode (see the Slave Mode and the Memory Mode descriptions in the *Memory Architecture*

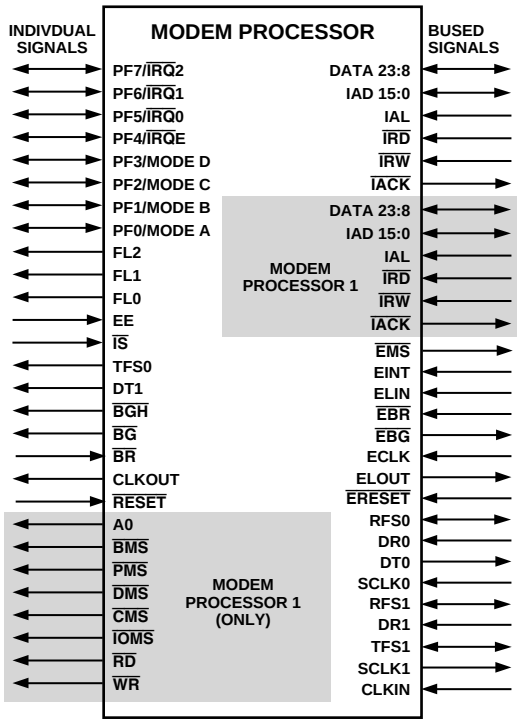


Figure 2. Modem Processor Signals

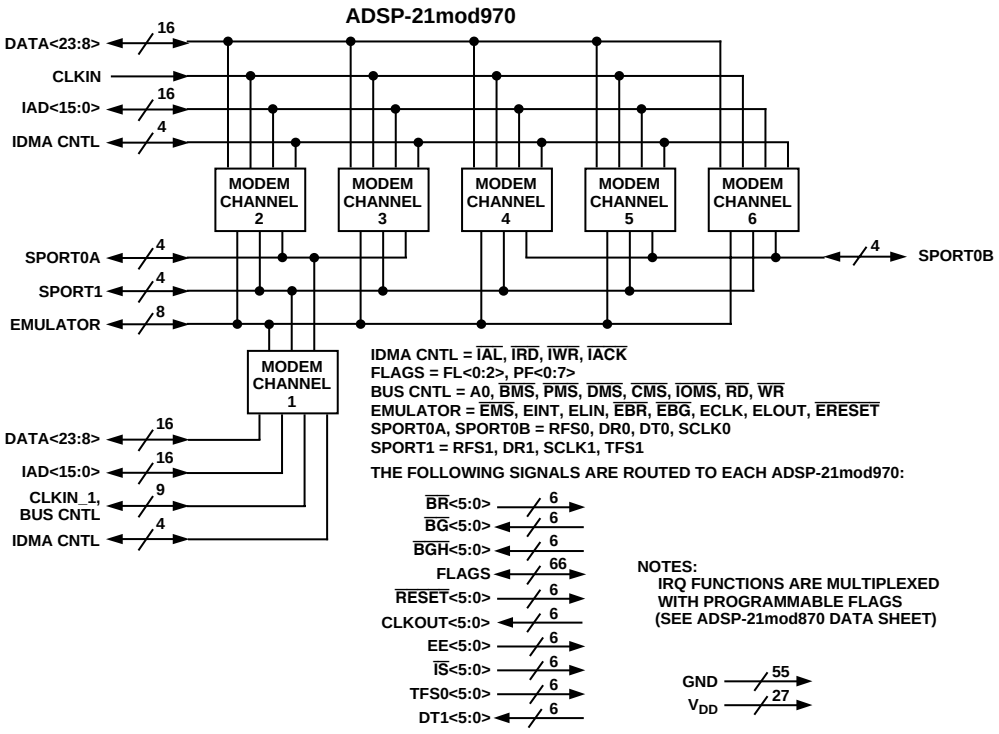


Figure 1. Modem Pool

section). The Slave Mode is considered to be the normal mode of operation in a modem pool application. Figure 3 shows the modem pool configured for slave mode operation.

The master mode of the ADSP-21mod970 configures five of the modem processors with identical functions and isolates one of the modem processors, Processor 1. In the Master Mode, Processor 1 is not connected to the DMA bus as are the other five modem processors. Processor 1 operates in a different mode where external pins can be used for access to a 16-bit data bus, a 14-bit address bus with associated bus control pins. In master mode, Processor 1 is treated as a master of the modem pool and communicates with an external device such as a RAM, ROM or a memory shared with a host processor. In this configuration, the master processor performs some controlling function of the remaining five modem processors. Figure 4 shows the modem pool configured for Slave Mode operation.

Since the memory bus of Processor 1 is accessible via external pins in master mode, Processor 1 can be configured for one of the several memory modes available on the ADSP-21xx family. (See Full Memory, Host Mode Descriptions.)

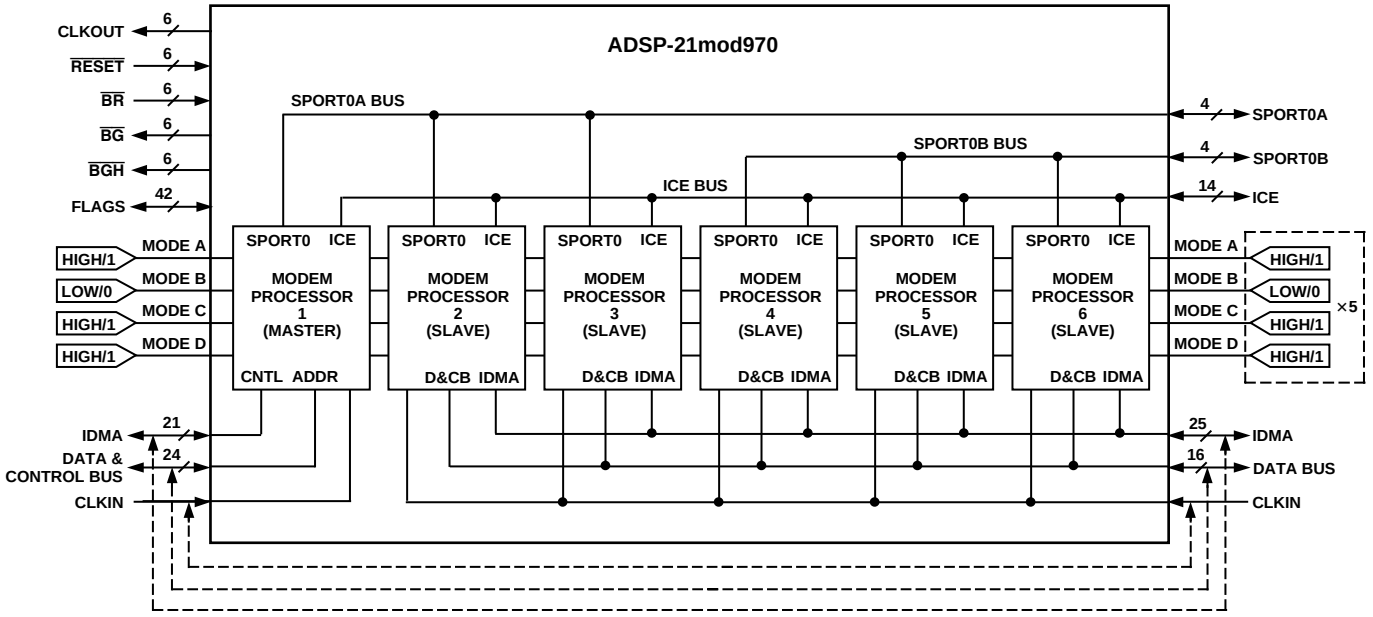


Figure 3. Configured for Slave Mode

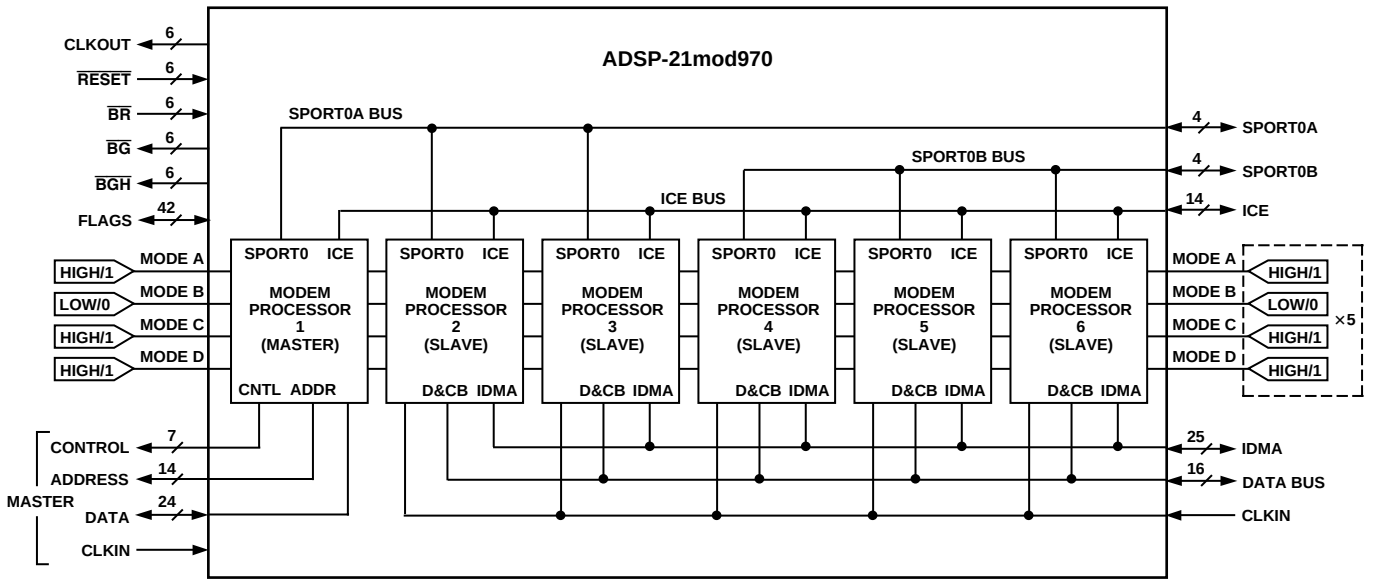


Figure 4. Configured for Master Mode

Serial Ports

The ADSP-21mod970 has a multichannel serial port (SPORT) connected to each internal digital modem processor for serial communications.

Following is a brief list of the capabilities of the ADSP-21mod970 SPORT. For additional information on the internal Serial Ports, refer to the *ADSP-2100 Family User's Manual, Third Edition.*

- SPORT is bidirectional and has a separate, double-buffered transmit and receive section.
- SPORT can use an external serial clock or generate its own serial clock internally.
- SPORT has independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulsewidths and timings.
- SPORT supports serial data word lengths from 3 to 16 bits and provides optional A-law and μ-law companding according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORT can receive and transmit an entire circular buffer of data with one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- A multichannel interface selectively receives and transmits a 24- or 32-word, time-division multiplexed, serial bitstream.

PIN DESCRIPTIONS

The ADSP-21mod970 is available in a 304-lead PBGA package. In order to maintain maximum functionality and reduce package size and pin count, some serial port, programmable flag, interrupt and external bus pins have dual, multiplexed functionality. The external bus pins are configured during $\overline{\text{RESET}}$ only, while serial port pins are software configurable during program execution. Flag and interrupt functionality is retained concurrently on multiplexed pins. In cases where pin functionality is reconfigurable, the default state is shown in plain text; alternate functionality is shown in italics.

Common-Mode Pins

Pin Name(s)	# of Pins	Input/ Output	Function
$\overline{\text{RESET}}$	6	I	Processor Reset Input
$\overline{\text{BR}}$	6	I	Bus Request Input
$\overline{\text{BG}}$	6	O	Bus Grant Output
$\overline{\text{BGH}}$	6	O	Bus Grant Hang Output
$\overline{\text{DMS}}$	1	O	Data Memory Select Output
$\overline{\text{PMS}}$	1	O	Program Memory Select Output
$\overline{\text{BMS}}$	1	O	Byte Memory Select Output
$\overline{\text{IOMS}}$	I	O	I/O Memory Select Output
$\overline{\text{CMS}}$	1	O	Combined Memory Select Output
$\overline{\text{RD}}$	1	O	Memory Read Enable Output
$\overline{\text{WR}}$	1	O	Memory Write Enable Output
$\overline{\text{IRQ2}}$/	6	I	Edge- or Level-Sensitive Interrupt Request[1]
PF7		I/O	*Programmable I/O Pin*
$\overline{\text{IRQL1}}$/	6	I	Level-Sensitive Interrupt Requests[1]
PF6		I/O	*Programmable I/O Pin*
$\overline{\text{IRQL0}}$/	6	I	Level-Sensitive Interrupt Requests[1]
PF5		I/O	*Programmable I/O Pin*
$\overline{\text{IRQE}}$/	6	I	Edge-Sensitive Interrupt Requests[1]
PF4		I/O	*Programmable I/O Pin*
Mode D/	6	I	Mode Select Input—Checked Only During $\overline{\text{RESET}}$
PF3		I/O	*Programmable I/O Pin During Normal Operation*
Mode C/	6	I	Mode Select Input—Checked Only During $\overline{\text{RESET}}$
PF2		I/O	*Programmable I/O Pin During Normal Operation*
Mode B/	6	I	Mode Select Input—Checked Only During $\overline{\text{RESET}}$
PF1		I/O	*Programmable I/O Pin During Normal Operation*
Mode A/	6	I	Mode Select Input—Checked Only During RESET
PF0		I/O	*Programmable I/O Pin During Normal Operation*
CLKIN	2	I	Clock Input
CLKOUT	6	O	Processor Clock Output
SPORT	24	I/O	Serial Port I/O Pins[2]
FL0, FL1, FL2	18	O	Output Flags
V_{DD} and GND	82	I	Power and Ground
EZ-Port	14	I/O	For Emulation Use

NOTES

[1]Interrupt/Flag Pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, the modem pool will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices, or set as a programmable flag.

[2]SPORT configuration determined by the modem pool's System Control Register. Software configurable.

Memory Interface Pins
The ADSP-21mod970 modem pool can be used in one of two modes, master mode or slave mode. In master mode, Modem Processor 1 operates with full memory (BDMA operation with full external overlay memory and I/O capability). In Slave Mode, Modem Processor 1 operates in host configuration (IDMA operation with limited external addressing capabilities). The operating mode is determined by the state of the Mode C pin during $\overline{\text{RESET}}$ and cannot be changed while the modem pool is running. See the Memory Architecture section for more information.

Full Memory Pins (Mode C = 0) Modem Processor 1 Only

Pin Name	# of Pins	Input/ Output	Function
A13:0	14	O	Address Output Pins for Program, Data, Byte and I/O Spaces
D23:0	24	I/O	Data I/O Pins for Program, Data, Byte and I/O Spaces (8 MSBs Are Also Used as Byte Memory Addresses)

Host Pins (Mode C = 1)*
Modem Processor 1 and Modem Processors 2–6

Pin Name	# of Pins	Input/ Output	Function
IAD15:0	32	I/O	IDMA Port Address/Data Bus
A0	1	O	Address Pin for External I/O, Program, Data, or Byte Access (Modem Processor 1 Only)
D23:8	32	I/O	Data I/O Pins for Program, Data Byte and I/O Spaces
$\overline{\text{IWR}}$	2	I	IDMA Write Enable
$\overline{\text{IRD}}$	2	I	IDMA Read Enable
IAL	2	I	IDMA Address Latch Pin
$\overline{\text{IS}}$	6	I	IDMA Select
$\overline{\text{IACK}}$	2	O	IDMA Port Acknowledge Configurable in Mode D; Open Drain

*In Host Mode, external peripheral addresses can be decoded using the A0, $\overline{\text{CMS}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$ and $\overline{\text{IOMS}}$ signals of Modem Processor 1.

Interrupts
The interrupt controller allows each modem processor in the modem pool to respond individually to eleven possible interrupts and reset with minimum overhead. The ADSP-21mod970 provides four dedicated external interrupt input pins, $\overline{\text{IRQ2}}$, $\overline{\text{IRQL1}}$, $\overline{\text{IRQL0}}$, and $\overline{\text{IRQE}}$ (shared with the PF7:4 pins) for each modem processor. The ADSP-21mod970 also supports internal interrupts from the timer, the byte DMA port, the serial port, software and the power-down control circuit. The interrupt levels are internally prioritized and individually maskable (except power-down and reset). The $\overline{\text{IRQ2}}$, $\overline{\text{IRQL1}}$, and $\overline{\text{IRQL0}}$ input pins can be programmed to be either level- or edge-sensitive. $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ are level-sensitive and $\overline{\text{IRQE}}$ is edge sensitive. The priorities and vector addresses of all interrupts are shown in Table I.

Table I. Interrupt Priority and Interrupt Vector Addresses

Source Of Interrupt	Interrupt Vector Address (Hex)
$\overline{\text{RESET}}$ (or Power-Up with PUCR = 1)	0000 (Highest Priority)
Power-Down (Nonmaskable)	002C
$\overline{\text{IRQ2}}$	0004
$\overline{\text{IRQL1}}$	0008
$\overline{\text{IRQL0}}$	000C
SPORT0 Transmit	0010
SPORT0 Receive	0014
$\overline{\text{IRQE}}$	0018
BDMA Interrupt	001C
SPORT1 Transmit or $\overline{\text{IRQ1}}$	0020
SPORT1 Receive or $\overline{\text{IRQ0}}$	0024
Timer	0028 (Lowest Priority)

When the modem pool is reset, interrupt servicing is disabled.

LOW POWER OPERATION
The ADSP-21mod970 has three low power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down
The ADSP-21mod970 modem pool has a low power feature that lets the modem pool enter a very low power dormant state through software control. Following is a brief list of power-down features. Refer to the *ADSP-2100 Family User's Manual, Third Edition,* "System Interface" chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The modem pool begins executing instructions in as few as 400 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 400 CLKIN cycle recovery.
- Power-down is initiated by the software power-down force bit. Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the modem pool to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{\text{RESET}}$ pin also can be used to terminate power-down.

Idle
When the ADSP-21mod970 is in the idle mode, the modem pool waits indefinitely in a low power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In idle mode IDMA, BDMA and autobuffer cycle steals still occur.

Slow Idle

The IDLE instruction is enhanced on the ADSP-21mod970 to let the modem pool's internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction.

The format of the instruction is

IDLE (n);

where *n* = 16, 32, 64 or 128. This instruction keeps the modem pool fully functional, but operating at the slower clock rate. While it is in this state, the modem pool's other internal clock signals, such as SCLK, CLKOUT and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard IDLE instruction.

When the IDLE (*n*) instruction is used, it effectively slows down the modem pool's internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by *n*, the clock divisor. When an enabled interrupt is received, the ADSP-21mod970 will remain in the idle state for up to a maximum of *n* modem pool cycles (*n* = 16, 32, 64 or 128) before resuming normal operation.

When the IDLE (*n*) instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the modem pool's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the modem pool takes to come out of the idle state (a maximum of *n* cycles).

SYSTEM CONFIGURATION

Figure 5 shows a typical multichannel modem configuration with the ADSP-21mod970. A line interface can be used to connect the multichannel subscriber or client data stream to the multichannel serial port of the ADSP-21mod970. The ADSP-21mod970 can support up to 64 channels. The IDMA port of the ADSP-21mod970 is used to give a host processor full access to the internal memory of the ADSP-21mod970. This lets the host dynamically configure the ADSP-21mod970 by loading code and data into its internal memory. This configuration also lets the host access server data directly from the ADSP-21mod970's internal memory. In this configuration, the Modem Processor 1 should be put into host memory mode where Mode D = 1, Mode C = 1, Mode B = 0, and Mode A = 1 (see Table II).

CLOCK SIGNALS

The ADSP-21mod970 is clocked by a TTL-compatible clock signal that runs at half the instruction rate; a 26 MHz input clock yields a 19 ns processor cycle (which is equivalent to 52 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled. The clock input signal is connected to the processor's CLKIN input.

The CLKIN input cannot be halted, changed during operation, or operated below the specified frequency during normal operation. The only exception is while the processor is in the power-down state. For additional information, refer to Chapter 9, *ADSP-2100 Family User's Manual, Third Edition,* for a detailed explanation of this power-down feature.

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate.

Reset

The $\overline{\text{RESET}}$ signals initiate a reset of each modem processor in the ADSP-21mod970. The $\overline{\text{RESET}}$ signals must be asserted during the power-up sequence to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to let the internal clocks stabilize. If $\overline{\text{RESET}}$s are activated any time after power-up, the clocks continue to run and do not require stabilization time.

The power-up sequence is defined as the total time required for the oscillator circuits to stabilize after a valid V_{DD} is applied to the processors, and for the internal phase-locked loops (PLL) to lock onto the specific frequency. A minimum of 2000 CLKIN cycles ensures that the PLLs have locked, but this does not include the oscillators start-up time. During this power-up sequence, the RESET signals should be held low. On any subsequent resets, the RESET signals must meet the minimum pulsewidth specification, t_{RSP}.

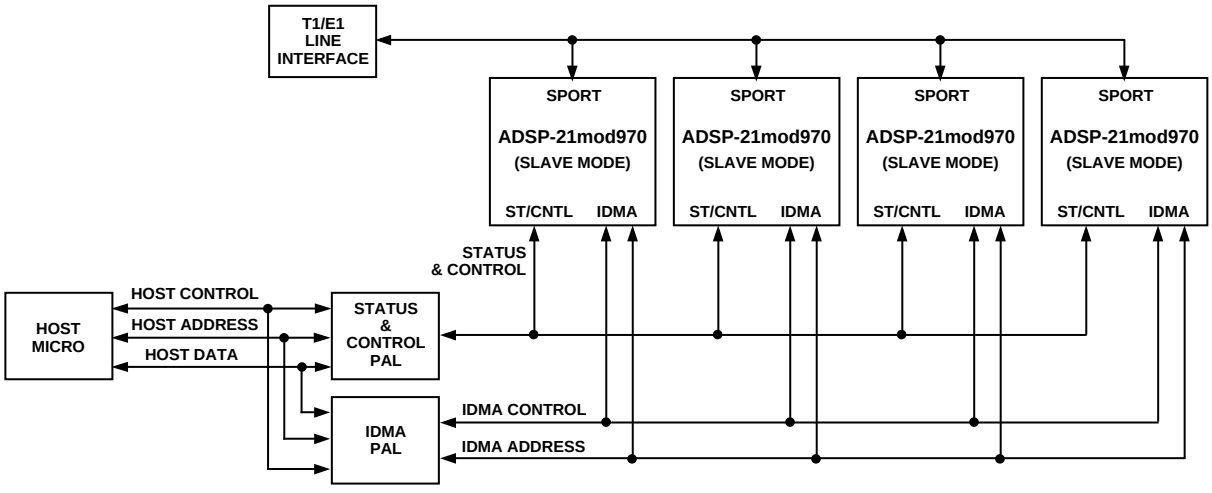


Figure 5. Multichannel Modem Configuration

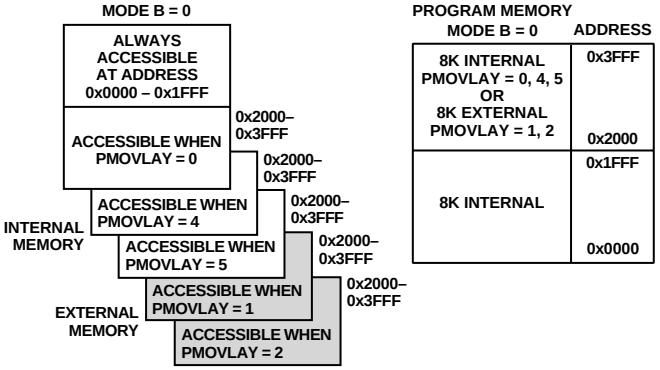
The $\overline{\text{RESET}}$ inputs contain some hysteresis; however, if an RC circuit is used to generate the $\overline{\text{RESET}}$ signals, the use of external Schmidt triggers are recommended.

The reset for each individual modem processor sets the internal stack pointers to the empty stack condition, masks all interrupts and clears the MSTAT register. When a $\overline{\text{RESET}}$ is released, if there is no pending bus request and the modem processor is configured for booting, the boot-loading sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

MEMORY ARCHITECTURE

The ADSP-21mod970 provides a variety of memory and peripheral interface options for Modem Processor 1. The key functional groups are Program Memory, Data Memory, Byte Memory and I/O. Refer to the figures and tables below for PM and DM memory allocations in the ADSP-21mod970.

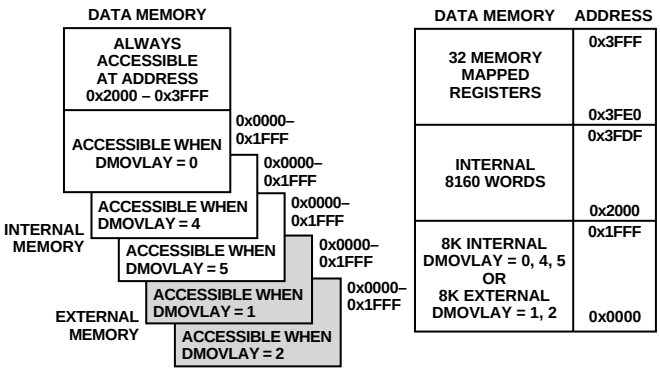
The ADSP-21mod970 modem pool operates in one of two memory modes: Slave Mode or Master Mode. The memory modes determine the memory access to Modem Processor 1. In Slave Mode, the memory of Modem Processor 1 is configured for Host Mode; in Master Mode, the memory of Modem Processor 1 is configured for Full-Memory Mode. Memories for Modem Processors 2–6 are configured only for Host Mode. The differences between these memory modes are explained in the following sections. Figure 6 shows Program Memory, while Figure 7 shows Data Memory. Table II summarizes ADSP-21mod970 operating modes. Table III explains the mode bits and memory booting.



PMOVLAY	MEMORY	A13*	A12:0*
0, 4, 5	INTERNAL	NOT APPLICABLE	NOT APPLICABLE
1	EXTERNAL OVERLAY1	0	13 LSBs OF ADDRESS BETWEEN 0x2000 AND 0x3FFF
2	EXTERNAL OVERLAY2	1	13 LSBs OF ADDRESS BETWEEN 0x2000 AND 0x3FFF

*FULL-MEMORY MODE ONLY

Figure 6. Program Memory (Memory Shown in Grey Is Accessible Only in Full-Memory Mode)



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*FULL-MEMORY MODE ONLY

Figure 7. Data Memory

Table II. Processor and Memory Mode

Memory Modes for Modem Processor 1	ADSP-21mod970 Modes	
	Master	**Slave**
Host	• All Internal Program Memory Available • All Internal Data Memory Available • IDMA Port Enabled	• All Internal Program Memory Available • All Internal Data Memory Available • IDMA Port Enabled
Full-Memory	• All Internal and External Program Memory Available • All Internal and External Data Memory Available • I/O Space Available • Byte Memory DMA (BDMA) Enabled	Not Applicable

Table III. Modes of Operation

MODE D	MODE C	MODE B	MODE A	Booting Method
X	0	0	0	BDMA feature is used to load the first 32 program memory words from byte memory space. Program execution is held off until all 32 words are loaded. Chip is configured in Full-Memory Mode[1]
0	1	0	0	BDMA feature is used to load the first 32 program memory words from byte memory space. Program execution is held off until all 32 words are loaded. Chip is configured in Host Mode. $\overline{\text{IACK}}$ requires pull-down. (**REQUIRES ADDITIONAL HARDWARE.**)
0	1	0	1	IDMA feature is used to load internal memory as desired. Program execution is held off until internal program memory location 0x0000 is written to. Chip is configured in Host Mode.[1] $\overline{\text{IACK}}$ requires pull-down.
1	1	0	0	BDMA feature is used to load the first 32 program memory words from byte memory space. Program execution is held off until all 32 words are loaded. Chip is configured in Host Mode. IACK requires external pull-down. (**REQUIRES ADDITIONAL HARDWARE.**)
1	1	0	1	IDMA feature is used to load internal memory as desired. Program execution is held off until internal program memory location 0x0000 is written to. Chip is configured in Host Mode.[1] $\overline{\text{IACK}}$ requires external pull-down.[1]

NOTE
[1]Considered standard operating settings. These configurations simplify your design and improve memory management.

Slave Mode
This section describes the Slave Mode memory configuration of Modem Processor 1. Modem Processors 2–6 are always configured for Slave Mode.

Program Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0). External program execution is not available in host mode due to a restricted data bus that is 16-bits wide only.

Data Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0).

Internal Memory DMA Port (IDMA Port; Host Memory Mode)
The IDMA Port provides an efficient way for a host system and the ADSP-21mod970 to communicate. The port is used to access the on-chip program memory and data memory of each modem processor with only one processor cycle per word overhead. The IDMA port cannot be used, however, to write to the processor's memory-mapped control registers. A typical IDMA transfer process is described as follows:

1. Host starts IDMA transfer.
2. Host checks $\overline{\text{IACK}}$ control line to see if the processor is busy.
3. Host uses $\overline{\text{IS}}$ and IAL control lines to latch either the DMA starting address (IDMAA) or the PM/DM OVLAY selection into the processor's IDMA control registers.

   If IAD [15] = 1, the value of IAD [7:0] represent the IDMA overlay: IAD [14:8] must be set to 0.

   If IAD [15] = 0, the value of IAD [13:0] represent the starting address of internal memory to be accessed and IAD [14] reflects PM or DM for access.
4. Host uses $\overline{\text{IS}}$ and $\overline{\text{IRD}}$ (or $\overline{\text{IWR}}$) to read (or write) processor internal memory (PM or DM).
5. Host checks $\overline{\text{IACK}}$ line to see if the processor has completed the previous IDMA operation.
6. Host ends IDMA transfer.

The IDMA port has a 16-bit multiplexed address and data bus and supports 24-bit program memory. The IDMA port is completely asynchronous and can be written to while the ADSP-21mod970 is operating at full speed.

The processor memory address is latched and then automatically incremented after each IDMA transaction. An external device can therefore access a block of sequentially addressed memory by specifying only the starting address of the block. This increases throughput as the address does not have to be sent for each memory access.

IDMA Port access occurs in two phases. The first is the IDMA Address Latch cycle. When the acknowledge is asserted, a 14-bit address and 1-bit destination type can be driven onto the bus by an external device. The address specifies an on-chip memory location, the destination type specifies whether it is a DM or PM access. The falling edge of the address latch signal latches this value into the IDMAA register.

Once the address is stored, data can then either be read from or written to, the ADSP-21mod970's on-chip memory. Asserting the select line ($\overline{\text{IS}}$) and the appropriate read or write line ($\overline{\text{IRD}}$ and $\overline{\text{IWR}}$ respectively) signals the ADSP-21mod970 that a particular transaction is required. In either case, there is a one-processor-cycle delay for synchronization. The memory access consumes one additional processor cycle.

Once an access has occurred, the latched address is automatically incremented, and another access can occur.

Through the IDMAA register, the processor can also specify the starting address and data format for DMA operation. Asserting the IDMA port select ($\overline{\text{IS}}$) and address latch enable (IAL) directs the ADSP-21mod970 to write the address onto the

IAD0[14.0] bus into the IDMA Control Register. If IAD[15] is set to 0, IDMA latches the address. If IAD[15] is set to 1, IDMA latches OVLAY memory. The IDMAA register is memory mapped at address DM (0x3FE0). Note that the latched address (IDMAA) cannot be read back by the host. The IDMA Overlay Register is memory mapped at address DM (0x3FE7). See Figure 8 for more information on IDMA memory maps.

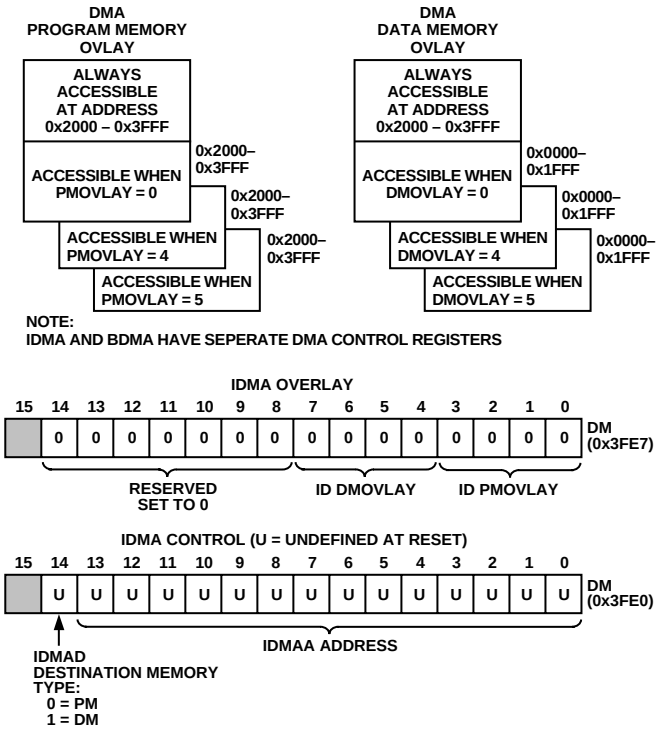


Figure 8. IDMA Control/OVLAY Registers

IDMA Port Booting
The ADSP-21mod970 can also boot programs through its Internal DMA port. If Mode C = 1, Mode B = 0, and Mode A = 1, the ADSP-21mod970 boots from the IDMA port. IDMA feature can load as much on-chip memory as desired. Program execution is held off until on-chip program memory location 0 is written to.

Master Mode
This section describes the Master Mode memory configuration of Modem Processor 1. Master Mode is not available for Modem Processors 2–6.

Program Memory (Full Memory Mode) is a 24-bit-wide space for storing both instruction op codes and data. The ADSP-21mod970 has 32K words of Program Memory RAM on chip, and it can access up to two 8K external memory overlay spaces using the external data bus.

Data Memory (Full Memory Mode) is a 16-bit-wide space used for the storage of data variables and for memory-mapped control registers. The ADSP-21mod970 has 32K words on Data Memory RAM on chip, consisting of 16,352 user-accessible locations and 32 memory-mapped registers. The ADSP-21mod970 also supports up to two 8K external memory overlay spaces through the external data bus. All internal accesses complete in one cycle. Accesses to external memory are timed using the wait states specified by the DWAIT register.

I/O Space (Full Memory Mode)
The ADSP-21mod970 supports an additional external memory space called I/O space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports 2048 locations of 16-bit wide data. The lower eleven bits of the external address bus are used; the upper three bits are undefined. Two instructions were added to the core ADSP-2100 Family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated three-bit wait state registers, IOWAIT0-3, which specify up to seven wait states to be automatically generated for each of four regions. The wait states act on address ranges as shown in Table IV.

Table IV. Wait States

Address Range	Wait State Register
0x000–0x1FF	IOWAIT0
0x200–0x3FF	IOWAIT1
0x400–0x5FF	IOWAIT2
0x600–0x7FF	IOWAIT3

Byte Memory
The byte memory space is a bidirectional, 8-bit-wide, external memory space used to store programs and data. Byte memory is accessed using the BDMA feature. The byte memory space consists of 256 pages, each of which is 16K × 8.

The byte memory space on the ADSP-21mod970 supports read and write operations as well as four different data formats. The byte memory uses data bits 15:8 for data. The byte memory uses Data Bits 23:16 and Address Bits 13:0 to create a 22-bit address. This allows up to a 4 meg × 8 (32 megabit) ROM or RAM to be used without glue logic. All byte memory accesses are timed by the BMWAIT register.

Byte Memory DMA (BDMA, Full Memory Mode)
The byte memory DMA controller allows loading and storing of program instructions and data using the byte memory space. The BDMA circuit can access the byte memory space while the processor is operating normally and steals only one processor cycle per 8-, 16- or 24-bit word transferred.

The BDMA circuit supports four different data formats that are selected by the BTYPE register field. The appropriate number of 8-bit accesses are done from the byte memory space to build the word size selected. Table V shows the data formats supported by the BDMA circuit.

Table V. Data Formats

BTYPE	Internal Memory Space	Word Size	Alignment
00	Program Memory	24	Full Word
01	Data Memory	16	Full Word
10	Data Memory	8	MSBs
11	Data Memory	8	LSBs

Unused bits in the 8-bit data memory formats are filled with 0s. The BIAD register field is used to specify the starting address for the on-chip memory involved with the transfer. The 14-bit BEAD register specifies the starting address for the external byte

memory space. The 8-bit BMPAGE register specifies the starting page for the external byte memory space. The BDIR register field selects the direction of the transfer. Finally the 14-bit BWCOUNT register specifies the number of DSP words to transfer and initiates the BDMA circuit transfers.

BDMA accesses can cross page boundaries during sequential addressing. A BDMA interrupt is generated on the completion of the number of transfers specified by the BWCOUNT register.

The BWCOUNT register is updated after each transfer so it can be used to check the status of the transfers. When it reaches zero, the transfers have finished and a BDMA interrupt is generated. The BMPAGE and BEAD registers must not be accessed by the processor during BDMA operations.

The source or destination of a BDMA transfer will always be on-chip program or data memory.

When the BWCOUNT register is written with a nonzero value the BDMA circuit starts executing byte memory accesses with wait states set by BMWAIT. These accesses continue until the count reaches zero. When enough accesses have occurred to create a destination word, it is transferred to or from on-chip memory. The transfer takes one processor cycle. Processor accesses to external memory have priority over BDMA byte memory accesses.

The BDMA Context Reset bit (BCR) controls whether the processor is held off while the BDMA accesses are occurring. Setting the BCR bit to 0 allows the processor to continue operations. Setting the BCR bit to 1 causes the processor to stop execution while the BDMA accesses are occurring, to clear the context of the processor, and start execution at Address 0 when the BDMA accesses have completed. The BDMA overlay bits specify the OVLAY memory blocks to be accessed for internal memory.

Bootstrap Loading (Booting)

The ADSP-21mod970 has two mechanisms to allow automatic loading of the internal program memory after reset. The method for booting is controlled by the Mode A, B and C configuration bits. When the MODE pins specify BDMA booting, the ADSP-21mod970 initiates a BDMA boot sequence when reset is released.

The BDMA interface is set up during reset to the following defaults when BDMA booting is specified: the BDIR, BMPAGE, BIAD and BEAD registers are set to 0, the BTYPE register is set to 0 to specify program memory 24-bit words, and the BWCOUNT register is set to 32. This causes 32 words of on-chip program memory to be loaded from byte memory. These 32 words are used to set up the BDMA to load in the remaining program code. The BCR bit is also set to 1, which causes program execution to be held off until all 32 words are loaded into on-chip program memory. Execution then begins at Address 0.

The ADSP-2100 Family development software (Revision 5.02 and later) fully supports the BDMA booting feature and can generate byte memory space compatible boot code.

The IDLE instruction can also be used to allow the processor to hold off execution while booting continues through the BDMA interface. For BDMA accesses while in Host Mode, the addresses to boot memory must be constructed externally to the ADSP-21mod970. The only memory address bit provided by the processor is A0.

Composite Memory Select ($\overline{\text{CMS}}$)

The ADSP-21mod970 has a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$) but can combine their functionality.

Each bit in the CMSSEL register, when set, causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the $\overline{\text{PMS}}$ and $\overline{\text{DMS}}$ bits in the CMSSEL register and use the $\overline{\text{CMS}}$ pin to drive the chip select of the memory, and use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The $\overline{\text{CMS}}$ pin functions like the other memory select signals with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the $\overline{\text{CMS}}$ signal at the same time as the selected memory select signal. All enable bits default to 1 at reset, except the $\overline{\text{BMS}}$ bit.

Boot Memory Select ($\overline{\text{BMS}}$) Disable

The ADSP-21mod970 also lets you boot the processor from one external memory space while using a different external memory space for BDMA transfers during normal operation. You can use the $\overline{\text{CMS}}$ to select the first external memory space for BDMA transfers and $\overline{\text{BMS}}$ to select the second external memory space for booting. The $\overline{\text{BMS}}$ signal can be disabled by setting Bit 3 of the System Control Register to 1. The System Control Register is illustrated in Figure 9.

Bus Request and Bus Grant

Each modem processor in the ADSP-21mod970 can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the bus request ($\overline{\text{BR}}$) signal. If the modem processor is not performing an external memory access, then it responds to the active $\overline{\text{BR}}$ input in the following processor cycle by:

- Three-stating the data and address buses and the $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{CMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$ output drivers,
- Asserting the bus grant ($\overline{\text{BG}}$) signal, and
- Halting program execution.

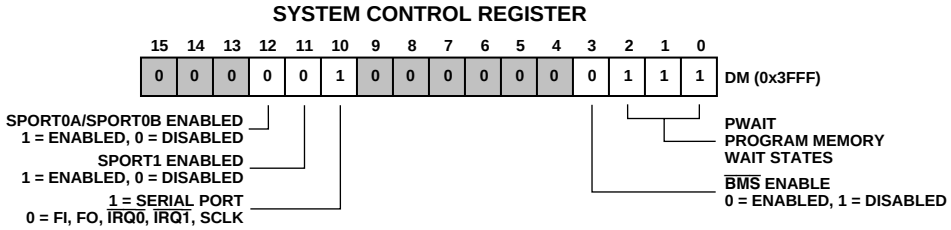


Figure 9. System Control Register

If Go Mode is enabled, the modem processor will not halt program execution until it encounters an instruction that requires an external memory access.

If a modem processor is performing an external memory access when an external device asserts the $\overline{BR}$ signal, it will not three-state the memory interfaces or assert the $\overline{BG}$ signal until the processor cycle after the access completes. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, reenables the output drivers and continues program execution from the point where it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

The $\overline{BGH}$ pin is asserted when a modem processor is ready to execute an instruction, but is stopped because the external bus is already granted to another device. The other device can release the bus by deasserting bus request. Once the bus is released, the modem processor deasserts $\overline{BG}$ and $\overline{BGH}$ and executes the external memory access.

When the ADSP-21mod970 is powered up, all the modem processors must relinquish bus control, and only one processor at a time may control the bus.

Flag I/O Pins

Each modem processor has eight general purpose programmable input/output flag pins. They are controlled by two memory mapped registers. The PFTYPE register determines the direction, 1 = output and 0 = input. The PFDATA register is used to read and write the values on the pins. Data being read from a pin configured as an input is synchronized to the ADSP-21mod970's clock. Bits that are programmed as outputs will read the value being output. The PF pins default to input during reset.

In addition to the programmable flags, each modem processor has three fixed-mode output flags, FL0, FL1, and FL2.

Note: Pins PF0, PF1, PF2 and PF3 are also used for device configuration during reset.

DESIGNING AN EZ-ICE-COMPATIBLE SYSTEM

The ADSP-21mod970 has on-chip emulation support and an ICE-Port, a special set of pins that interface to the EZ-ICE. These features allow in-circuit emulation without replacing the target system processor by using only a 14-pin connection from the target system to the EZ-ICE. Target systems must have a 14-pin connector to accept the EZ-ICE's in-circuit probe, a 14-pin plug.

The EZ-ICE can emulate only one modem processor at a time. You must include hardware to select which processor in the ADSP-21mod970 you want to emulate. Figure 10 is a functional representation of the modem processor selection hardware. You can use one ICE-Port connector with two ADSP-21mod970 processors without using additional buffers.

Issuing the "chip reset" command during emulation causes the modem processor to perform a full chip reset, including a reset of its memory mode. Therefore, it is vital that the mode pins are set correctly PRIOR to issuing a chip reset command from the emulator user interface. As the mode pins share functionality with PF0:3 on the ADSP-21mod970, it may be necessary to reset the target hardware separately to insure the proper mode selection state on emulator chip reset. See the *ADSP-2100 Family EZ-Tools data sheet* for complete information on ICE products.

The ICE-Port interface consists of the following ADSP-21mod970 pins:

$\overline{EBR}$	$\overline{EMS}$	ELIN
$\overline{EBG}$	$\overline{EINT}$	ELOUT
$\overline{ERESET}$	ECLK	EE

These ADSP-21mod970 pins must be connected only to the EZ-ICE connector in the target system. These pins have no function except during emulation, and do not require pull-up or pull-down resistors. The traces for these signals between the ADSP-21mod970 and the connector must be kept as short as possible, no longer that 3 inches.

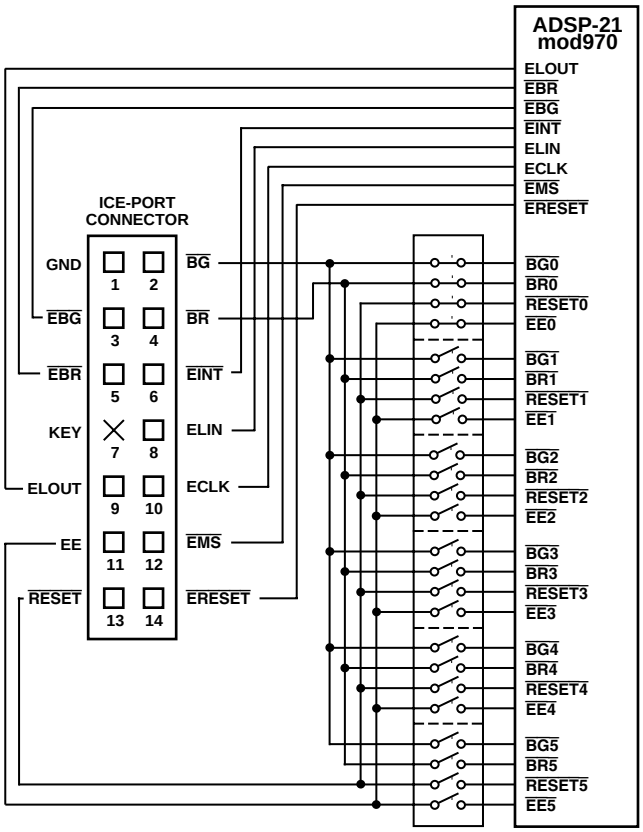


Figure 10. Selecting a Modem Processor in the ADSP-21mod970

The following pins are also used by the EZ-ICE:

$\overline{BR}$	$\overline{BG}$	$\overline{RESET}$	GND

The EZ-ICE uses the EE (emulator enable) signal to take control of the ADSP-21mod970 in the target system. This causes the processor to use its $\overline{ERESET}$, $\overline{EBR}$ and $\overline{EBG}$ pins instead of the $\overline{RESET}$, $\overline{BR}$ and $\overline{BG}$ pins. The $\overline{BG}$ output is three-stated. These signals do not need to be jumper-isolated in a system.

The EZ-ICE connects to target system via a ribbon cable and a 14-pin female plug. The female plug is plugged onto the 14-pin connector (a pin strip header) on the target board.

Target Board Connector for EZ-ICE Probe
The EZ-ICE connector (a standard pin strip header) is shown in Figure 11. This connector must be added to the target board design if the EZ-ICE is to be used. Be sure to allow enough room in the system to fit the EZ-ICE probe onto the 14-pin connector.

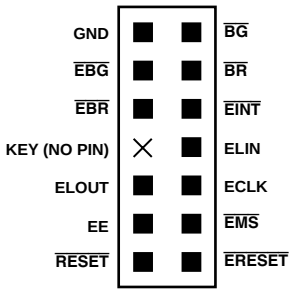


Figure 11. Target Board Connector for EZ-ICE

The 14-pin, 2-row pin strip header is keyed at the Pin 7 location—you must remove Pin 7 from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. The pin strip header must have at least 0.15 inch clearance on all sides to accept the EZ-ICE probe plug.

Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec.

Target Memory Interface
For your target system to be compatible with the EZ-ICE emulator, it must comply with the memory interface guidelines listed below.

PM, DM, BM, IOM, and CM
Design the Program Memory (PM), Data Memory (DM), Byte Memory (BM), I/O Memory (IOM) and Composite Memory (CM) external interfaces to comply with worst case device timing requirements and switching characteristics as specified in this data sheet. The performance of the EZ-ICE may approach published worst case specification for some memory access timing requirements and switching characteristics.

Note: If your target does not meet the worst case chip specification for memory access parameters, you may not be able to emulate your circuitry at the desired CLKIN frequency. Depending on the severity of the specification violation, you may have trouble manufacturing your system as processor components statistically vary in switching characteristic and timing requirements within published limits.

Restriction: All memory strobe signals on the ADSP-21mod970 ($\overline{RD}$, $\overline{WR}$, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, and $\overline{IOMS}$) used in your target system must have 10 kΩ pull-up resistors connected when the EZ-ICE is being used. The pull-up resistors are necessary because there are no internal pull-ups to guarantee their state during prolonged three-state conditions resulting from typical EZ-ICE debugging sessions. These resistors may be removed at your option when the EZ-ICE is not being used.

Target System Interface Signals
When the EZ-ICE board is installed, the performance on some system signals changes. Design your system to be compatible with the following system interface signal changes introduced by the EZ-ICE board:

- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the processor on the $\overline{RESET}$ signal.
- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the processor on the $\overline{BR}$ signal.
- EZ-ICE emulation ignores $\overline{RESET}$ and $\overline{BR}$ when single-stepping.
- EZ-ICE emulation ignores $\overline{RESET}$ and $\overline{BR}$ when in Emulator Space (processor halted).
- EZ-ICE emulation ignores the state of target $\overline{BR}$ in certain modes. As a result, the target system may take control of the processor's external memory bus only if bus grant ($\overline{BG}$) is asserted by the EZ-ICE board's processor.

ADSP-21mod970–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	K Grade Min	K Grade Max	Unit
V_{DD}	3.15	3.45	V
T_{AMB}	0	+70	°C

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	K/B Grades Min	Typ	Max	Unit
V_{IH}	Hi-Level Input Voltage[1, 2]	@ V_{DD} = max	2.0			V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DD} = max	2.2			V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min			0.8	V
V_{OH}	Hi-Level Output Voltage[1, 4, 5]	@ V_{DD} = min				
		I_{OH} = –0.5 mA	2.4			V
		@ V_{DD} = min				
		I_{OH} = –100 µA[6]	V_{DD} – 0.3			V
V_{OL}	Lo-Level Output Voltage[1, 4, 5]	@ V_{DD} = min				
		I_{OL} = 2 mA			0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DD} = max				
		V_{IN} = V_{DD} max			10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DD} = max				
		V_{IN} = 0 V			10	µA
I_{OZH}	Three-State Leakage Current[7]	@ V_{DD} = max				
		V_{IN} = V_{DD} max[8]			10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DD} = max				
		V_{IN} = 0 V[8]			10	µA
I_{DD}	Supply Current (Idle)[9]	@ V_{DD} = 3.3				µA
		t_{CK} = 19 ns[10]		62		mA
		t_{CK} = 25 ns[10]		53		mA
		t_{CK} = 30 ns[10]		47		mA
I_{DD}	Supply Current (Dynamic)[11]	@ V_{DD} = 3.3				
		T_{AMB} = +25°C				
		t_{CK} = 19 ns[10]		387		mA
		t_{CK} = 25 ns[10]		299		mA
		t_{CK} = 30 ns[10]		253		mA
C_I	Input Pin Capacitance[6]	@ V_{IN} = 2.5 V,				
		f_{IN} = 1.0 MHz,			40	pF
C_O	Output Pin Capacitance[6, 7, 12]	T_{AMB} = +25°C				
		@ V_{IN} = 2.5 V,				
		f_{IN} = 1.0 MHz,				
		T_{AMB} = +25°C			40	pF

NOTES

[1] Bidirectional pins: D0-D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7.

[2] Input only pins: $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[3] Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[4] Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, $\overline{\text{BGH}}$.

[5] Although specified for TTL outputs, all ADSP-21mod970 outputs are CMOS-compatible and will drive to V_{DD} and GND, assuming no dc loads.

[6] Guaranteed but not tested.

[7] Three-statable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1.

[8] 0 V on $\overline{\text{BR}}$.

[9] Idle refers to ADSP-21mod970 state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.

[10] V_{IN} = 0 V and 3 V. For typical figures for supply currents, refer to Power Dissipation section.

[11] I_{DD} measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunction (types 1, 4, 5, 12, 13, 14), 30% are type 2 and type 6, and 20% are idle instructions.

[12] Output pin capacitance is the capacitive load for any three-stated output pin.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +4.6 V
Input Voltage . . . . . –0.5 V to V_{DD} + 0.5 V
Output Voltage Swing . . . . . –0.5 V to V_{DD} + 0.5 V
Storage Temperature Range . . . . . –65°C to +150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TIMING PARAMETERS

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

MEMORY TIMING SPECIFICATIONS

Table VI shows common memory device specifications and the corresponding ADSP-21mod970 timing parameter.

Table VI. Memory Devices and Timing Parameters

Memory Device Specification	ADSP-21mod970 Timing Parameter	Timing Parameter Definition
Address Setup to Write Start	t_{ASW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Low
Address Setup to Write End	t_{AW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Deasserted
Address Hold Time	t_{WRA}	A0–A13, $\overline{xMS}$ Hold before $\overline{WR}$ Low
Data Setup Time	t_{DW}	Data Setup before $\overline{WR}$ High
Data Hold Time	t_{DH}	Data Hold after $\overline{WR}$ High
$\overline{OE}$ to Data Valid	t_{RDD}	$\overline{RD}$ Low to Data Valid
Address Access Time	t_{AA}	A0–A13, $\overline{xMS}$ to Data Valid

Note: $\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, $\overline{IOMS}$.

FREQUENCY DEPENDENCY FOR TIMING SPECIFICATIONS

t_{CK} is defined as 0.5 t_{CKI}. The ADSP-21mod970 uses an input clock with a frequency equal to half the instruction rate: a 26.32 MHz input clock (which is equivalent to 38.0 ns) yields a 19 ns processor cycle (equivalent to 52 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain the specification value.

Example: t_{CKH} = 0.5 t_{CK} – 7 ns = 0.5 (19 ns) – 7 ns = 2.5 ns

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

T_{AMB} = $T_J - (PD \times \theta_{JA})$
T_J = Junction Temperature in °C
PD = Power Dissipation in W
θ_{JA} = Thermal Resistance (Junction-to-Ambient)

Package	θ_{JA}
PBGA	26.9°C/W

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-21mod970 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

POWER DISSIPATION

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

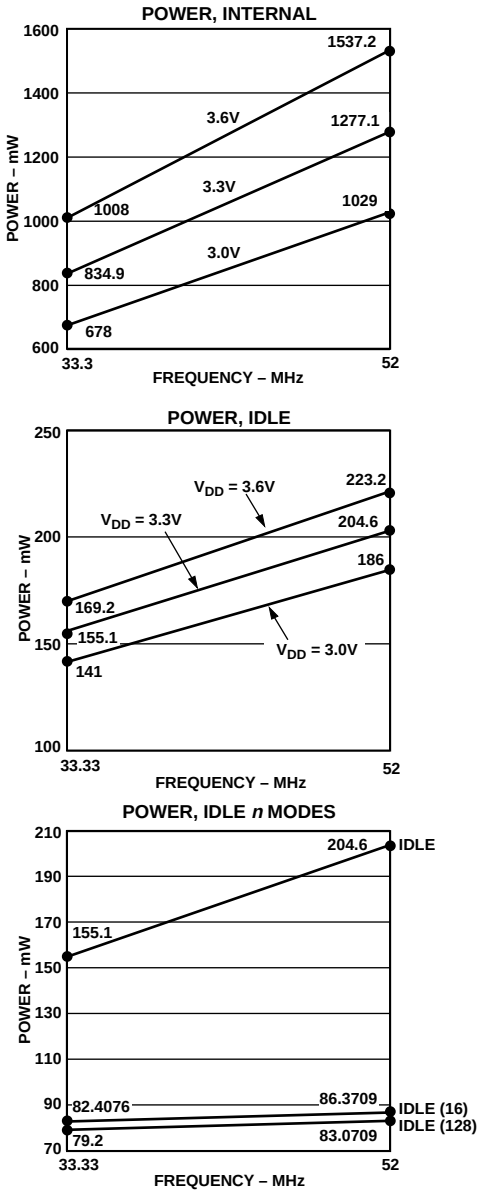


Figure 12. Power vs. Frequency

CAPACITIVE LOADING

Figures 13 and 14 show the capacitive loading characteristics of the ADSP-21mod970.

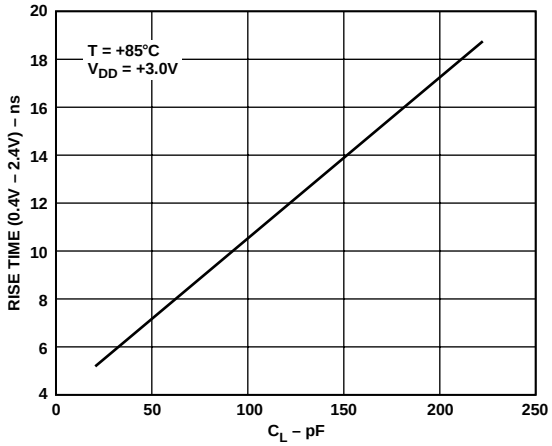


Figure 13. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

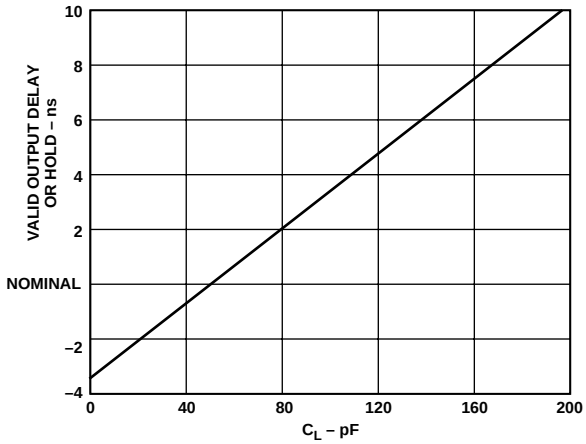


Figure 14. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference between $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 15. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5\ V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

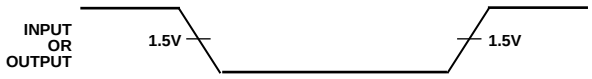


Figure 15. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 16. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

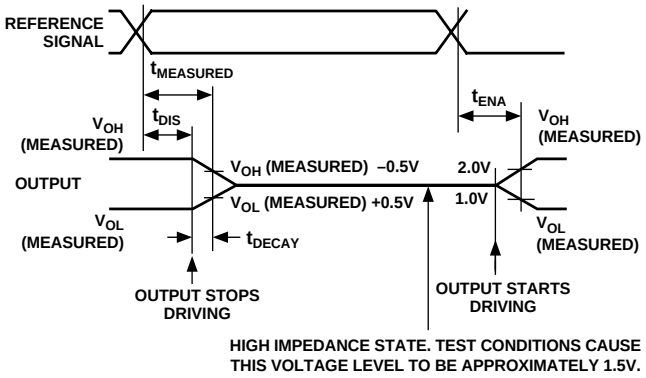


Figure 16. Output Enable/Disable

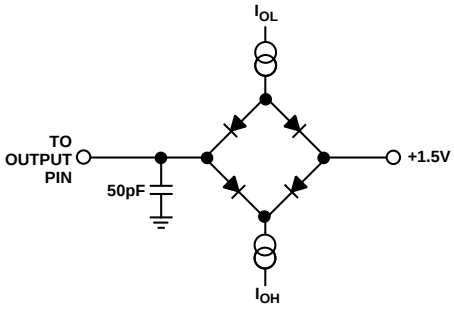


Figure 17. Equivalent Device Loading for AC Measurements (Including All Fixtures)

TIMING PARAMETERS

Parameter		Min	Max	Unit
Clock Signals and Reset				
Timing Requirements:				
t_{CKI}	CLKIN Period	38	100	ns
t_{CKIL}	CLKIN Width Low	15		ns
t_{CKIH}	CLKIN Width High	15		ns
Switching Characteristics:				
t_{CKL}	CLKOUT Width Low	0.5 t_{CK} – 7		ns
t_{CKH}	CLKOUT Width High	0.5 t_{CK} – 7		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	ns
Control Signals				
Timing Requirements:				
t_{RSP}	$\overline{\text{RESET}}$ Width Low	5 t_{CK}[1]		ns
t_{MS}	Mode Setup before $\overline{\text{RESET}}$ High	2		ns
t_{MH}	Mode Setup after $\overline{\text{RESET}}$ High	5		ns

NOTE
[1]Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles assuming stable CLKIN (not including crystal oscillator start-up time).

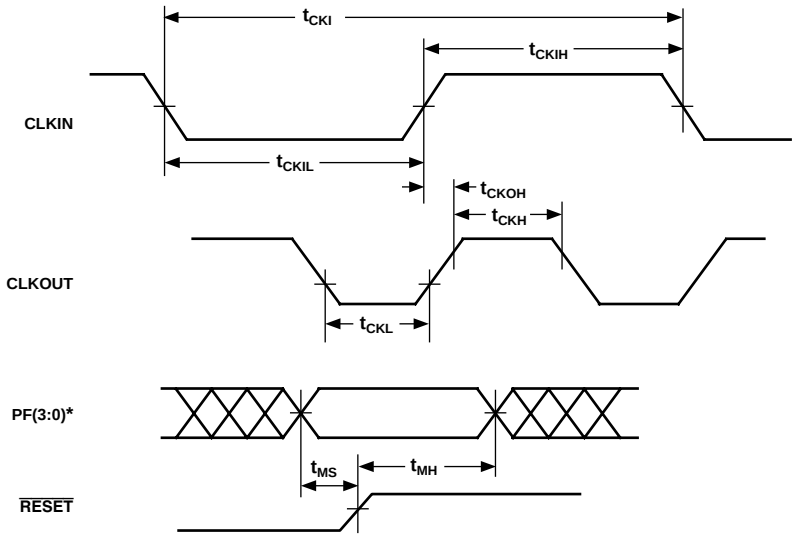


Figure 18. Clock Signals

Parameter		Min	Max	Unit
Interrupts and Flags				
Timing Requirements:				
t_{IFS}	$\overline{IRQx}$, FI, or PFx Setup before CLKOUT Low[1, 2, 3, 4]	0.25 t_{CK} + 15		ns
t_{IFH}	$\overline{IRQx}$, FI, or PFx Hold after CLKOUT High[1, 2, 3, 4]	0.25 t_{CK}		ns
Switching Characteristics:				
t_{FOH}	Flag Output Hold after CLKOUT Low[5]	0.25 t_{CK} – 7		ns
t_{FOD}	Flag Output Delay from CLKOUT Low[5]		0.5 t_{CK} + 6	ns

NOTES
[1]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to Interrupt Controller Operation in the Program Control chapter of the *ADSP-2100 Family User's Manual, Third Edition,* for further information on interrupt servicing.)
[2]Edge-sensitive interrupts require pulsewidths greater than 10 ns; level-sensitive interrupts must be held low until serviced.
[3]$\overline{IRQx}$ = $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$, $\overline{IRQE}$.
[4]PFx = PF0, PF1, PF2, PF3, PF4, PF5, PF6, PF7.
[5]Flag outputs = PFx, FL0, FL1, FL2, Flag_out.

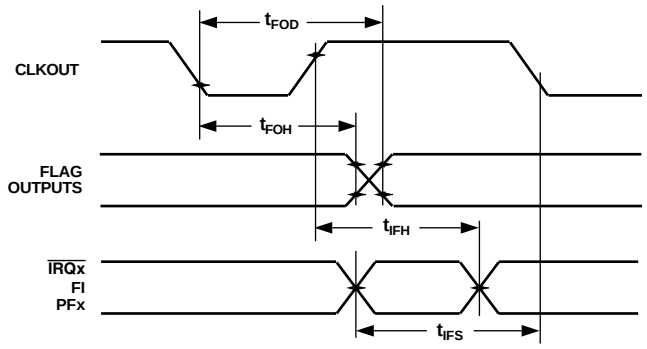


Figure 19. Interrupts and Flags

TIMING PARAMETERS

Parameter		Min	Max	Unit
Bus Request–Bus Grant				
Timing Requirements:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	0.25 t_{CK} + 2		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	0.25 t_{CK} + 17		ns
Switching Characteristics:				
t_{SD}	CLKOUT High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable		0.25 t_{CK} + 10	ns
t_{SDB}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	0.25 t_{CK} – 4		ns
t_{SDBH}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low[2]	0		ns
t_{SEH}	$\overline{BGH}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable[2]	0		ns

NOTES
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.
[1]$\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-2100 Family User's Manual, Third Edition,* for $\overline{BR}$/$\overline{BG}$ cycle relationships.
[2]$\overline{BGH}$ is asserted when the bus is granted and the processor requires control of the bus to continue.

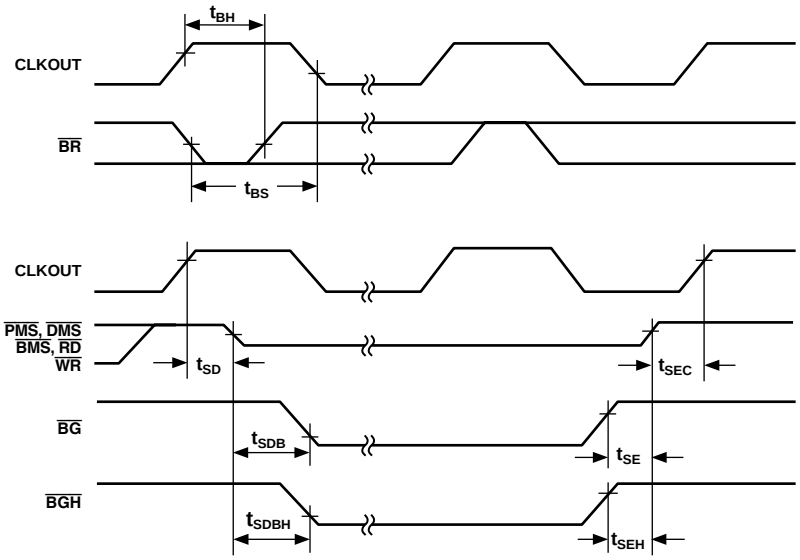


Figure 20. Bus Request–Bus Grant

Parameter		Min	Max	Unit
Memory Read				
Timing Requirements:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		0.5 t_{CK} – 9 + w	ns
t_{AA}	A0–A13, $\overline{xMS}$ to Data Valid		0.75 t_{CK} – 12.5 + w	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristics:				
t_{RP}	$\overline{RD}$ Pulsewidth	0.5 t_{CK} – 5 + w		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	0.25 t_{CK} – 5	0.25 t_{CK} + 7	ns
t_{ASR}	A0–A13, $\overline{xMS}$ Setup before $\overline{RD}$ Low	0.25 t_{CK} – 6		ns
t_{RDA}	A0–A13, $\overline{xMS}$ Hold after $\overline{RD}$ Deasserted	0.25 t_{CK} – 3		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	0.5 t_{CK} – 5		ns

w = wait states × t_{CK}.
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

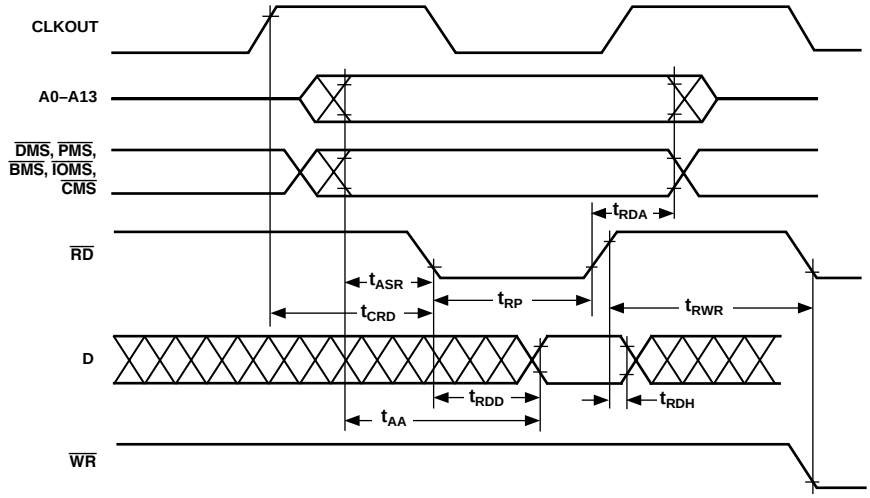


Figure 21. Memory Read

TIMING PARAMETERS

Parameter		Min	Max	Unit
Memory Write				
Switching Characteristics:				
t_{DW}	Data Setup before $\overline{WR}$ High	0.5 t_{CK} – 7 + w		ns
t_{DH}	Data Hold after $\overline{WR}$ High	0.25 t_{CK} – 2		ns
t_{WP}	$\overline{WR}$ Pulsewidth	0.5 t_{CK} – 5 + w		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Low	0.25 t_{CK} – 6		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	0.25 t_{CK} – 7		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	0.25 t_{CK} – 5	0.25 t_{CK} + 7	ns
t_{AW}	A0–A13, $\overline{xMS}$, Setup before $\overline{WR}$ Deasserted	0.75 t_{CK} – 9 + w		ns
t_{WRA}	A0–A13, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted	0.25 t_{CK} – 3		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	0.5 t_{CK} – 5		ns

w = wait states × t_{CK}.
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

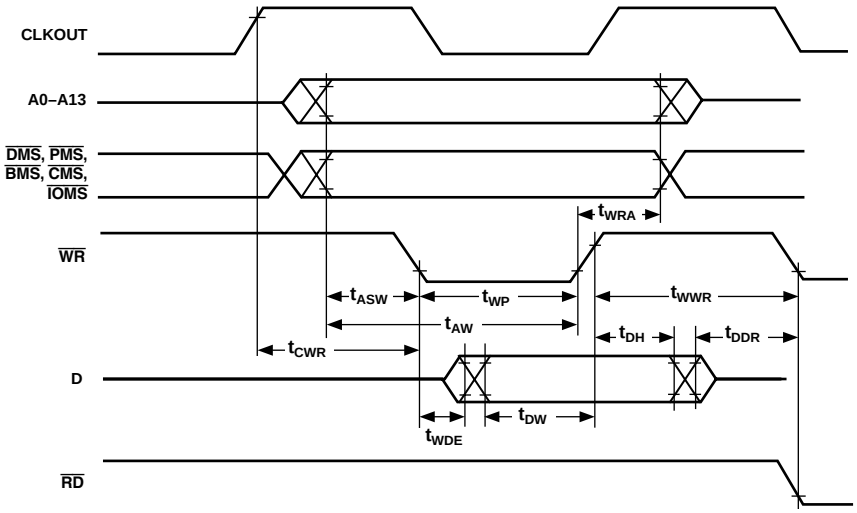


Figure 22. Memory Write

Parameter		Min	Max	Unit
Serial Ports				
Timing Requirements:				
t_{SCK}	SCLK Period	38		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	7		ns
t_{SCP}	$SCLK_{IN}$ Width	15		ns
Switching Characteristics:				
t_{CC}	CLKOUT High to $SCLK_{OUT}$	0.25 t_{CK}	0.25 t_{CK} + 10	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		15	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		15	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS (Alt) to DT Enable	0		ns
t_{TDV}	TFS (Alt) to DT Valid		14	ns
t_{SCDD}	SCLK High to DT Disable		15	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		15	ns

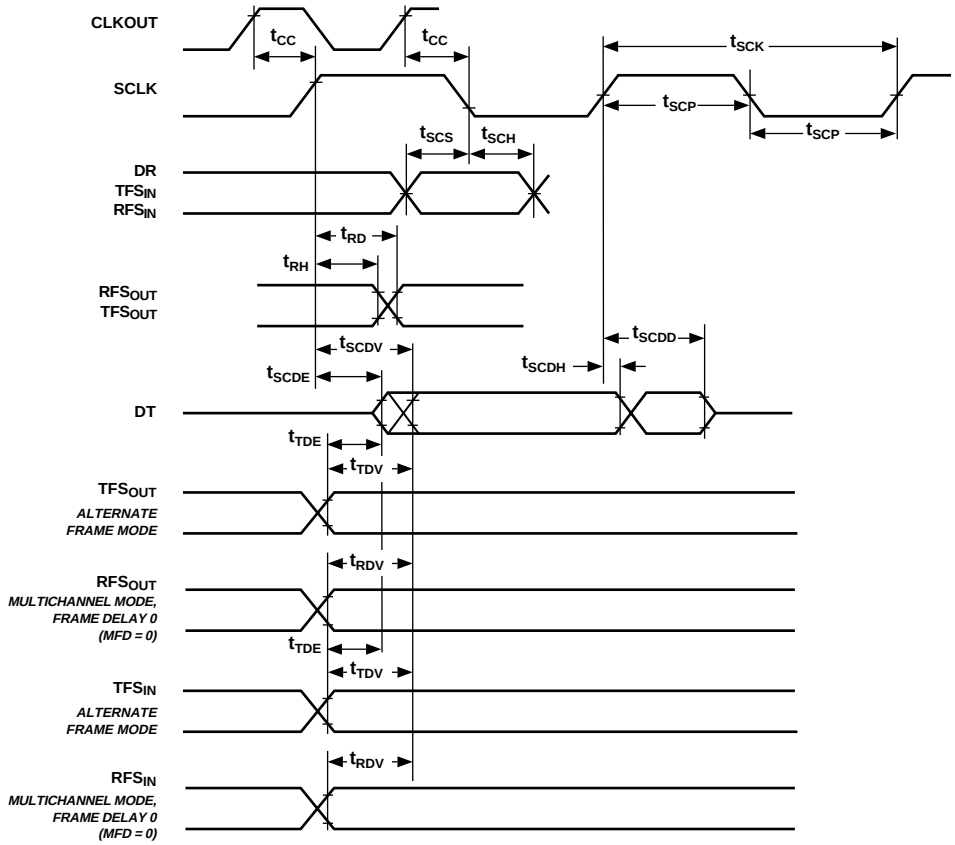


Figure 23. Serial Ports

TIMING PARAMETERS

Parameter		Min	Max	Unit
IDMA Address Latch				
Timing Requirements:				
t_{IALP}	Duration of Address Latch[1, 2]	10		ns
t_{IASU}	IAD15–0 Address Setup before Address Latch End[2]	5		ns
t_{IAH}	IAD15–0 Address Hold after Address Latch End[2]	2		ns
t_{IKA}	$\overline{IACK}$ Low before Start of Address Latch[2, 3]	0		ns
t_{IALS}	Start of Write or Read after Address Latch End[1, 2]	3		ns
t_{IALD}	Address Latch Start after Address Latch End[1, 2]	2		ns

NOTES
[1]Start of Address Latch = $\overline{IS}$ Low and IAL High.
[2]End of Address Latch = $\overline{IS}$ High or IAL Low.
[3]Start of Write or Read = $\overline{IS}$ Low and $\overline{IWR}$ Low or $\overline{IRD}$ Low.

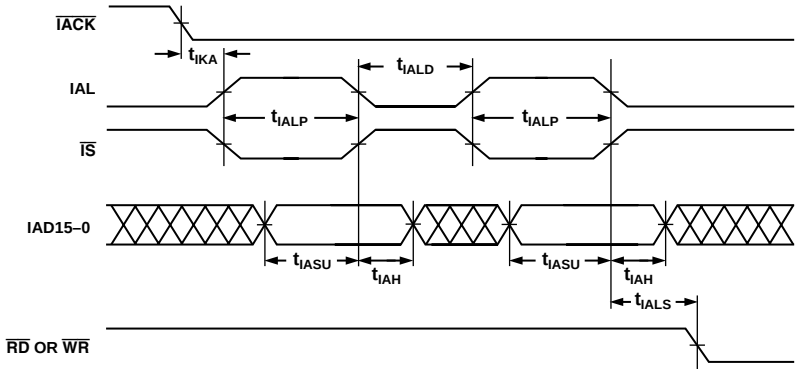


Figure 24. IDMA Address Latch

Parameter		Min	Max	Unit
IDMA Write, Short Write Cycle				
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low before Start of Write[1]	0		ns
t_{IWP}	Duration of Write[1, 2]	15		ns
t_{IDSU}	IAD15–0 Data Setup before End of Write[2, 3, 4]	5		ns
t_{IDH}	IAD15–0 Data Hold after End of Write[2, 3, 4]	2		ns
Switching Characteristic:				
t_{IKHW}	Start of Write to $\overline{IACK}$ High	4	15	ns

NOTES
[1]Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2]End of Write = $\overline{IS}$ High or $\overline{IWR}$ High.
[3]If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[4]If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.

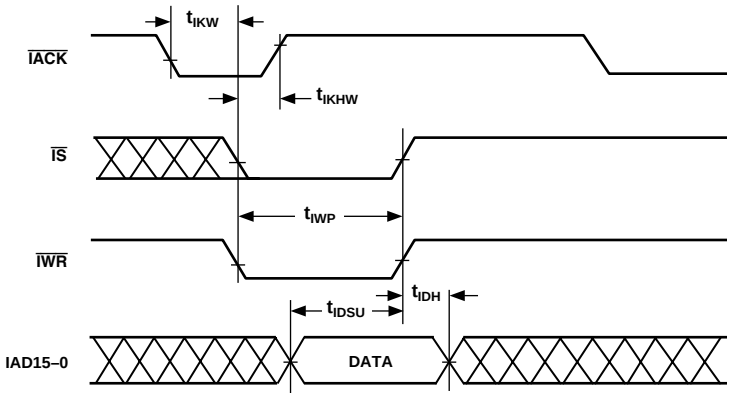


Figure 25. IDMA Write, Short Write Cycle

TIMING PARAMETERS

Parameter		Min	Max	Unit
IDMA Write, Long Write Cycle				
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low before Start of Write[1]	0		ns
t_{IKSU}	IAD15–0 Data Setup before $\overline{IACK}$ Low[2, 3, 4]	0.5 t_{CK} + 10		ns
t_{IKH}	IAD15–0 Data Hold after $\overline{IACK}$ Low[2, 3, 4]	2		ns
Switching Characteristics:				
t_{IKLW}	Start of Write to $\overline{IACK}$ Low[4]	1.5 t_{CK}		ns
t_{IKHW}	Start of Write to $\overline{IACK}$ High	4	15	ns

NOTES
[1]Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2]If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[3]If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.
[4]This is the earliest time for $\overline{IACK}$ Low from Start of Write. For IDMA Write cycle relationships, please refer to the *ADSP-2100 Family User's Manual, Third Edition*.

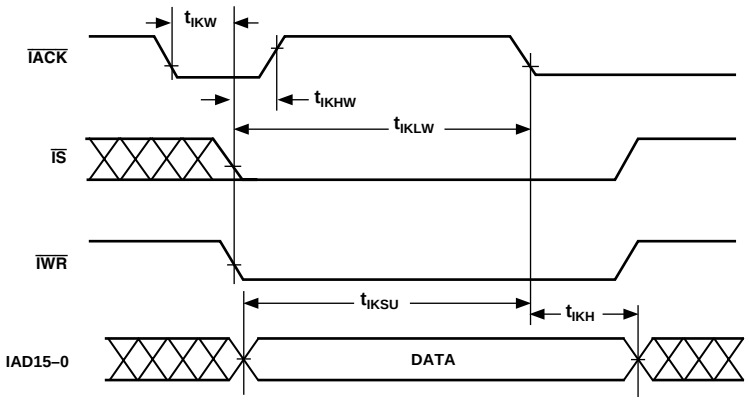


Figure 26. IDMA Write, Long Write Cycle

Parameter		Min	Max	Unit
IDMA Read, Long Read Cycle				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[1]	0		ns
t_{IRK}	End of Read after $\overline{IACK}$ Low[2]	2		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[1]	4	15	ns
t_{IKDS}	IAD15–0 Data Setup before $\overline{IACK}$ Low	0.5 t_{CK} – 7		ns
t_{IKDH}	IAD15–0 Data Hold after End of Read[2]	0		ns
t_{IKDD}	IAD15–0 Data Disabled after End of Read[2]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		10	ns
t_{IRDH1}	IAD15–0 Previous Data Hold after Start of Read (DM/PM1)[3]	2 t_{CK} – 5		ns
t_{IRDH2}	IAD15–0 Previous Data Hold after Start of Read (PM2)[4]	t_{CK} – 5		ns

NOTES
[1]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[2]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.
[3]DM read or first half of PM read.
[4]Second half of PM read.

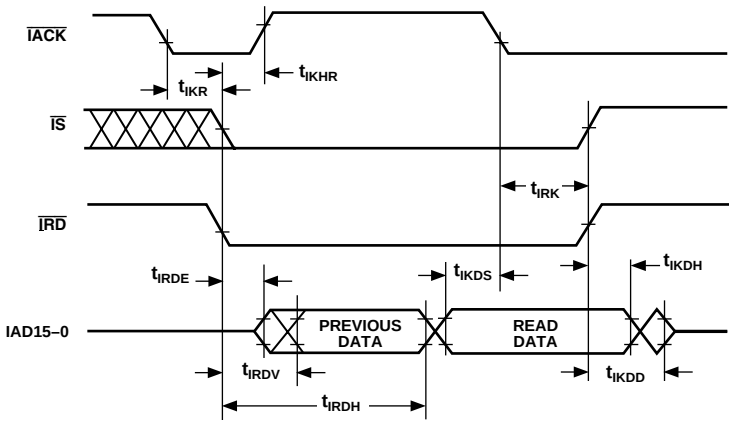


Figure 27. IDMA Read, Long Read Cycle

TIMING PARAMETERS

Parameter		Min	Max	Unit
IDMA Read, Short Read Cycle				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[1]	0		ns
t_{IRP}	Duration of Read	15		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[1]	4	15	ns
t_{IKDH}	IAD15–0 Data Hold after End of Read[2]	0		ns
t_{IKDD}	IAD15–0 Data Disabled after End of Read[2]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		10	ns

NOTES
[1]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[2]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

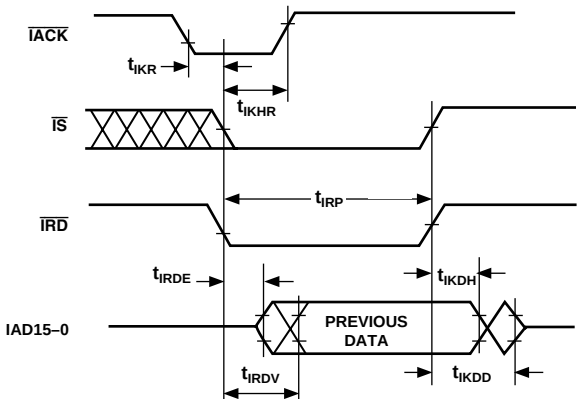


Figure 28. IDMA Read, Short Read Cycle

304-Ball PBGA Package Pinout

The ADSP-21mod970 package pinout is shown in the table below.

Ball Number	Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number	Signal Name
A1	GND	B23	IAD1	D22	IAD4	K4	$\overline{\text{CMS\_1}}$
A2	PF0_1	C1	IAD5_1	D23	IAD3	K20	PF5_3
A3	PF2_1	C2	IAD0_1	E1	IAD8_1	K21	$\overline{\text{EBG}}$
A4	FL1_1	C3	GND	E2	IAD7_1	K22	$\overline{\text{EBR}}$
A5	D23_1	C4	$\overline{\text{BGH\_1}}$	E3	IAD2_1	K23	$\overline{\text{EINT}}$
A6	D21_1	C5	PF3_1	E4	IAD1_1	L1	D17
A7	D13_1	C6	FL2_1	E20	CLKIN	L2	D18
A8	D16_1	C7	D12_1	E21	GND	L3	PF5_1
A9	GND	C8	D17_1	E22	GND	L4	PF7_1
A10	PF0_2	C9	GND	E23	GND	L20	V_{DD}
A11	PF1_2	C10	IAD13_1	F1	IAD12_1	L21	$\overline{\text{ERESET}}$
A12	FL0_2	C11	IAD15_1	F2	IAD9_1	L22	ELIN
A13	FL1_2	C12	PF2_2	F3	IAD10_1	L23	ELOUT
A14	V_{DD}	C13	V_{DD}	F4	$\overline{\text{IWR\_1}}$	M1	D15
A15	V_{DD}	C14	V_{DD}	F20	GND	M2	D16
A16	PF0_3	C15	V_{DD}	F21	GND	M3	PF6_1
A17	PF1_3	C16	IS_2	F22	GND	M4	$\overline{\text{BGH\_4}}$
A18	FL0_3	C17	CLKOUT_2	F23	GND	M20	V_{DD}
A19	FL1_3	C18	PF4_2	G1	CLKIN_1	M21	V_{DD}
A20	D21	C19	DT1_2	G2	IAD11_1	M22	V_{DD}
A21	D22	C20	EE_2	G3	D8_1	M23	V_{DD}
A22	D23	C21	GND	G4	$\overline{\text{IRD\_1}}$	N1	D13
A23	GND	C22	IAD2	G20	$\overline{\text{IAL}}$	N2	D12
B1	IAD3_1	C23	IAD0	G21	$\overline{\text{IRD}}$	N3	D14
B2	GND	D1	IAD6_1	G22	$\overline{\text{IWR}}$	N4	PF1_4
B3	PF1_1	D2	IAD4_1	G23	GND	N20	V_{DD}
B4	FL0_1	D3	A0_1	H1	$\overline{\text{RD\_1}}$	N21	PF6_3
B5	D22_1	D4	GND	H2	$\overline{\text{WR\_1}}$	N22	ECLK
B6	D20_1	D5	D10_1	H3	$\overline{\text{IAL\_1}}$	N23	$\overline{\text{EMS}}$
B7	D19_1	D6	D11_1	H4	$\overline{\text{IS\_1}}$	P1	GND
B8	D15_1	D7	D9_1	H20	CLKOUT_3	P2	GND
B9	GND	D8	D18_1	H21	RFS0A	P3	GND
B10	D14_1	D9	GND	H22	DR0A	P4	TFS0_1
B11	$\overline{\text{BGH\_2}}$	D10	IAD14_1	H23	$\overline{\text{IS\_3}}$	P20	DT1_3
B12	PF3_2	D11	$\overline{\text{BR\_1}}$	J1	$\overline{\text{DMS\_1}}$	P21	PF2_6
B13	FL2_2	D12	$\overline{\text{BG\_1}}$	J2	$\overline{\text{BMS\_1}}$	P22	$\overline{\text{RESET\_3}}$
B14	V_{DD}	D13	$\overline{\text{IACK\_1}}$	J3	$\overline{\text{PMS\_1}}$	P23	EE_3
B15	V_{DD}	D14	V_{DD}	J4	CLKOUT_1	R1	IAD6
B16	$\overline{\text{BGH\_3}}$	D15	V_{DD}	J20	SCLK0A	R2	IAD7
B17	PF2_3	D16	$\overline{\text{BG\_2}}$	J21	PF4_3	R3	IAD5
B18	PF3_3	D17	$\overline{\text{BR\_2}}$	J22	$\overline{\text{BG\_3}}$	R4	PF0_4
B19	FL2_3	D18	PF5_2	J23	$\overline{\text{BR\_3}}$	R20	PF0_6
B20	D20	D19	$\overline{\text{RESET\_2}}$	K1	D19	R21	PF1_6
B21	DT0A	D20	GND	K2	PF4_1	R22	FL2_6
B22	GND	D21	GND	K3	$\overline{\text{IOMS\_1}}$	R23	FL1_6

304-Ball PBGA Package Pinout (continued)

Ball Number	Signal Name	Ball Number	Signal Name	Ball Number	Signal Name	Ball Number	Signal Name
T1	D10	W23	GND	AA8	PF4_5	AB16	PF2_5
T2	D9	Y1	V_{DD}	AA9	GND	AB17	CLKOUT_6
T3	D11	Y2	V_{DD}	AA10	PF6_5	AB18	RFS0B
T4	EE_1	Y3	V_{DD}	AA11	V_{DD}	AB19	GND
T20	$\overline{\text{BGH\_6}}$	Y4	GND	AA12	DT1_5	AB20	SCLK0B
T21	TFS0_3	Y5	FL0_4	AA13	$\overline{\text{BGH\_5}}$	AB21	$\overline{\text{RESET\_6}}$
T22	PF3_6	Y6	V_{DD}	AA14	PF7_2	AB22	GND
T23	FL0_6	Y7	FL2_4	AA15	PF1_5	AB23	$\overline{\text{BG\_6}}$
U1	IAD9	Y8	CLKOUT_5	AA16	FL1_5	AC1	GND
U2	IAD11	Y9	GND	AA17	TFS1	AC2	$\overline{\text{BR\_4}}$
U3	IAD8	Y10	$\overline{\text{IS\_5}}$	AA18	DR1	AC3	PF7_4
U4	PF2_4	Y11	V_{DD}	AA19	GND	AC4	GND
U20	GND	Y12	TFS0_2	AA20	DT1_6	AC5	TFS0_4
U21	GND	Y13	PF6_2	AA21	GND	AC6	V_{DD}
U22	GND	Y14	PF0_5	AA22	$\overline{\text{BG\_5}}$	AC7	V_{DD}
U23	GND	Y15	FL0_5	AA23	IAD14	AC8	GND
V1	IAD10	Y16	FL2_5	AB1	PF5_4	AC9	GND
V2	IAD12	Y17	RFS1	AB2	GND	AC10	TFS0_5
V3	DT1_1	Y18	SCLK1	AB3	PF6_4	AC11	V_{DD}
V4	PF3_4	Y19	GND	AB4	GND	AC12	EE_5
V20	GND	Y20	GND	AB5	DT1_4	AC13	PF5_6
V21	GND	Y21	$\overline{\text{BR\_5}}$	AB6	V_{DD}	AC14	GND
V22	GND	Y22	IAD13	AB7	$\overline{\text{RESET\_4}}$	AC15	PF6_6
V23	GND	Y23	$\overline{\text{IACK}}$	AB8	PF5_5	AC16	PF7_6
W1	D8	AA1	PF4_4	AB9	GND	AC17	DT0B
W2	CLKOUT_4	AA2	$\overline{\text{BG\_4}}$	AB10	PF7_5	AC18	TFS0_6
W3	$\overline{\text{RESET\_1}}$	AA3	GND	AB11	V_{DD}	AC19	GND
W4	$\overline{\text{IS\_4}}$	AA4	GND	AB12	$\overline{\text{RESET\_5}}$	AC20	DR0B
W20	$\overline{\text{IS\_6}}$	AA5	FL1_4	AB13	PF4_6	AC21	EE_6
W21	PF7_3	AA6	V_{DD}	AB14	GND	AC22	$\overline{\text{BR\_6}}$
W22	IAD15	AA7	EE_4	AB15	PF3_5	AC23	GND

ORDERING GUIDE

Part Number	Ambient Temperature Range	Processor Clock	Package Description	Package Option
ADSP-21mod970-000	0°C to +70°C	26.0 MHz	304-Ball PBGA	B-304

RELATED DOCUMENTS

ADSP-21mod970-110 Multiport Internet Gateway Processor solution.

PIN ●	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	GND	PF0_1	PF2_1	FL1_1	D23_1	D21_1	D13_1	D16_1	GND	PF0_2	PF1_2	FL0_2	FL1_2	V_{DD}	V_{DD}	PF0_3	PF1_3	FL0_3	FL1_3	D21	D22	D23	GND	A
B	IAD3_1	GND	PF1_1	FL0_1	D22_1	D20_1	D19_1	D15_1	GND	D14_1	$\overline{BGH\_2}$	PF3_2	FL2_2	V_{DD}	V_{DD}	$\overline{BGH\_3}$	PF2_3	PF3_3	FL2_3	D20	DT0A	GND	IAD1	B
C	IAD5_1	IAD0_1	GND	$\overline{BGH\_1}$	PF3_1	FL2_1	D12_1	D17_1	GND	IAD13_1	IAD15_1	PF2_2	V_{DD}	V_{DD}	V_{DD}	IS_2	CLK OUT_2	PF4_2	DT1_2	EE_2	GND	IAD2	IAD0	C
D	IAD6_1	IAD4_1	A0_1	GND	D10_1	D11_1	D9_1	D18_1	GND	1AD14_1	$\overline{BR\_1}$	$\overline{BG\_1}$	$\overline{IACK\_1}$	V_{DD}	V_{DD}	$\overline{BG\_2}$	$\overline{BR\_2}$	PF5_2	$\overline{RESET\_2}$	GND	GND	IAD4	IAD3	D
E	IAD8_1	IAD7_1	IAD2_1	IAD1_1																CLKIN	GND	GND	GND	E
F	IAD12_1	IAD9_1	IAD10_1	$\overline{IWR\_1}$																GND	GND	GND	GND	F
G	CLKIN_1	IAD11_1	D8_1	$\overline{IRD\_1}$																$\overline{IAL}$	$\overline{IRD}$	$\overline{IWR}$	GND	G
H	$\overline{RD\_1}$	$\overline{WR\_1}$	$\overline{IAL\_1}$	$\overline{IS\_1}$																CLK OUT_3	RFS0A	DR0A	$\overline{IS\_3}$	H
J	$\overline{DMS\_1}$	$\overline{BMS\_1}$	$\overline{PMS\_1}$	CLK OUT_1																SCLK0A	PF4_3	$\overline{BG\_3}$	$\overline{BR\_3}$	J
K	D19	PF4_1	$\overline{IOMS\_1}$	$\overline{CMS\_1}$																PF5_3	$\overline{EBG}$	$\overline{EBR}$	$\overline{EINT}$	K
L	D17	D18	PF5_1	PF7_1																V_{DD}	$\overline{ERESET}$	ELIN	ELOUT	L
M	D15	D16	PF6_1	$\overline{BGH\_4}$																V_{DD}	V_{DD}	V_{DD}	V_{DD}	M
N	D13	D12	D14	PF1_4																V_{DD}	PF6_3	ECLK	$\overline{EMS}$	N
P	GND	GND	GND	TFS0_1																DT1_3	PF2_6	$\overline{RESET\_3}$	EE_3	P
R	IAD6	IAD7	IAD5	PF0_4																PF0_6	PF1_6	FL2_6	FL1_6	R
T	D10	D9	D11	EE_1																$\overline{BGH\_6}$	TFS0_3	PF3_6	FL0_6	T
U	IAD9	IAD11	IAD8	PF2_4																GND	GND	GND	GND	U
V	IAD10	IAD12	DT1_1	PF3_4																GND	GND	GND	GND	V
W	D8	CLK OUT_4	$\overline{RESET\_1}$	$\overline{IS\_4}$																$\overline{IS\_6}$	PF7_3	IAD15	GND	W
Y	V_{DD}	V_{DD}	V_{DD}	GND	FL0_4	V_{DD}	FL2_4	CLK OUT_5	GND	$\overline{IS\_5}$	V_{DD}	TFS0_2	PF6_2	PF0_5	FL0_5	FL2_5	RFS1	SCLK1	GND	GND	$\overline{BR\_5}$	IAD13	$\overline{IACK}$	Y
AA	PF4_4	$\overline{BG\_4}$	GND	GND	FL1_4	V_{DD}	EE_4	PF4_5	GND	PF6_5	V_{DD}	DT1_5	$\overline{BGH\_5}$	PF7_2	PF1_5	FL1_5	TFS1	DR1	GND	DT1_6	GND	$\overline{BG\_5}$	IAD14	AA
AB	PF5_4	GND	PF6_4	GND	DT1_4	V_{DD}	$\overline{RESET\_4}$	PF5_5	GND	PF7_5	V_{DD}	$\overline{RESET\_5}$	PF4_6	GND	PF3_5	PF2_5	CLK OUT_6	RFS0B	GND	SCLK0B	$\overline{RESET\_6}$	GND	$\overline{BG\_6}$	AB
AC	GND	$\overline{BR\_4}$	PF7_4	GND	TFS0_4	V_{DD}	V_{DD}	GND	GND	TFS0_5	V_{DD}	EE_5	PF5_6	GND	PF6_6	PF7_6	DT0B	TFS0_6	GND	DR0B	EE_6	$\overline{BR\_6}$	GND	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

ADSP-21mod970
(TOP VIEW)

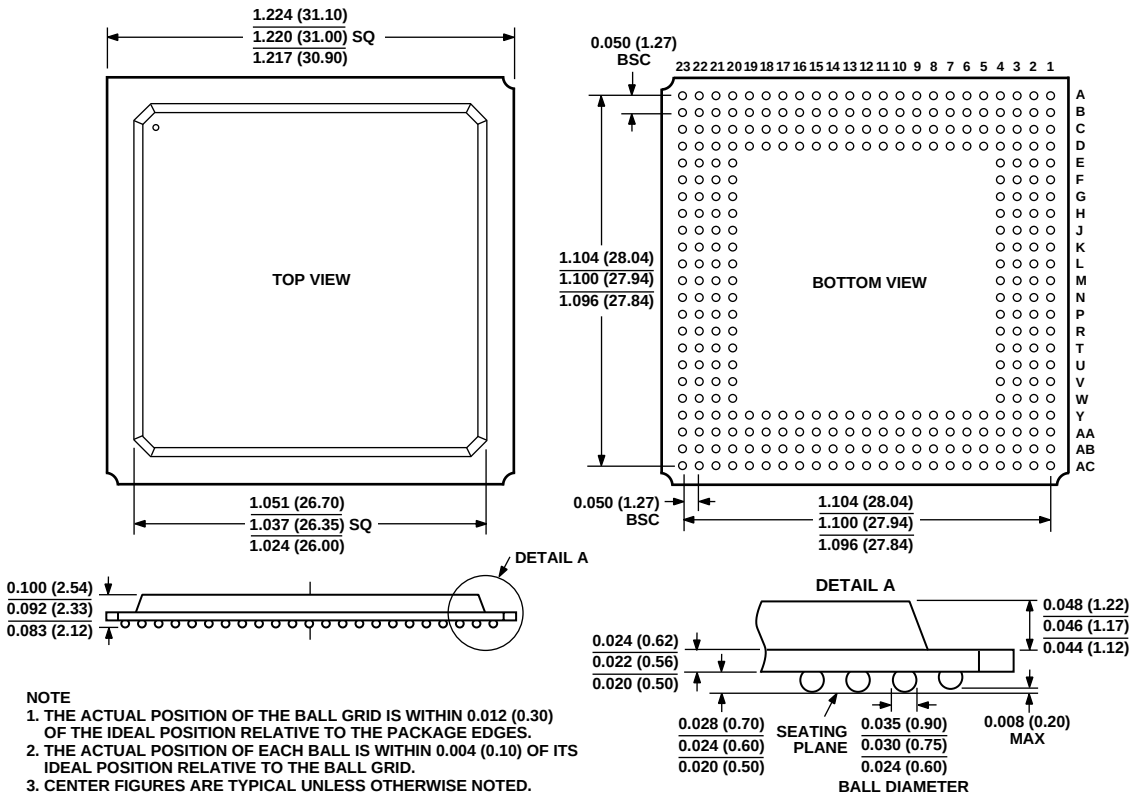
NOTE: THE NUMBER AFTER THE UNDERSCORE IN SIGNAL NAMES CORRESPONDS TO THE MODEM CHANNEL NUMBER IN THE FUNCTIONAL BLOCK DIAGRAM ON PAGE 1. ANY SIGNAL NAME WITHOUT AN UNDERSCORE CORRESPONDS TO SIGNALS BEING SHARED AMONG MODEM CHANNELS NUMBER 2–6.

ADSP-21mod970 Pinout

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

304-Ball Metric Plastic Ball Grid Array
(B-304)



NOTE
1. THE ACTUAL POSITION OF THE BALL GRID IS WITHIN 0.012 (0.30) OF THE IDEAL POSITION RELATIVE TO THE PACKAGE EDGES.
2. THE ACTUAL POSITION OF EACH BALL IS WITHIN 0.004 (0.10) OF ITS IDEAL POSITION RELATIVE TO THE BALL GRID.
3. CENTER FIGURES ARE TYPICAL UNLESS OTHERWISE NOTED.

C3494–2.5–7/99

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