ADSP-218x
16-bit DIGITAL SIGNAL PROCESSORS

Code-Compatible and Pin-Compatible Fixed-Point DSP Family

KEY FEATURES:

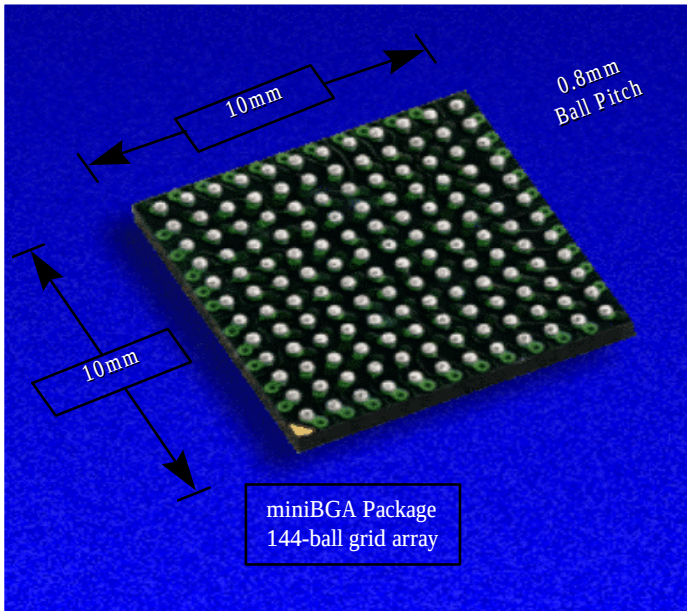
- **Up to 1.5 Mbits of on-chip SRAM (80 K words)**
- **Up to 75 MHz/75 MIPS**
- **As low as .4 mA/MIP at 75 MHz**
- **All instructions execute in a single clock cycle**
- **Easy-to-use algebraic-like assembly language syntax**
- **Binary code-compatible within the ADSP-218x family**
- **Assembly code-compatible with all ADSP-2100 DSPs**
- **Three computational units in parallel operate simultaneously with two data address generators and powerful program sequencer**
- **16-bit-wide internal DMA port**
- **2 serial ports, including multichannel serial port for direct interfacing to T1/E1 lines**
- **Byte DMA transfers of up to 4 Mbytes of stored code or data**

OVERVIEW:

Analog Device's industry-leading DSP and SRAM integration capability is evident in the ADSP-218x Family. Well-known for its leadership in 32-bit DSP and SRAM integration, pioneered by the SHARC family, ADI provides the 16-bit complement in the ADSP-218x family. With up to 1.5 Mbits of on-chip SRAM, many functions run without the need for external memory, vastly simplifying the algorithm development and debug process. In addition to minimizing memory I/O bottlenecks, executing algorithms using on-chip memory reduces chip count, board space, and power consumption. Large amounts of SRAM, coupled with the ADSP-218x family's sophisticated DMA and programming features, make the ADSP-218x processors truly easy-to-use in a variety of applications.

Packaging technology also plays an important role in how easily designers can incorporate these processors into their applications. Advanced miniaturization techniques and pin out standardization can significantly simply the design-in process. The ADSP-2183, for example, is packaged in a tiny 10mm x 10mm Ball quid array (mini BGA). In a one-centimeter square, the design engineer has over 52 MIPS, 32K words of SRAM, and two serial interface ports.

Likewise, ADI's pin-for-pin compatible packaging strategy saves designers time. With little or no change to the hardware,



ADI's mini-BGA package houses the world's smallest DSP, the ADSP-2183. Packaging innovations play a critical role, helping design engineers realize the system-level advantages of ADI's highly-integrated, power-efficient ADSP-218x DSPs.

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designers can migrate to higher speeds, lower voltages, and larger memory sizes.

CODE-COMPATIBLE ARCHITECTURE

Code compatibility is the hallmark of the ADI 16-bit DSP family. The ADSP-218x DSPs continue this tradition, preserving customer investment and bringing along hardware and software development tools from numerous independent partners.

The ADSP-2100 architecture consists of three computational units arranged architecturally in parallel, two independent address generators, and a powerful program sequencer. The computational units provide all mathematical functions for the processor, including single-cycle multiply/accumulates, bit manipulation, and shifting operations. The dual Data Address Generators can provide simultaneous addresses to two memory spaces, allowing the processors to fetch two data values in a single processor cycle. The Program Sequencer provides single-cycle operation for all instructions, low-latency interrupt response, and nested, zero-overhead looping.

MAXIMIZING MEMORY AND I/O BANDWIDTH

With the SRAM available on the ADSP-218x processors, many applications can be implemented without the use of external SRAM. This increases processor efficiency by eliminating any wasted clock cycles caused by the bottlenecks that occur with off-chip memory accesses. Multifunction instructions, enabled by the 24-bit instruction word, and zero-overhead nested looping capabilities combine to produce very efficient algorithm execution.

To maintain data flow to and from the core, the ADSP-218x family incorporates several types of peripheral DMA support. The DSPs can access up to 4 mbytes of stored code or data through Byte DMA (BDMA) transfers. Serial port autobuffering supports memory reads and writes of serial port data. Host processor systems can read or write DSP memory directly through a 16-bit-wide Internal DMA (IDMA) port.

Benchmarks for ADSP-218x DSPs

Modem Algorithm	MIPS	PM	DM	Comments
V.34 Annex 12	23	16K	16K	@ 33.6 Kbps
V.32bis	11.5	7.5K	7K	

Speech Algorithm	O/P Rate	MIPS	PM	DM
G.721	32 Kbps	7.6	628	137
G.728	16 Kbps	28	7.2K	2K
G.729	8 Kbps	21	10.2	5.4K
G.165 (Line Echo)	20 msec span	6	430	225
Acoustic Echo Cancellation	from 64 msec	2.9	720	534
Acoustic Echo Cancellation	up to 384 msec	6.8	1.33K	1.15K

Signal Processing Algorithm	Performance
1024-Point Complex FFT	34K Inst. Clocks
4096-Point Complex FFT	149K Inst. Clocks

The DMA functionality allows for modular system designs with a minimum of external circuitry. For applications where a DSP will be used alone, the BDMA feature allows the ADSP-218x processors to access very large code and data segments without the need for fast, expensive SRAM. Because BDMA transfers happen in the background, the DSP continues uninterrupted, executing programs or accessing data sets. This access can be through the use of low-cost, byte-wide storage media such as EPROM.

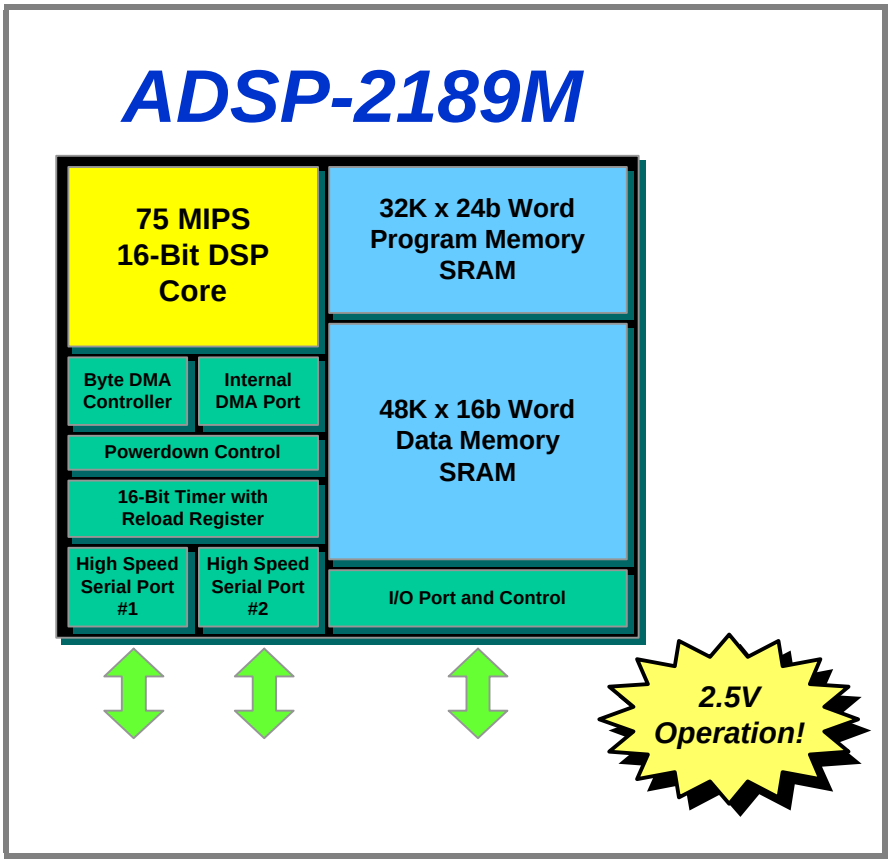
For host-based systems, the IDMA port allows a great deal of system flexibility while keeping chip count low. Since the host has direct write access to both DSP Program Memory and Data Memory, no external memory devices are required for the DSP. The host can boot-load code and data into the DSP, write data variables, and reload, or load additional code if the system requires it.

The multichannel serial port on the ADSP-218x processors allows direct interface to T1 and E1 lines. This built-in time division multiplexing eliminates the complicated code development that would be required to divide the serial data stream into channels, and can support 24-channel and 32-channel frames.

LOW-COST DEVELOPMENT TOOLS

The Analog Devices EZ-KIT Lite Development System is a complete, ultra-low-cost tool for evaluating and prototyping. The kit includes an ADSP-2181-based EZ-LAB® board, assembler, linker, simulator, PROM splitter utility, and demo source code. Evaluation demos range from MPEG audio decode to various speech compression, filtering, and telephony algorithms.

An ADSP-218X EZ-ICE® system provides a productive software and hardware development and integration environment for the ADSP-218x family of products. It features full-speed, in-circuit emulation of the ADSP-218x, connects to the target system via a special Emulator port, supports uploading/downloading of memory from a PC, allows display and modification of memory and registers, single-step execution, and breakpoint execution, and provides a Windows®-based GUI.



The ADSP-2189M integrates more on-chip memory than any 16-bit DSP available. With 1.5 Mbits of on-chip SRAM and a 75 MHz clock frequently, the device consumes only 0.4 mA/MIP.

ADSP-218x DSP Family Selection Guide

Product	Pkg	Program RAM	Data RAM	Serial Ports	Byte DMA	16-Bit Tri-State DMA	MIPS/MHz	Power Efficiency	Vcc
ADSP-2189M	100-TQFP	32K	48K	2	Yes	Yes	75	0.4 mA/MIP	2.5V
	100-TQFP	32K	48K	2	Yes	Yes	66	0.4 mA/MIP	2.5V
ADSP-2187L	100-TQFP	32K	32K	2	Yes	Yes	52	0.8 mA/MIP	3.3V
	100-TQFP	32K	32K	2	Yes	Yes	40	0.8 mA/MIP	3.3V
ADSP-2186L	100-TQFP	8K	8K	2	Yes	Yes	33	1.8 mA/MIP	3.3V
	100-TQFP	8K	8K	2	Yes	Yes	28	1.8 mA/MIP	3.3V
	144-miniBGA	8K	8K	2	Yes	Yes	40	1.8 mA/MIP	3.3V
ADSP-2186	100-TQFP	8K	8K	2	Yes	Yes	40	1.8 mA/MIP	5V
	100-TQFP	8K	8K	2	Yes	Yes	33	1.8 mA/MIP	5V
	100-TQFP	8K	8K	2	Yes	Yes	28	1.8 mA/MIP	5V
ADSP-2185L	100-TQFP	16K	16K	2	Yes	Yes	52	0.8 mA/MIP	3.3V
	100-TQFP	16K	16K	2	Yes	Yes	40	0.8 mA/MIP	3.3V
	100-TQFP	16K	16K	2	Yes	Yes	33	0.8 mA/MIP	3.3V
	100-TQFP	16K	16K	2	Yes	Yes	28	0.8 mA/MIP	3.3V
	144-miniBGA	16K	16K	2	Yes	Yes	40	0.8 mA/MIP	3.3V
ADSP-2185	100-TQFP	16K	16K	2	Yes	Yes	40	1.8 mA/MIP	5V
	100-TQFP	16K	16K	2	Yes	Yes	33	1.8 mA/MIP	5V
	100-TQFP	16K	16K	2	Yes	Yes	28	1.8 mA/MIP	5V
ADSP-2184L	100-TQFP	4K	4K	2	Yes	Yes	33	1.8 mA/MIP	3.3V
ADSP-2184	100-TQFP	4K	4K	2	Yes	Yes	33	1.8 mA/MIP	5V
ADSP-2183	144-miniBGA	16K	16K	2	Yes	Yes	52	0.8 mA/MIP	3.3V

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