Dual PLL Frequency Synthesizer

Preliminary Technical Data — ADF4206/ADF4207/ADF4208

FEATURES

ADF4206: 500MHz/500MHz
ADF4207: 1.1GHz/1.1GHz
ADF4208: 2.0GHz/1.1GHz
+2.7 V to +5.5 V Power Supply
Selectable Charge Pump Currents
Selectable Dual Modulus Prescaler
3-Wire Serial Interface
Power Down Mode

APPLICATIONS

Portable Wireless Communications (PCS/PCN, Cordless)
Cordless and Cellular Telephone Systems
Wireless Local Area Networks (WLANs)
Cable TV Tuners (CATV)
Pagers

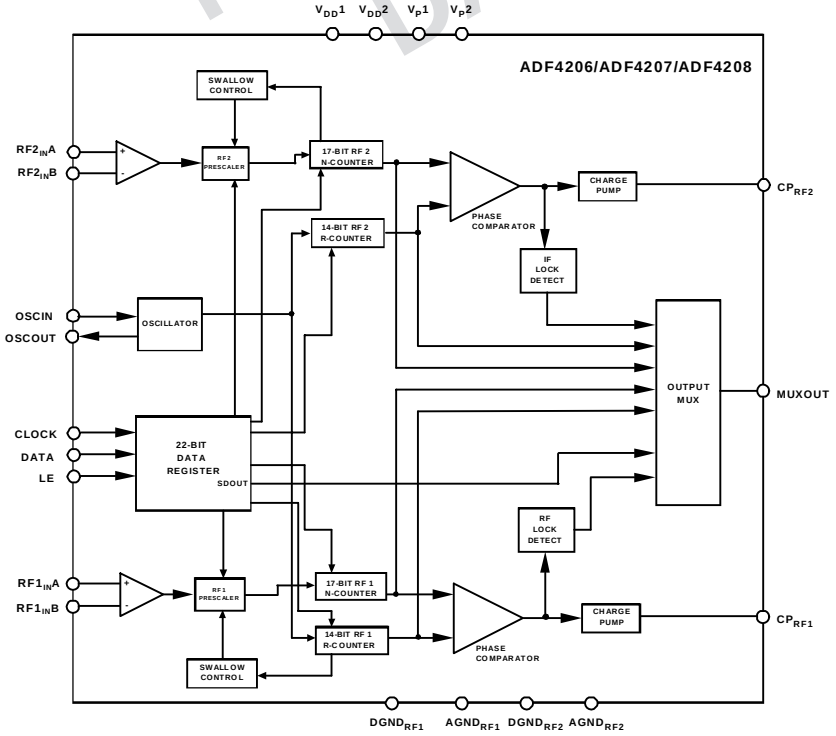
GENERAL DESCRIPTION

The ADF4206/ADF4207/ADF4208 is a dual frequency synthesizer which can be used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters. They consist of a low-noise digital PFD (Phase Frequency Detector), a precision charge pump, a programmable reference divider, programmable A and B counters and a dual-modulus prescaler (P/P+1). The A (6-bit) and B (11-bit) counters, in conjunction with the dual modulus prescaler (P/P+1), implement an N divider (N= BP+A). In addition, the 14-bit reference counter (R Counter), allows selectable REFIN frequencies at the PFD input. A complete PLL (Phase-Locked Loop) can be implemented if the synthesizers are used with an external loop filter and VCO's (Voltage Controlled Oscillators)

Control of all the on-chip registers is via a simple 3-wire interface.

The devices operate with a 3V (± 10%) or 5V(± 10%) power supply and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM



REV.PrD 07/99

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ADF4206/07/08 – SPECIFICATIONS[1] (V_{DD} = +3 V ± 10%, +5 V ± 10%; V_P = V_{DD}, +5 V ± 10%; GND = 0 V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	B Version	BChips	Units	Test Conditions/Comments
RF CHARACTERISTICS				
RF 1 Input Frequency ($RF1_{IN}$)				
ADF4206	50/500	50/500	MHz min/max	
ADF4207	0.05/1.1	0.05/1.1	GHz min/max	
ADF4208	0.1/2.0	0.1/2.0	GHz min/max	
RF 2 Input Frequency ($RF2_{IN}$)				
ADF4206	50/500	50/500	MHz min/max	
ADF4207	0.05/1.1	0.05/1.1	GHz min/max	
ADF4208	0.05/1.1	0.05/1.1	GHz min/max	
Reference Input Frequency	5/40	5/40	MHz min/max	
Phase Detector Frequency	10	10	MHz max	
RF Input Sensitivity	-15/0	-15/0	dBm min/max	3V Power Supply
	-10/0	-10/0	dBm min/max	5V Power Supply
Reference Input Sensitivity	-5	-5	dBm min	
CHARGE PUMP				
I_{CP} sink/source				
High Value	5	5	mA typ	
Low Value	625	625	µA typ	
I_{CP} Three State Current	1	1	nA max	
Sink and Source Current Matching	2	2	% typ	$0.5V < V_{CP} < V_P - 0.5$
I_{CP} vs. V_{CP}	2	2	% typ	$0.5V < V_{CP} < V_P - 0.5$
I_{CP} vs. Temperature	2	2	% typ	$V_{CP} = V_P/2$
LOGIC INPUTS				
V_{INH}, Input High Voltage	$0.8*V_{CC}$	$0.8*V_{CC}$	V min	
V_{INL}, Input Low Voltage	$0.2*V_{CC}$	$0.2*V_{CC}$	V max	
I_{INH}/I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
Oscillator Input Current	±100	±100	µA max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	V_{CC} - 0.4	V_{CC} - 0.4	V min	I_{OH} = 1mA
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{OL} = 1mA
POWER SUPPLIES				
$V_{DD}1$	2.7/5.5	2.7/5.5	V min/V max	
$V_{DD}2$	$V_{CC}1$			
V_P	$V_{CC}1$/5.5	$V_{CC}1$/5.5	V min/V max	
I_{DD}				
ADF4206	4.0	4.0	mA max	
ADF4207	4.5	4.5	mA max	
ADF4208	5.0	5.0	mA max	
Low Power Sleep Mode	1	1	µA typ	

ADF4206/07/08 – SPECIFICATIONS[1] (V_{DD} = +3 V ± 10%, +5 V ± 10%; V_P = V_{DD}, +5 V ± 10%; GND = 0 V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	B Version	BChips	Units	Test Conditions/Comments
NOISE CHARACTERISTICS				
Phase Noise Floor	-173	-173	dBc/Hz typ	@ 25kHz PFD Frequency
	-165	-165	dBc/Hz typ	@ 200kHz PFD Frequency
Phase Noise Performance[2]				@ VCO Output
ADF4206 (RF1, RF2)[3]	-97	-97	dBc/Hz typ	
ADF4207 (RF1, RF2), ADF4208 (RF2)[4]	-91	-91	dBc/Hz typ	
ADF4207 (RF1, RF2), ADF4208 (RF2)[5]	-82	-82	dBc/Hz typ	
ADF4208 (RF1)[6]	-85	-85	dBc/Hz typ	
ADF4208 (RF1)[7]	-66	-66	dBc/Hz typ	
Spurious Signals				Measured at offset of f_{PFD}, $2f_{PFD}$
ADF4206 (RF1, RF2)[3]	tbd/tbd	tbd/tbd	dB typ	
ADF4207 (RF1, RF2), ADF4208 (RF2)[4]	tbd/tbd	tbd/tbd	dB typ	
ADF4207 (RF1, RF2), ADF4208 (RF2)[5]	tbd/tbd	tbd/tbd	dB typ	
ADF4208 (RF1)[6]	tbd/tbd	tbd/tbd	dB typ	
ADF4208 (RF1)[7]	tbd/tbd	tbd/tbd	dB typ	

NOTES

1 Operating temperature range is as follows: B Version: –40°C to +85°C.

2 The phase noise is measured with the EVAL-ADF4206/7EB or the EVAL-ADF4208EB Evaluation Boards and the HP8562E Spectrum Analyzer. The spectrum analyzer provides the REFIN for the synthesizer. (f_{REFOUT} = 10MHz @ 0dBm)

3. f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{RF} = 460MHz; N = 2300; Loop B/W = 20kHz
4. f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{RF} = 900MHz; N = 4500; Loop B/W = 12kHz
5. f_{REFIN} = 10 MHz; f_{PFD} = 30kHz; Offset frequency = 1 kHz; f_{RF} = 836MHz; N = 27867; Loop B/W = 3kHz
6. f_{REFIN} = 10 MHz; f_{PFD} = 200kHz; Offset frequency = 1 kHz; f_{RF} = 1880MHz; N = 9400; Loop B/W = 20kHz
7. f_{REFIN} = 10 MHz; f_{PFD} = 10kHz; Offset frequency = 250Hz; f_{RF} = 1880MHz; N = 188000; Loop B/W = 1kHz

Specifications subject to change without notice.

CHIP LAYOUT

TIMING CHARACTERISTICS (V_{DD} = +5 V 10%, +3 V ± 10%; GND = 0 V, unless otherwise noted)

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Units	Test Conditions/Comments
t_1	50	ns min	DATA to CLOCK Set Up Time
t_2	10	ns min	DATA to CLOCK Hold Time
t_3	50	ns min	CLOCK High Duration
t_4	50	ns min	CLOCK Low Duration
t_5	50	ns min	CLOCK to LE Set Up Time
t_6	50	ns min	LE Pulse Width

NOTE
Guaranteed by Design but not Production Tested.

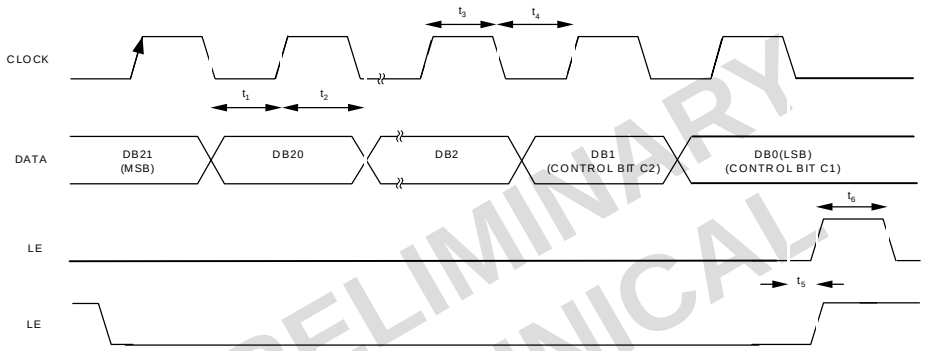

Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... –0.3 V to V_P +0.3 V
V_P to GND ..... –0.3 V to +7 V
V_P to V_{DD} ..... – 0.3 V to +7 V
Digital I/O Voltage to GND ..... –0.3 V to V_{CC} + 0.3 V
Analog I/O Voltage to GND ..... –0.3 V to V_P + 0.3 V
Operating Temperature Range
Industrial (B Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Maximum Junction Temperature ..... +150°C
TSSOP θ_{JA} Thermal Impedance ..... TBD°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This device is a high-performance RF integrated circuit with an ESD rating of < 2kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADF4206BRU	–40°C to +85°C	RU-16
ADF4206BCHIPS	–40°C to +85°C	
ADF4207BRU	–40°C to +85°C	RU-16
ADF4207BCHIPS	–40°C to +85°C	
ADF4208BRU	–40°C to +85°C	RU-20
ADF4208BCHIPS	–40°C to +85°C	

*RU = Thin Shrink Small Outline Package (TSSOP).

PIN DESCRIPTION

Mnemonic	Function
$V_{DD}1$	Positive power supply for the RF1 section. A 0.1µF capacitor should be connected between this pin and the RF1 ground pin, $DGND_{RF1}$. $V_{DD}1$ should have a value of +5V ± 10% or +3V ± 10%. $V_{DD}1$ must have the same potential as $V_{DD}2$.
V_P1	Power supply for the RF1 charge pump. This should be greater than or equal to V_{DD}.
CP_{RF1}	Output from the RF1 charge pump. This is normally connected to a loop filter which drives the input to an external VCO.
$DGND_{RF1}$	Ground pin for the RF1 digital circuitry.
$RF1_{IN}A/RF1_{IN}$	Input to the RF1 Prescaler. This low-level input signal is normally taken from the RF1 VCO.
$RF1_{IN}B$	Complementary Input to the RF1 Prescaler of the ADF4208. This point should be decoupled to the ground plane with a small bypass capacitor. If this is not done then there will be some degradation in RF sensitivity.
$AGND_{RF1}$	Ground pin for the RF1 analog circuitry.
OSC_{IN}	Oscillator Input. It has a $V_{DD}/2$ threshold and can be driven from an external CMOS or TTL logic gate.
OSC_{OUT}	Oscillator output.
MUXOUT	This multiplexer output allows either the IF/RF Lock Detect, the scaled RF or the scaled Reference Frequency to be accessed externally.
CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 22-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
$AGND_{RF2}$	Ground pin for the RF2 analog circuitry.
$RF2_{IN}B$	Complementary Input to the RF2 Prescaler. This point should be decoupled to the ground plane with a small bypass capacitor. If this is not done then there will be some degradation in RF2 sensitivity.
$RF2_{IN}A/RF2_{IN}$	Input to the RF2 Prescaler. This low-level input signal is normally taken from the RF2 VCO.
$DGND_{RF2}$	Ground pin for the RF2, digital, interface and control circuitry.
CP_{RF2}	Output from the RF2 charge pump. This is normally connected to a loop filter which drives the input to an external VCO.
V_P2	Power supply for the RF2 charge pump. This should be greater than or equal to V_{DD}.
$V_{DD}2$	Positive power supply for the RF2, interface and oscillator sections. A 0.1µF capacitor should be connected between this pin and the RF2 ground pin, $DGND_{RF2}$. $V_{DD}2$ should have a value of +5V ± 10% or +3V ± 10%. $V_{DD}2$ must have the same potential as $V_{DD}1$.

PIN CONFIGURATIONS