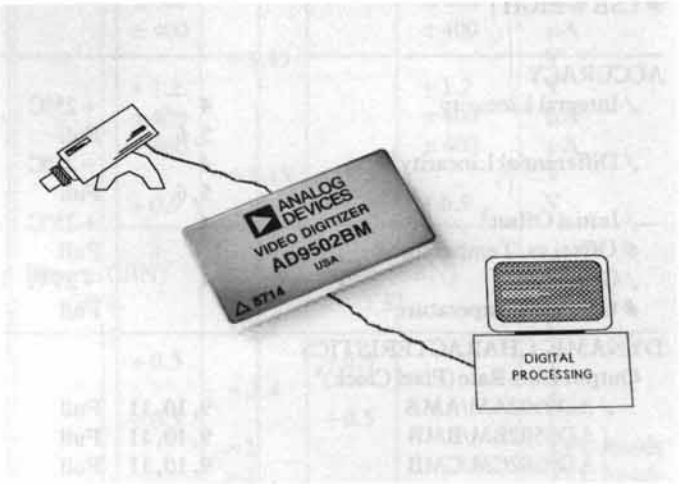
Hybrid RS-170 Video Digitizer

AD9502

FEATURES
8-Bit Gray Scale Resolution
Screen Resolution to 512×512
Phase-Locked Pixel Clock
TTL Compatible

APPLICATIONS
Machine Vision Systems
Automatic Inspection
Image Processing



GENERAL DESCRIPTION

The Analog Devices' AD9502 is a video digitizer which converts RS-170, NTSC, or PAL camera signals directly into 8-bit digital information and control signals.

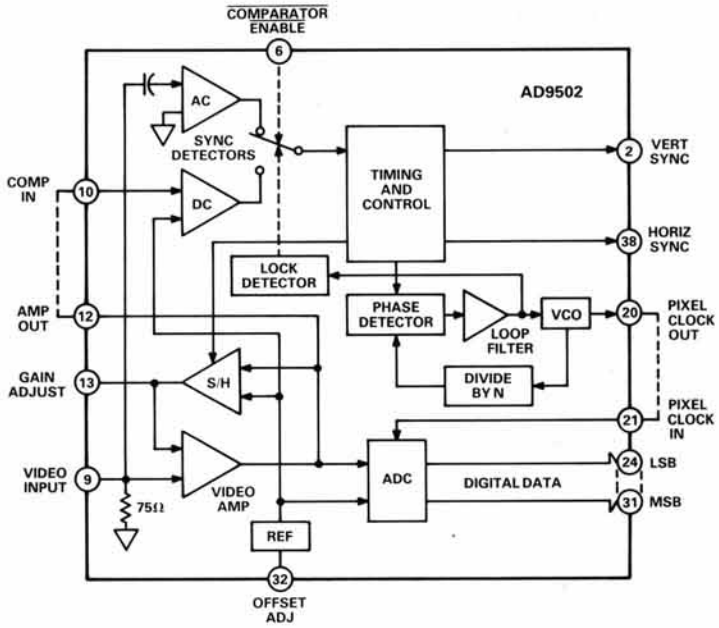
All of the analog preprocessing functions needed to move from the analog world of cameras to the digital world of signal processing are contained in this single hybrid component.

Included are a video amplifier with dc restoration, sync detector and separator, phase-locked pixel clock oscillator, and an 8-bit analog-to-digital converter. The AD9502 is also extremely adapatable by virtue of providing for ±3dB gain control and offset variations of 0 to 10 IRE units. These latter characteristics increase the flexibility of the device by making it useable over a wide range of input signal amplitudes and set up level outputs from various types of cameras.

A pixel clock synchronized to the sync portion of the composite signal is generated by the phase-locked oscillator and the sync detector/separator circuit. Depending on model number, the nominal frequency of this clock is 7.31MHz, 9.83MHz, or 12.85MHz. These frequencies correspond to 512 pixels per line or 384 pixels per line, and aspect ratios of 4:3 or 1:1.

In addition to the pixel clock, AD9502 control signals also include horizontal and vertical sync pulses. This combination of outputs allows the user to manage frame memory efficiently; output data can be precisely located for optimum support of complex digital signal processing algorithms.

Six models of the AD9502 are available; all units operate over case temperature ranges of −25°C to +85C. Models AD9502AM, AD9502BM, and AD9502CM with pixel clock frequencies of 7.31MHz, 9.83MHz, and 12.85MHz, respectively, are tested at +25°C. Models AD9502AMB, AD9502BMB, and AD9502CMB, with the same clock frequencies, are tested at temperatures from −25°C to +85°C. During their manufacturing, these latter units also receive additional high-reliability processing.



AD9502 Functional Block Diagram

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SPECIFICATIONS (typical @ +25°C with nominal supplies, unless otherwise noted)

Parameter[1,2]	Sub Group	Temp	−25°C to +85°C AD9502AM/BM/CM[1] Min	Typ	Max	−25°C to +85°C AD9502AMB/BMB/CMB[2] Min	Typ	Max	Units
RESOLUTION									
(GS = Gray Scale)				8			8		Bits
(FS = Full Scale)				0.4			0.4		% GS
# LSB WEIGHT[3]				8.4			8.4		mV
				0.39			0.39		IRE Units
ACCURACY									
√ Integral Linearity	4	+25°C		±1.0	±2.5		±1.0	±2.5	% FS
	5,6	Full		±1.5	±3.0		±1.5	±3.0	% FS
√ Differential Linearity[4]	4	+25°C		±2	±3.0		±2	±3.0	LSB
	5,6	Full		±2	±3.0		±2	±3.0	LSB
√ Initial Offset[5]	4	+25°C		±50	±200		±50	±200	mV
# Offset vs. Temperature		Full		±250			±250		µV/°C
√ Gain[6]	4	+25°C	1.91	2.8	4	1.91	2.8	4	V/V
# Gain vs. Temperature[7]		Full		±250			±250		ppm/°C
DYNAMIC CHARACTERISTICS									
Output Data Rate (Pixel Clock)[8]									
√ AD9502AM/AMB	9, 10, 11	Full		7.31			7.31		MHz
√ AD9502BM/BMB	9, 10, 11	Full		9.83			9.83		MHz
√ AD9502CM/CMB	9, 10, 11	Full		12.85			12.85		MHz
# Sampling Jitter		+25°C		1	5		1	5	ns, rms
# Digital Output Delay		+25°C	20	30	50	20	30	50	ns
√ Horizontal Sync Delay	9	+25°C	−0.4	0.3	0.7	−0.4	0.3	0.7	µs
√ Horizontal Sync Delay	10, 11	Full	−0.4	0.3	0.7	−0.4	0.3	0.7	µs
√ Horizontal Sync Width	9	+25°C	4.5	4.8	5.4	4.5	4.8	5.4	µs
√ Horizontal Sync Width	10, 11	Full	4.5	4.8	5.4	4.5	4.8	5.4	µs
√ Vertical Sync Delay	9	+25°C	5.5	6.0	6.7	5.6	6.0	6.7	µs
√ Vertical Sync Delay	10, 11	Full	5.5	6.0	6.7	5.6	6.0	6.7	µs
√ Sample Delay	9	+25°C	7.9	9.0	9.4	7.9	9.0	9.4	µs
√ Sample Delay	10, 11	Full	7.9	9.0	9.4	7.9	9.0	9.4	µs
VIDEO INPUT									
Signal Type				RS-170			RS-170		
√ Impedance	1	+25°C	67	75	83	67	75	83	Ω
√ Impedance	2, 3	Full	67	75	83	67	75	83	Ω
Input level for rated performance									
# Amplitude		+25°C	0.71	1.0	1.41	0.71	1.0	1.41	V p-p
# Amplitude		Full	0.71	1.0	1.41	0.71	1.0	1.41	V p-p
# Dynamic Range									
(back porch ref. to ground)		25°C	−0.83		+1.5	−0.83		+1.5	V
# Dynamic Range		Full	−0.83		+1.5	−0.83		+1.5	V
# Bandwidth (3dB)		+25°C	5	7.5		5	7.5		MHz
# Bandwidth (3dB)		Full	5	7.5		5	7.5		MHz
AUXILIARY SYNC INPUT[9]									
Comparator (Pin 10)									
Width			1		6	1		6	µs
Frequency[8]				15.75			15.75		kHz
# Loading				<1			<1		TTL Load
Input Current									
√ I_{IN} High (V_{IN} = 2.75V)	1	+25°C			50			50	µA
√ I_{IN} Low (V_{IN} = 2.3V)	1	+25°C			50			50	µA
√ Logic Level "1"	1	+25°C	+2.75			+2.75			V
√ Logic Level "0"	1	+25°C			+2.3			+2.3	V
√ I_{IN} High (V_{IN} = 2.75V)	2, 3	Full			50			50	µA
√ I_{IN} Low (V_{IN} = 2.3V)	2, 3	Full			50			50	µA
√ Logic Level "1"	2, 3	Full	+2.75			+2.75			V
√ Logic Level "0"	2, 3	Full			+2.3			+2.3	V

Parameter[1,2]	Sub Group	Temp	−25°C to +85°C AD9502AM/BM/CM[1] Min	Typ	Max	−25°C to +85°C AD9502AMB/BMB/CMB[2] Min	Typ	Max	Units
AUXILIARY SYNCH INPUT[9] (Cont.)									
Comparator Enable (Pin 6)									
# Loading				<1			<1		TTL Load
Input Current									
√ I_{IN} Low (V_{IN} = 0.0V)	1	+25°C			±400			±400	μA
√ I_{IN} High (V_{IN} = 5.0V)	1	+25°C			±400			±400	μA
√ Logic Level "1"	1	+25°C	+3.15			+3.15			V
√ Logic Level "0"	1	+25°C			+1.2			+1.2	V
√ I_{IN} High (V_{IN} = 0V)	2,3	Full			±400			±400	μA
√ I_{IN} Low (V_{IN} = 5.0V)	2,3	Full			±400			±400	μA
√ Logic Level "1"	2,3	Full	+3.15			+3.15			V
√ Logic Level "0"	2,3	Full			+0.9			+0.9	V
DIGITAL OUTPUTS									
Coding[10]			Comp. Binary (CBN)			Comp. Binary (CBN)			
Logic Compatibility			TTL			TTL			
√ Logic Level "1"	1	+25°C	+2.4			+2.4			V
√ Logic Level "0"	1	+25°C			+0.5		+0.5		V
√ Logic Level "1"	2,3	Full	+2.4			+2.4			V
√ Logic Level "0"	2,3	Full			+0.5		+0.5		V
√ Drive	1	+25°C	≥2			≥2			TTL Loads
√ Drive	2,3	Full	≥2			≥2			TTL Loads
# Time Skew		+25°C		10		10			ns
# Time Skew		Full		10		10			ns
POWER REQUIREMENTS									
√ +V_S (+12 to +15V dc)	1	+25°C		50	75		50	75	mA
√ −V_S (−12 to −15V dc)	1	+25°C		30	45		30	45	mA
√ +V_{CC} (+5V dc ±5%)	1	+25°C		110	150		110	150	mA
√ Power Dissipation	1	+25°C		1.75	2.55		1.75	2.55	W
√ +V_S (+12 to +15V dc)	2,3	Full		50	75		50	75	mA
√ −V_S (−12 to −15V dc)	2,3	Full		30	45		30	45	mA
√ V_{CC} (+5V dc ±5%)	2,3	Full		110	150		110	150	mA
√ Power Dissipation	2,3	Full		1.75	2.55		1.75	2.55	W
THERMAL RESISTANCE									
# Junction to Air (θ_{ja})				18			18		°C/W
# Junction to Case (θ_{jc})				4			4		°C/W
PRICES – (1–24)				289			508		$

NOTES
√ 100% tested (see Notes 1 and 2).
Specification guaranteed by design; not tested.
[1]AD9502AM/BM/CM specifications preceded by a check (√) are tested at +25°C ambient temperature; performance is guaranteed over case temperature range of −25°C to 85°C.
[2]AD9502AMB/BMB/CMB specifications preceded by a check (√) are tested at −25°C case, +25°C ambient, and +85°C case temperatures unless otherwise indicated (See Explanation of Group A Military Subgroups).
[3]Internal ADC reference = 2.15V = 100 IRE units.
[4]Specifications shown guaranteed over temperature on AD9502AMB/BMB/CMB.
[5]Offset is difference between voltage reference at OFFSET ADJUST (Pin 32) and the dc restored voltage value at AMP OUT (Pin 12). Offset is adjustable with external potentiometer to accommodate 0 to 10 IRE units of setup level.
[6]Adjustable with external potentiometer. Compensates for 3dB variation from nominal 1V p-p composite signal.
[7]Gain tempco is equal to the voltage reference at OFFSET ADJUST (Pin 32).
[8]Pixel clock stability is directly related to 15.75kHz input clock stability. Frequency of pixel clock is set at factory for desired aspect ratio and screen resolution; consult Table I for available frequency selections.
[9]Auxiliary sync can be driven from TTL source and can be composite or horizontal only. In horizontal, no output provided at VERTICAL SYNC (Pin 2).
[10]Reference black level output code = 1111 1111; reference white = 0000 0000.

EXPLANATION OF GROUP A MILITARY SUBGROUPS

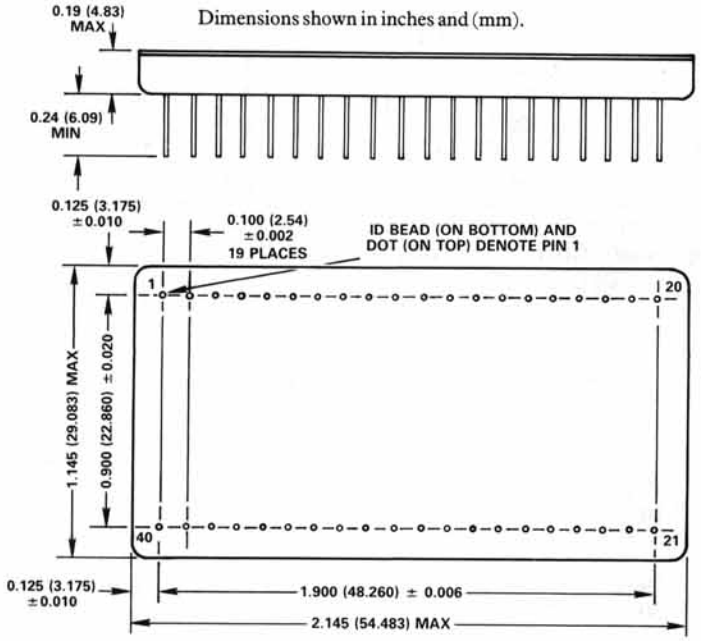
Subgroup 1 – Static tests at +25°C. (10% PDA calculated against Subgroup 1 for high-rel versions.)
Subgroup 2 – Static tests at max rated operating temp.
Subgroup 3 – Static tests at min rated operating temp.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at max rated operating temp.
Subgroup 6 – Dynamic tests at min rated operating temp.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at max and min rated operating temperatures.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at max rated operating temp.
Subgroup 11 – Switching tests at min rated operating temp.
Subgroup 12 – Periodically sample tested.

ABSOLUTE MAXIMUM RATINGS

Logic Supply Voltage ($\pm V_S$) . . . . . $\pm 18V$
Operating Temperature Range (Case)
AD9502AM/BM/CM . . . . . $-25°C$ to $+85°C$
AD902AMB/BMB/CMB . . . . . $-25°C$ to $+85°C$
Junction Temperature . . . . . $+165°C$
Storage Temperature Range . . . . . $-65°C$ to $+150°C$
Lead Soldering Temperature (Soldering 10sec) . . . . $+300°C$

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	DO NOT CONNECT*	40	CASE GROUND
2	VERTICAL SYNC	39	GROUND
3	CASE GROUND	38	HORIZONTAL SYNC
4	GROUND	37	+5V dc
5	+5V dc	36	GROUND
6	$\overline{\text{COMPARATOR ENABLE}}$	35	+5V dc
7	DO NOT CONNECT*	34	DO NOT CONNECT*
8	+5 V dc	33	GROUND
9	VIDEO INPUT	32	OFFSET ADJUST
10	COMPARATOR INPUT	31	BIT 1 (MSB)
11	DO NOT CONNECT*	30	BIT 2
12	AMPLIFIER OUTPUT	29	BIT 3
13	GAIN ADJUST	28	BIT 4
14	+V (+12V to +15V)	27	BIT 5
15	−V (−12V to −15V)	26	BIT 6
16	GROUND	25	BIT 7
17	GROUND	24	BIT 8 (LSB)
18	DO NOT CONNECT*	23	+5V dc (ADC)
19	+5V dc (VCO)	22	ANALOG GROUND
20	PIXEL CLOCK OUT	21	PIXEL CLOCK IN

*THESE PINS ARE USED FOR FACTORY TESTING AND SHOULD NOT BE USED AS TIE POINTS OR CONNECTED INTO EXTERNAL CIRCUITS.

THEORY OF OPERATION

The use of analog-to-digital converters (ADCs) for digitizing Gray Scale picture information in a standard RS-170 composite signal is widespread throughout the video industry.

But digitizing only the picture information is not sufficient. If a complete video frame is to be stored in memory (in a technique generally called "frame grabbing"), the composite signal from the camera must have additional processing steps applied. Among others, these include dc restoration; sync detection and separation; and synchronization to a pixel clock, often "slaved" to a master system clock. Analog circuits for achieving these operations must be combined, and interfaced to digital logic for subsequent processing of the signal.

The principal functions of "front end" video processors which receive the camera signal are to sychronize the frame memory and digitize each pixel (smallest controllable picture element) of video information.

Performing these functions is common in the video industry. But the method of accomplishing them is eased considerably with the AD9502 RS-170 Video Digitizer.

Refer to the AD9502 Functional Block Diagram.

The unit consists of four major parts: a phase-locked loop (PLL), dc restoration circuits, sync detector/timing circuits, and the ADC.

The PLL comprises a phase detector, loop filter/amplifier, voltage-controlled oscillator (VCO), and a digital divider; monolithic ICs are used for each section. The frequency of the pixel clock output (at Pin 20) is an integer multiple of the horizontal line frequency and is phase locked to the sync pulses of the incoming composite signal.

A video amplifier and the sample/hold (S/H) establish a feedback loop for dc restoration of the video input. Sync detection and timing result from the combined actions of the blocks marked AC, Lock Detector, Timing & Control, and the PLL.

Refer to Figure 1, the AD9502 Timing Diagram.

As shown, the leading edge of the sync tip pulse serves as the reference point for timing the actions of the AD9502. As part of the composite signal, these pulses are amplified and inverted by the video amplifier and drive the phase-locked loop within the unit, but only after the pulses are detected and conditioned.

The PLL is unlocked during the power-up phase, or if the input signal is missing. When it is, the comparator and all timing pulses are disabled, creating an ac-coupled signal path for synchronizing the PLL.

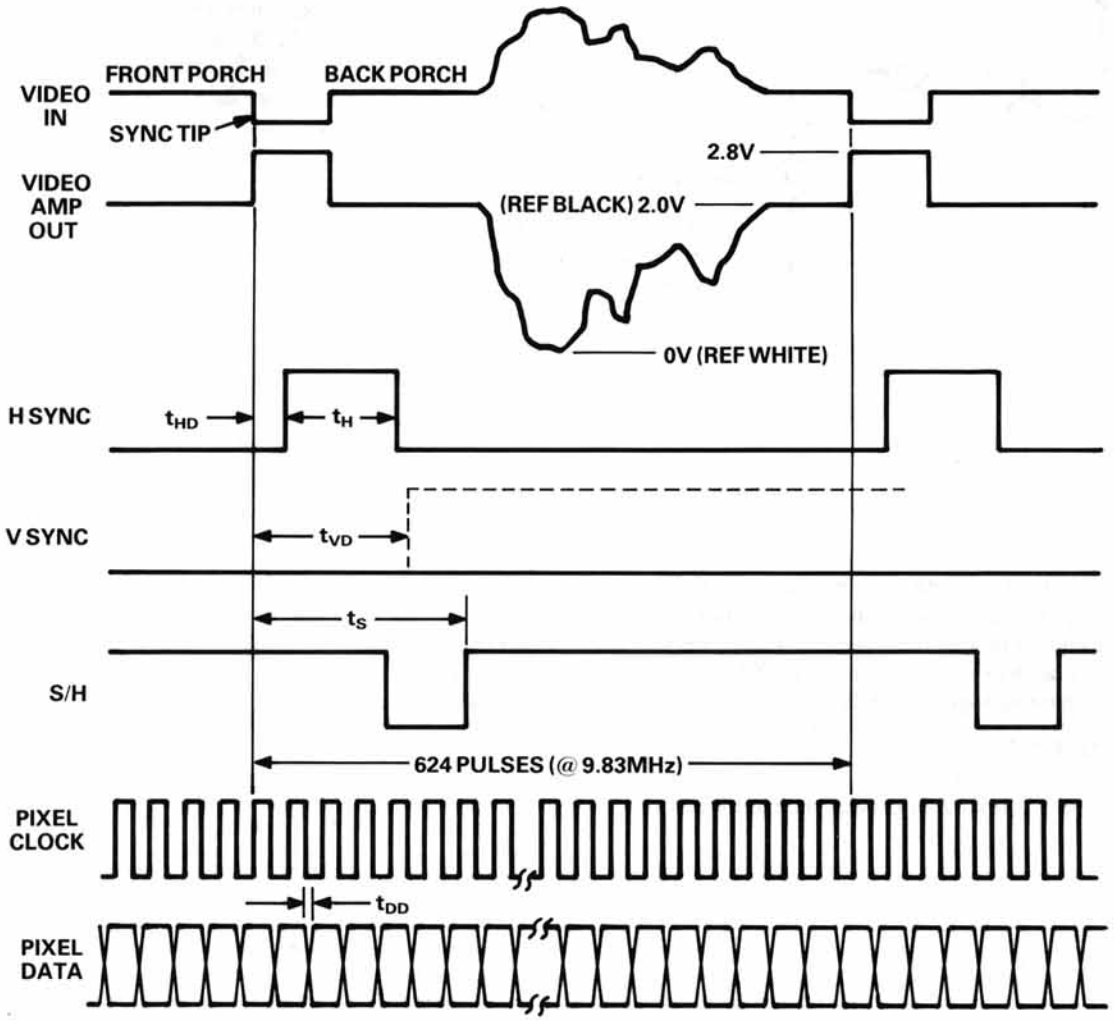
After the lock indicator detects a lock condition, the dc comparator is enabled and the ac-coupled path is disabled. The threshold of the comparator is set at slightly more than half the amplitude of the sync pulse height in the dc-restored RS-170 signal.

When the PLL is operating, the phase detector which is part of the loop generates an error voltage proportional to the timing error between the PLL's input signal (H Sync) and the VCO's divided-by-N output. If a difference exists between the two, the loop filter/amplifier shifts the VCO control voltage in the proper direction to minimize the error. The result of these actions is that the pixel clock output of the VCO is N times the horizontal frequency of the input to the AD9502.

The integer of the Divide by N circuit is set at the factory for the aspect ratio and resolution to be used by the customer and causes the phase detector to operate at a constant frequency. (Refer to ORDERING INFORMATION and Table I for details on specifying the desired frequency of the VCO).

To insure a stable pixel clock, the loop filter must block feed-through from the phase detector and noise. If it does not, the VCO will be unable to provide the required phase-coherent clock.

To some degree, clock stability and loop stability are conflicting requirements. Clock stability can be affected by noise and feed-



		µs MIN	MAX
t_{HD}	H SYNC DELAY	−0.4	+0.7
t_H	H SYNC WIDTH	+4.5	+5.4
t_{VD}	V SYNC DELAY	+5.5	+6.7
t_S	SAMPLE DELAY	+7.9	+9.4
t_{DD}	DATA DELAY	+0.02	+0.05

Figure 1. AD9502 Timing Diagram

through; loop stability can affect the acquisition time of the loop. The design of the unit has been optimized to minimize noise and feedthrough while assuring the PLL will lock during a vertical retrace period.

The vertical sync pulse (VSYNC) which is the other output of the Timing & Control circuit shown in the block diagram is generated whenever the duration of the incoming sync pulse is longer than 6.6µs. These pulses are shown with a dashed line in Figure 1 (and Figure 3) to indicate they are present only after the correct number of lines (containing horizontal sync information) have occurred and the display must be vertically retraced.

The sample-hold (S/H) pulse occurs after every incoming sync pulse except (a) when a vertical sync pulse occurs; or (b) when the PLL is not locked.

As shown, the S/H pulse occurs during the "back porch" of the composite signal. During this sample period, a closed loop formed by the video amplifier and the S/H minimizes the error between the top of the reference for the "flash" A/D converter and the back porch output level of the video amplifier.

When the S/H switches to the "hold" mode of operation during the active picture portion of the composite signal, its output inserts the correct amount of dc offset to position the video signal within the range of the A/D converter. The offset also positions the sync information properly in the range of the sync detector.

Since the RS-170 standard allows for differences in the amplitude and setup level of video signals, the AD9502 includes a capability for changing gain 3dB and varying offset by 200mV. This is illustrated in Figure 2.

Translated into practical terms pertinent to the video input, this ability to vary the input levles means the difference between the Reference Black level and the back porch of the input can be adjusted from 0 to 10 IRE units.

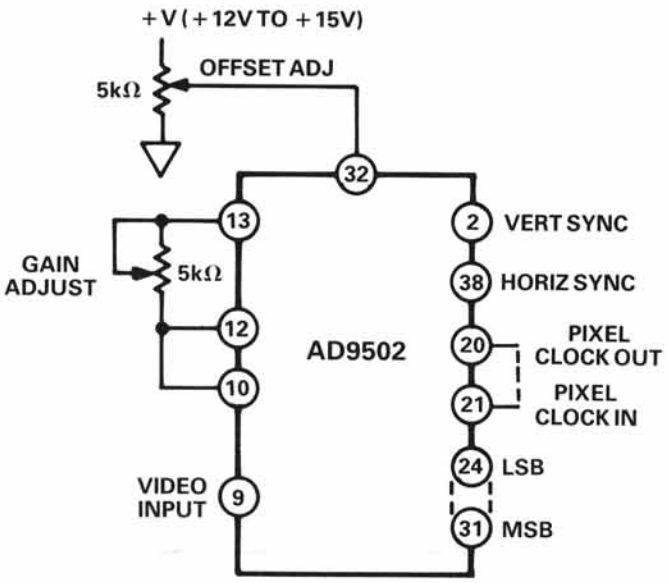


Figure 2. Offset and Gain Adjustments

As indicated earlier, the internal A/D converter is a "flash" type; it provides 8 bits of resolution of the video signal. The (+2.15 volt) voltage reference shown in the block diagram is used for the reference ladder of the converter and as a reference for dc restoration. The clock and data circuits are TTL compatible, capable of encode rates as high as 15MHz.

MONOCHROME APPLICATIONS

The discussion of applying the AD9502 in various applications may be enhanced with a brief summary of the nature of video signals.

A standard RS-170 video signal contains 525 horizontal lines of the type shown at the top of Figure 1 in each "frame." Visible picture information is contained in 485 of these lines; the remainder are used for test and reference information.

To reduce flicker on the screen, these frames of information are divided into two "fields" which are interlaced. For presentation, all odd-numbered horizontal lines are displayed on the screen from top to bottom. During vertical retrace, the electron gun of the cathode-ray tube (CRT) is repositioned from lower right to the upper left corner. When this is completed, even-numbered lines are scanned from top to bottom.

A complete frame of two fields is presented each 1/30 of a second (displaying each 242 1/2-line field at the 60Hz rate of standard power-line frequencies is the key to this technique for reducing flicker in the presentation). This means each line of horizontal information is equal to 63.5μs, i.e., 1/30/525.

The horizontal blanking interval uses 10.9μs of this time, leaving 52.6μs for displaying active picture (more correctly, "intensity") information. The resolution of this 52.6μs line will be determined by the number of pixels (smallest controllable picture element) used to digitize it.

Resolutions of 512 pixels and 384 pixels per line are the two which are generally used for computer-based display applications.

Regardless of the number of pixels, many applications which store the complete useable portion of the line will have a 4:3 aspect ratio. This is the standard ratio for RS-170 signals but non-square pixels which can result may cause problems for certain processing algorithms.

Square pixels are more desirable for these situations, and an aspect ratio of 1:1 is oftentimes preferred. To obtain it, many systems digitize only three quarters of each horizontal line; the image which results represents the center 39.45μs of the line's 52.6μs.

The AD9502 offers pixel rates which can accommodate either 4:3 or 1:1 aspect ratios in densities of either 384 pixels/line or 512 pixels/line, as shown in Table I. The frequencies cited in the first part of the table are those associated with monochrome video signals. For color cameras which supply RGB (red, green, blue) outputs, the frequencies are slightly different because of being based on the frequency of the color burst information.

NOTE: The difference of less than 1% between the theoretical 39.45μs and the 39.8μs of Table I is because of the incremental frequency settings possible with the VCO.

In most of Europe and in many other parts of the world, the PAL standard is used. This differs from NTSC by virtue of using 625 total lines, with 575 active lines; the frame rate is 25Hz instead of 30Hz. As shown in Table I, the AD9502 can also be used for these applications.

Monochrome RS-170
Horizontal Frequency = 15.750kHz

Part No	VCO (MHz)	Aspect Ratio	Active Time (μs)*	Pixels/ Line
AD9502AM	7.308	4:3	52.5	384
AD9502BM	9.828	1:1	39.0	384
AD9502BM	9.828	4:3	52.1	512
AD9502CM	12.85	1:1	39.8	512

NTSC
Horizontal Frequency = 15.734kHz

Part No	VCO (MHz)	Aspect Ratio	Active Time (μs)*	Pixels/ Line
AD9502AM	7.301	4:3	52.6	384
AD9502BM	9.818	1:1	39.1	384
AD9502BM	9.818	4:3	52.1	512
AD9502CM	12.84	1:1	39.9	512

European PAL**
Horizontal Frequency = 15.625kHz

Part No	VCO (MHz)	Aspect Ratio	Active Time (μs)*	Pixels/ Line
AD9502BM	9.750	4:3	44.1	430
AD9502CM	12.75	1:1	44.7	575

*For aspect ratio and VCO frequency shown, this is portion of the horizontal line which will be digitized.
**See ORDERING INFORMATION section.

Table I

Frame grabbers which process the video information generally store either 512 or 256 lines of information, depending upon whether they are designed to operate on a complete frame or only on each field.

In a 256-line memory system, only one of the two fields needs to be digitized; in a 512-line system, each field is stored independently.

The memory system being used must be able to identify each field to assure that each is assigned to the correct address in the memory. Figure 3 illustrates the relationships of the horizontal and vertical sync pulses generated by the AD9502, and the incoming video signal, and makes it easier to visualize how this identification is accomplished.

As shown, the horizontal and vertical sync pulses occur in time coincidence for the first field. For the second field, the start of

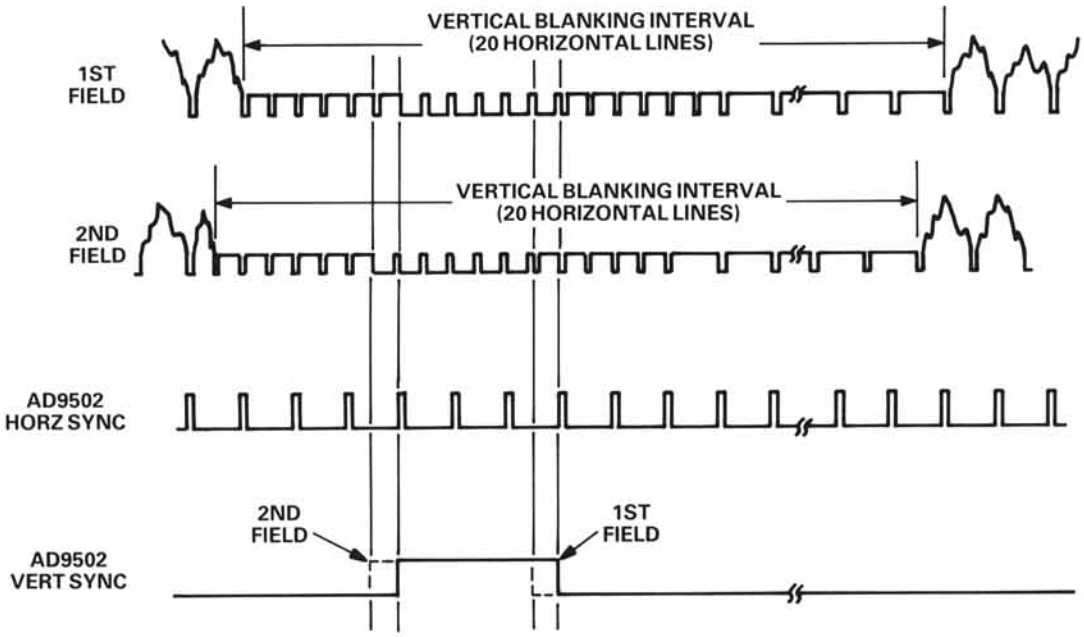


Figure 3. Field/Sync Timing Diagram

each of these two outputs occurs one-half line out of phase. In this way, the system can make a distinction between the two fields when both are to be stored.

Many systems use the pixel clock, horizontal sync, and vertical sync outputs from the AD9502 to address the frame memory for each field by triggering counters. A delay counter, in the horizontal or X axis, can be used to determine the point on the selected line where data storage begins. A second counter would count the pixels needed to obtain the desired pixels/line resolution; the number of counts will be determined by the aspect ratio being used.

Both of these counters are set by the horizontal sync pulse output of the AD9502.

Vertical retrace timing information is obtained in essentially the same way by using Y counters. For these, the counters are set by the vertical sync pulse output. The Y delay counter establishes the time of vertical retrace by counting the number of lines which occur after the vertical sync pulse; it then starts a second (lines/field) counter. The second Y counter establishes the number of lines to be digitized in each field.

Another counter circuit can be used to test for the presence or absence of the vertical sync pulse; the counter output is high if both sync pulses are present, indicating the first field.

The combination of X, Y, and first-field lines acts as address information for correctly routing the digitized picture data into the system memory.

(NOTE: Additional details are included in the Analog Devices application note, "The AD9502 Video Signal Digitizer and Its Application.")

In systems which use a master composite sync, this routing of digital information can be simplified by using the comparator enable function available on the AD9502.

Normally, Pins 10 and 12 are connected externally, as shown in the block diagram. This connection applies the output of the video amplifier to the input of the dc comparator circuit and, as discussed earlier, helps keep the PLL in a locked condition.

Alternatively, a TTL composite sync signal can be used by connecting Pin 6 ($\overline{\text{COMPARATOR ENABLE}}$) to ground. This disables the ac comparator, and the power-up and signal-loss start-up circuits; but they are no longer needed with a master sync.

Using the AD9502 in this way has the advantage of making it unnecessary for the dc comparator to operate with a video signal which may be noisy.

Besides grounding Pin 6, it is also necessary to remove the connection between Pins 10 and 12 and apply the master sync input to Pin 10. Figure 4 shows the difference in the two methods of operating the AD9502.

Note that the camera which is being used must also be locked to the master sync; if it is not, the AD9502 will not be able to sample the back porch of the composite signal for setting the dc reference of the A/D converter.

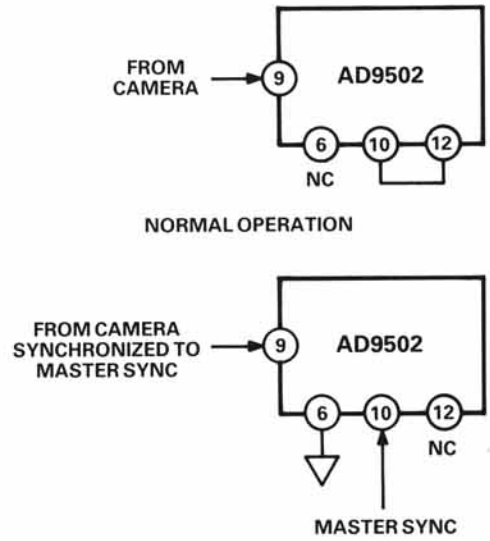


Figure 4. Monochrome Operation

COLOR (RGB) APPLICATIONS

In RGB applications, three monochrome video inputs represent the Red, Green, and Blue outputs of a color camera. Figure 5 illustrates how it is possible to configure three AD9502 units to accept RGB signals.

Generally, the Green input is used as the master sync reference; the other video digitizers are slaved from the Green sync pulses.

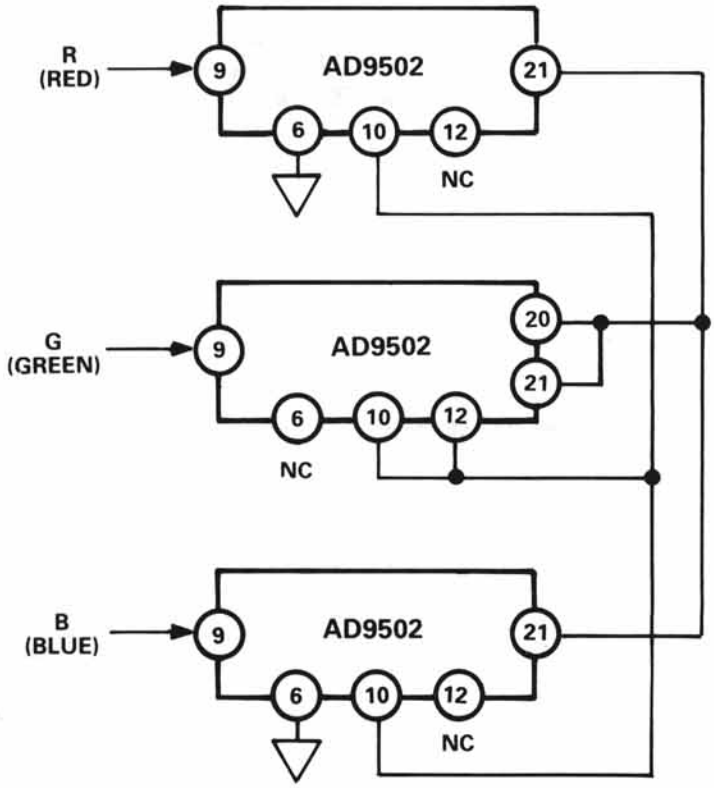


Figure 5. RGB Operation (External Pixel Clock)

When using multiple devices in this way, it is extremely important to use lead lengths which are as short as practical. The drive capability of the Green AD9502 is sufficient to drive the dc comparators in the Red and Blue digitizers, but only so long as the reactive effects of excessive lead lengths do not load the video amplifier in the Green unit.

No attempt should be made to drive low-impedance ($<25k\Omega$) loads with the output (Pin 12) of the Green digitizer. Frame memory management should use the horizontal and vertical sync pulses only from the Green AD9502.

As shown in Figure 5, the connection between Pins 20 and 21 is removed on the Red and Blue units; instead, Pin 21 of each is tied to Pins 20 and 21 of the Green unit.

The Red and Blue digitizers must have Pin 6 grounded, with a master sync (generated by the Green sync tip pulses) applied to Pin 10. Repeating for emphasis: lead lengths need to be as short as practical when applying the high-frequency pixel clock and for all connections among the digitizers.

Variations of the applications described here are possible, depending upon the system configuration and its use. In any application using an external pixel clock, the duty cycle must be set to insure that logic low is maintained for a minimum of 30ns. A shorter interval will have an adverse effect on linearity.

VCR/VTR OPERATION

The AD9502 can be operated with VCR or VTR equipment, but the sync signals which are supplied must be conditioned to insure they are stable in frequency before being applied to the device.

ORDERING INFORMATION

Six models of the AD9502 Video Digitizer are available, with three different pixel clock frequencies. Order model AD9502AM, AD9502BM, or AD9502CM for clock frequencies, respectively, of 7.31MHz, 9.83MHz, or 12.85MHz.

For units with high-rel processing and testing at the temperature extremes of $-25°C$ to $85°C$, the model numbers with the same clock frequencies contain an additional "B" suffix, i.e., AD9502AMB, AD9502BMB, or AD9502CMB.

A special PAL version of the AD9502 is available for digitizing 512×512 resolution with a 1:1 aspect ratio. Contact the factory for details.

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