a

A/D Converter

Preliminary Specification 8/21/98 AD9483

The AD9483 is a triple 8-bit monolithic analog-to-digital converter optimized for digitizing RGB graphics signals from personal computers and workstations. Its 140MSPS encode rate capability and full-power analog bandwidth of 330MHz supports display resolutions of up to 1280 x 1024 at 75Hz with sufficient input bandwidth to accurately acquire and digitize each pixel.

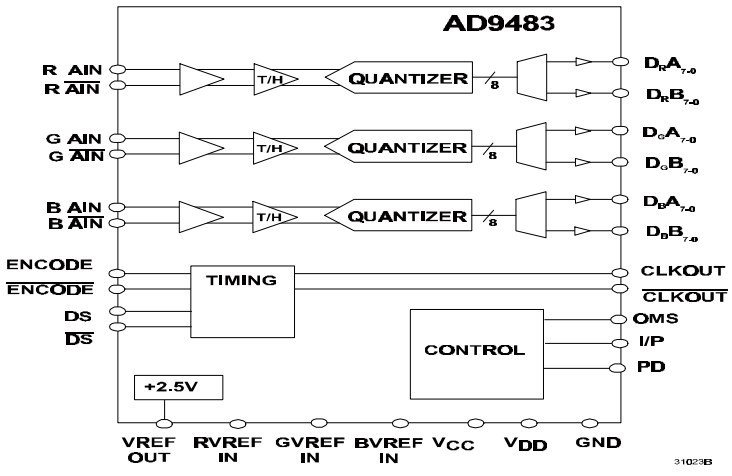
To minimize system cost and power dissipation, the AD9483 includes an internal +2.5V reference and track-and-hold circuit. The user provides only a +5V power supply and an encode clock. No external reference or driver components are required for many applications. The digital outputs are three-state CMOS outputs. Separate output power supply pins support interfacing with 3.3V or 5V logic.

The AD9483's encode input interfaces directly to TTL, CMOS, or positive-ECL logic and will operate with single-ended or differential inputs. The user may select demultiplexed or single channel digital outputs. The Dual Channel (demultiplexed) mode interleaves ADC data through two 8-bit channels at one-half the clock rate. Operation in Dual Channel mode reduces the speed and cost of external digital interfaces while allowing the ADCs to be clocked to the full 140MSPS conversion rate. In the Single Channel mode, all data is piped at the full clock rate to the Channel A outputs and the ADCs conversion rate is limited to 100MSPS. A data clock output is provided at the Channel A output data rate for both dual-channel or single-channel output modes.

Fabricated in an advanced BiCMOS process, the AD9483 is provided in a space-saving 100-lead MQFP surface mount plastic package (S-100) and is specified over the 0℃ to +85℃ temperature range.

FEATURES
140 MSPS Maximum Conversion Rate
100 MSPS Low Cost Version Available
330 MHz Analog Bandwidth
1 Vp-p Analog Input Range
Internal +2.5V Reference
Differential or Single-Ended Clock Input
3.3V/5.0V Tri-State CMOS Outputs
Single or Demultiplexed Output Ports
Data Clock Output Provided
Low Power : 1.4W Typical
+5V Converter Supply Operation

APPLICATIONS
RGB Graphics Processing
High Resolution Video
LCD Monitors and Projectors
Micromirror Projectors
Plasma Display Panels
Scan Converters



REV. 0

One Technology Way, P.O Box 9106, Norwood, MA 02062–9106, USA
Tel: 617/329–4700 **Fax: 617–326–8703**

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, V_{DD} = +3.3V, external reference, ENCODE = 140MHz differential PECL)

Parameter	Temp	Test Level	AD9483KS-140 Min	AD9483KS-140 Typical	AD9483KS-140 Max	AD9483KS-100 Min	AD9483KS-100 Typical	AD9483KS-100 Max	Units
RESOLUTION				8			8		bits
DC ACCURACY									
Differential Nonlinearity	+25°C	I		0.8	1.25/-1.0		0.8	1.25/-1.0	LSB
	Full	VI			1.50/-1.0			1.50/-1.0	LSB
Integral Nonlinearity	+25°C	I		0.9	1.50/-1.50		0.9	1.50/-1.50	LSB
	Full	VI			1.75/-1.75			1.75/-1.75	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
Gain Error [1]	+25°C	I		±0.5	±2		±0.5	±2	% FS
Gain Tempco[1]	Full	V		160			160		ppm/°C
ANALOG INPUT									
Input Voltage Range	Full	V		±512			±512		mV pp
(With Respect to AIN/)	Full	V	1.8		3.2	1.8		3.2	V
Input Offset Voltage	+25°C	I		±4	±16		±4	±16	mV
	Full	VI			±20			±20	mV
Input Resistance	+25°C	I	35	83		35	83		kΩ
	Full	VI	25			25			kΩ
Input Capacitance	+25°C	V		4			4		pF
Input Bias Current	+25°C	I		17	36		17	36	µA
	Full	VI			50			50	µA
Analog Bandwidth, Full Power	+25°C	V		330			330		MHz
REFERENCE OUTPUT									
Output Voltage	Full	VI	+2.4	+2.5	+2.6	+2.4	+2.5	+2.6	V
Temperature Coefficient	Full	V		110			110		ppm/°C
SWITCHING PERFORMANCE									
Maximum Conversion Rate	Full	VI	140			100			MSPS
Minimum Conversion Rate	Full	IV			10			10	MSPS
Encode Pulse Width High (t_{EH})	+25°C	IV	2.8		50	4.0		50	ns
Encode Pulse Width Low (t_{EL})	+25°C	IV	2.8		50	4.0		50	ns
Aperture Delay (t_A)	+25°C	V		1.5			1.5		ns
Aperture delay matching	+25°C	V		100			100		pS
Aperture Uncertainty (Jitter)	+25°C	V		2.3			2.3		ps rms
Data Sync Setup Time (t_{SDS})	+25°C	IV	0			0			ns
Data Sync Hold Time (t_{HDS})	+25°C	IV	0.5			0.5			ns
Data Sync Pulsewidth (t_{PWDS})	+25°C	IV	2.0			2.0			ns
Output Valid Time (t_V) [2]	Full	VI	5.5	6.3		5.5	6.3		ns
Output Propagation Delay (t_{PD})[2]	Full	VI		8.0	10		8.0	10	ns
Clock Valid Time (t_{CV})[3]	Full	VI	4.9	6.2		4.9	6.2		ns
Clock Propagation Delay (t_{CPD})[3]	Full	VI		8.0	7.0		8.0	7.0	ns
Data to Clock Skew (t_V-t_{CV})	Full	VI	-1.0	0	1.0	-1.0	0	1.0	ns
Data to Clock Skew (t_{PD}-t_{CPD})	Full	VI	-2.0	0	2.0	-2.0	0	2.0	ns
DIGITAL INPUTS									
Input Capacitance	+25°C	V		3			3		pF
DIFFERENTIAL INPUTS									
Differential Signal Amplitude (VID)	Full	IV	400			400			mV
HIGH Input Voltage (V_{IHD})	Full	IV	0.4		V_{CC}	0.4		V_{CC}	V
LOW Input Voltage (V_{ILD})	Full	IV	0			0			V
Common Mode Input (V_{ICM})	Full	IV	1.5			1.5			V
HIGH Level Current (I_{IH})	Full	VI			1.2			1.2	mA
LOW Level Current (I_{IL})	Full	VI			1.2			1.2	mA
SINGLE-ENDED INPUTS									
HIGH Input Voltage (V_{IH})	Full	IV	2.0		V_{CC}	2.0		V_D	V
LOW Input Voltage (V_{IL})	Full	IV	0		0.8	0		0.8	V
HIGH Level Current (I_{IH})	Full	VI			1			1	mA
LOW Level Current (I_{IL})	Full	VI			1			1	mA

Parameter	Temp	Test Level	AD9483KS-140 Min	AD9483KS-140 Typical	AD9483KS-140 Max	AD9483KS-100 Min	AD9483KS-100 Typical	AD9483KS-100 Max	Units
DIGITAL OUTPUTS									
Logic "1" Voltage	Full	VI	V_{DD}- 0.05			V_{DD}- 0.05			V
	Full	VI			0.05			0.05	V
Logic "0" Voltage									
Output Coding				Binary			Binary		
POWER SUPPLY									
V_{CC} Supply Current	Full	VI			215			215	mA
V_{DD} Supply Current	Full	VI			60			60	mA
Total Power Dissipation[4]	Full	VI			1.3			1.3	W
Powerdown Supply Current	25℃	V		4	20		4	20	mA
Powerdown Dissipation	25℃	V			100			100	mW
DYNAMIC PERFORMANCE [6]									
Transient Response	+25℃	V		1.5			1.5		ns
Crosstalk	Full	V		55			55		dB
Overvoltage Recovery Time	+25℃	V		1.5			1.5		ns
Signal-to-Noise Ratio (SNR)									
(Without Harmonics)									
f_{IN} = 19.7 MHz	+25℃	V		45			45		dB
f_{IN} = 49.7 MHz	+25℃	I	41	44		41	44		dB
f_{IN} = 69.7 MHz	+25℃	V		44			44		dB
Signal-to-Noise Ratio (SINAD)									
(With Harmonics)									
f_{IN} = 19.7 MHz	+25℃	V		44			44		dB
f_{IN} = 49.7 MHz	+25℃	I	40	43		40	43		dB
f_{IN} = 69.7 MHz	+25℃	V		42			42		dB
Effective Number of Bits									
f_{IN} = 19.7 MHz	+25℃	V		7.0			7.0		bits
f_{IN} = 49.7 MHz	+25℃	I	6.4	6.8		6.4	6.8		bits
f_{IN} = 69.7 MHz	+25℃	V		6.7			6.7		bits
2nd Harmonic Distortion									
f_{IN} = 19.7 MHz	+25℃	V		63			63		dBc
f_{IN} = 49.7 MHz	+25℃	I	50	58		50	58		dBc
f_{IN} = 69.7 MHz	+25℃	V		51			51		dBc
3rd Harmonic Distortion									
f_{IN} = 19.7 MHz	+25℃	V		55			55		dBc
f_{IN} = 49.7 MHz	+25℃	I	46	53		46	53		dBc
f_{IN} = 69.7 MHz	+25℃	V		51			51		dBc

NOTES

1. Gain error and gain temperature coefficient are based on the ADC only (with a fixed +2.5V external reference).
2. t_V and t_{PD} are measured from the threshold crossing of the ENCODE input to valid TTL levels at the digital outputs. The output ac load during test is 5pF.
3. t_{CV} and t_{CPD} are measured from the threshold crossing of the ENCODE input to valid TTL levels at the digital outputs. The output ac load during test is 20pF.
4. Measured under the following conditions: analog input is –1 dBfs at 19.7 MHz.
5. A change in input offset voltage with respect to a change in V_{DD}.
6. SNR / harmonics based on an analog input voltage of –1.0 dBfs referenced to a 1.024V full–scale input range.
7. Typical thermal impedance for the ST-100 (MQFP) 100–lead package: Θ_{JC} = TBD°C/W, Θ_{CA} = TBD°C/W, Θ_{JA} = 27°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Option
AD9483KS-100	0℃ to +85℃	ST-100
AD9483KS-140	0℃ to +85℃	ST-100
AD9483/PCB	+25℃	Evaluation Board

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at +25℃ and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at +25℃; guaranteed by design and characterization testing.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} ..... +6 V
V_{DD} ..... +6 V
Analog Inputs ..... V_{CC} to 0.0 V
VREF IN, VREF OUT ..... V_{CC} to 0.0 V
Digital Inputs ..... V_{CC} to 0.0 V
Digital Output Current ..... 20 mA
Operating Temperature ..... 0℃ to +85°C
Storage Temperature ..... ~~6~~5℃ to +150°C
Maximum Junction Temperature ..... +175°C
Maximum Case Temperature ..... +150°C

- Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Step	$A_{IN} - A_{IN}$/	Code	Binary
255	≥**0.512 V**	255	1111 1111
254	**0.508 V**	254	1111 1110
253	**0.504 V**	253	1111 1101
•	•	•	•
•	•	•	•
•	•	•	•
129	**0.006 V**	129	1000 0001
128	**0.002 V**	128	1000 0000
127	**–0.002 V**	127	0111 1111
126	**–0.006 V**	126	0111 1110
•	•	•	•
•	•	•	•
•	•	•	•
2	**–0.504 V**	2	0000 0010
1	**–0.508 V**	1	0000 0001
0	≤**–0.512 V**	0	0000 0000

Table 1. Output Coding

PIN DESCRIPTIONS

Pin Number	Name	Function
1, 6, 7, 10, 20, 30, 40, 50, 60, 70, 73, 77, 78, 80, 81, 95, 96, 100	GND	Ground
2	ENCODE	Encode clock for ADC (ADC samples on rising edge of ENCODE
3	ENCODE/	Encode clock compliment (ADC samples on falling edge of ENCODE/)
4	DS	Data Sync -Aligns output channels in Dual-Channel Mode.
5	DS/	Data Sync/ -Data Sync compliment
8	CLKOUT	Data Clock Output - Clock output at Channel A data rate
9	CLKOUT/	Data Clock Output/ - Data Clock Output compliment
11, 21, 31, 41, 51, 61, 71	V_{DD}	Output Power Supply -Nominally 3.3V
79, 82, 83, 93, 94, 98, 99	V_{CC}	Converter Power Supply -Nominally 5.0V
12-19	D_B B_7-D_BB_0	Digital Outputs of Converter "B", Channel B. D_BB_7 is the MSB.
22-29	D_B A_7-D_BA_0	Digital Outputs of Converter "B", Channel A. D_BA_7 is the MSB.
32-39	D_G B_7-D_GB_0	Digital Outputs of Converter "G", Channel B. D_GB_7 is the MSB.
42-49	D_G A_7-D_GA_0	Digital Outputs of Converter "G", Channel A. D_GA_7 is the MSB.
52-59	D_R B_7-D_RB_0	Digital Outputs of Converter "R", Channel B. D_RB_7 is the MSB.
62-69	D_R A_7-D_RA_0	Digital Outputs of Converter "R", Channel A. D_RA_7 is the MSB.
72	N/C	No connect
74	OMS	Selects single channel or demuxed output mode, (HIGH=single, LOW=demuxed).
75	I/P	Selects interleaved or parallel output mode, (HIGH=interleaved, LOW=parallel).
76	PD	Power down and three-state select (HIGH = power down)
84	R AIN/	Analog Input - Compliment for Converter "R"
85	R AIN	Analog Input - True for Converter "R"
86	R REF IN	Reference Input for Converter "R" (+2.5V typical, +/-10%)
87	G AIN/	Analog Input - Compliment for Converter "G"
88	G AIN	Analog Input - True for Converter "G"
89	G REF IN	Reference Input for Converter "G" (+2.5V typical, +/-10%)
90	B AIN/	Analog Input - Compliment for Converter "B"
91	B AIN	Analog Input - True for Converter "B"
92	B REF IN	Reference Input for Converter "B" (+2.5V typical, +/-10%)
97	REF OUT	Internal Reference Output (+2.5V typical); Bypass with .01uF to Ground

Timing

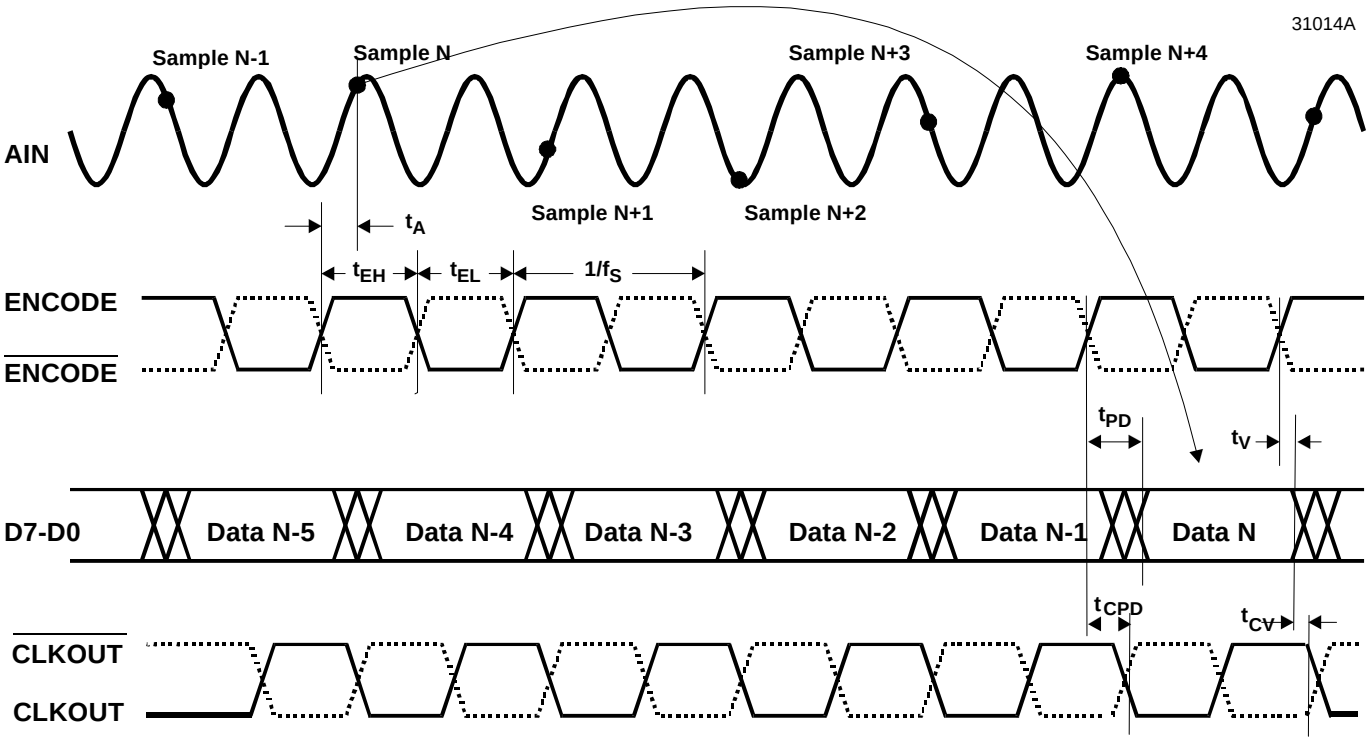


Figure 1. Timing - Single Channel Mode

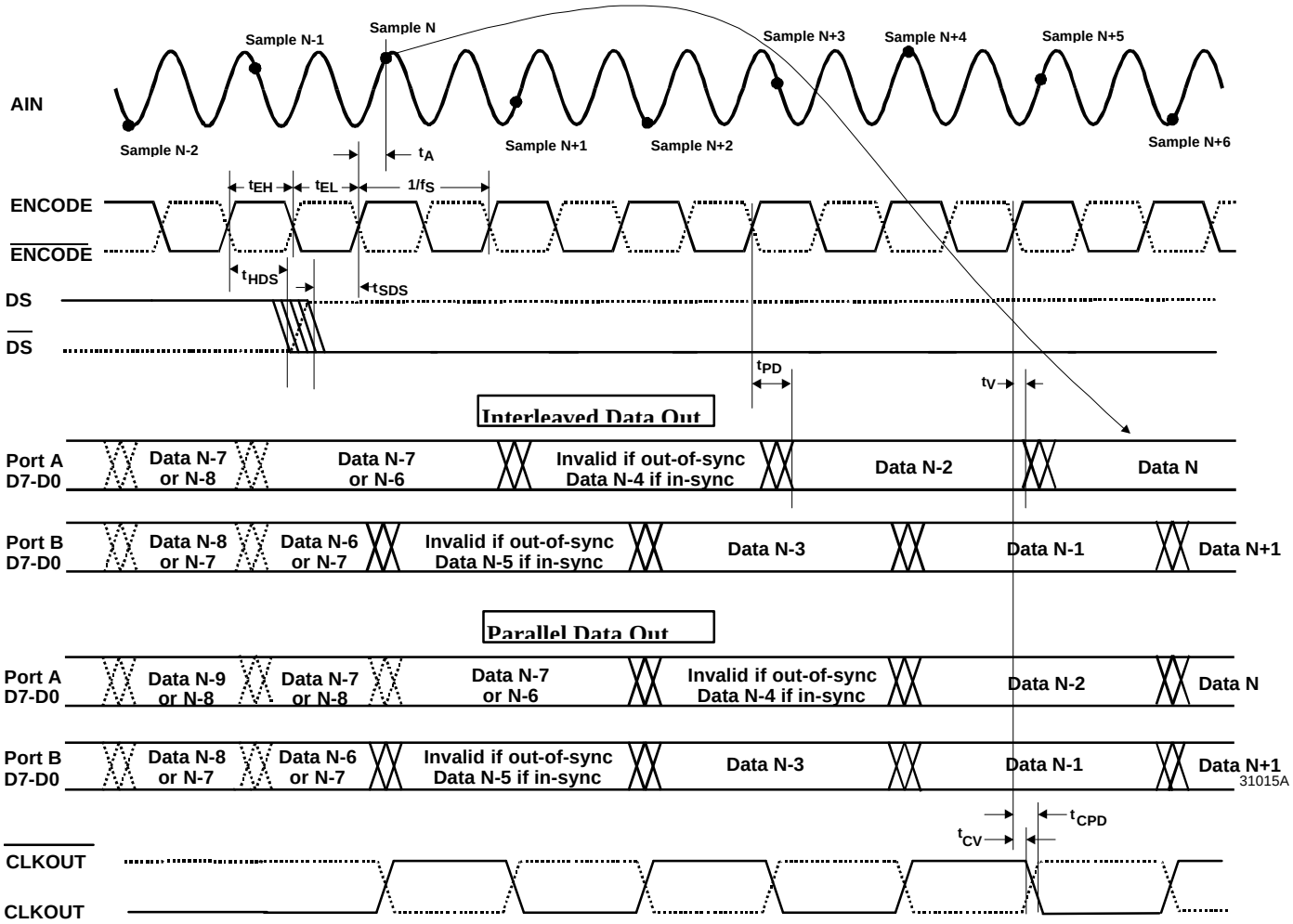


Figure 2. Timing - Dual Channel Mode

Equivalent Circuits

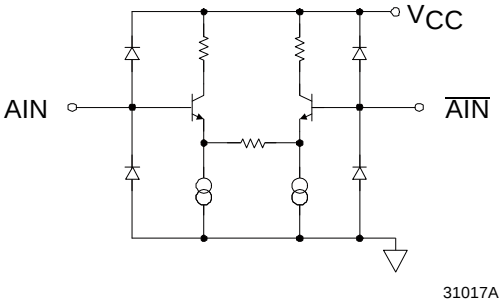


Figure 3. Equivalent Analog Input Circuit

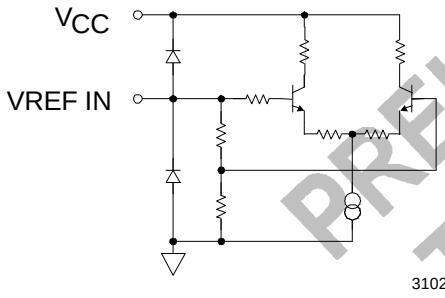


Figure 4. Equivalent Reference Input Circuit

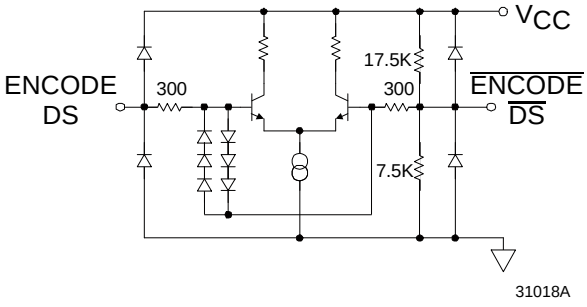


Figure 5. Equivalent Encode and Data Select Input Circuit

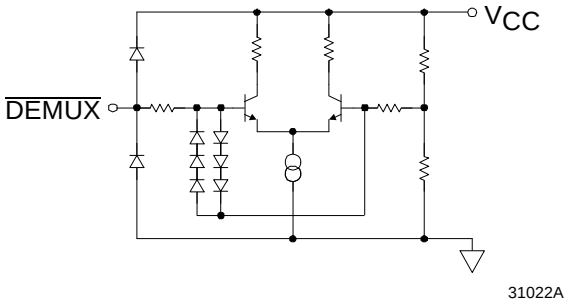


Figure 6. Equivalent DEMUX\ Input Circuit

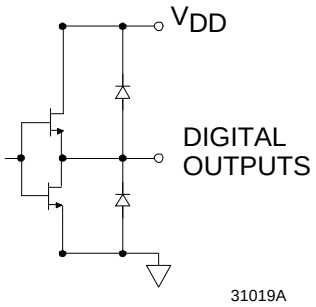


Figure 7. Equivalent Digital Output Circuit

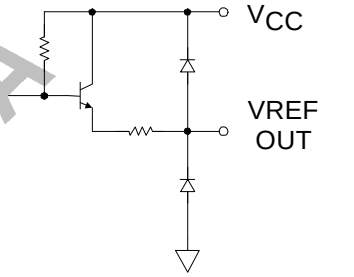


Figure 8. Equivalent Reference Output Circuit

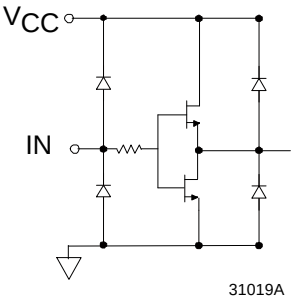


Figure 9. Equivalent Digital Input Circuit
(for PD, I/D, OMS inputs)

APPLICATION NOTES

Theory of Operation

The AD9483 combines Analog Devices'patented MagAmp bit-per-stage architecture with flash converter technology to create a high performance, low power ADC. For ease of use the part includes an on board reference and input logic that accepts TTL, CMOS, or PECL levels.

Each of the three analog input signals is buffered by a high-speed differential amplifier and applied to a track-and-hold (T/H) circuit. This T/H captures the value of the input at the sampling instant and maintains it for the duration of the conversion. The sampling and conversion process is initiated by a rising edge on the ENCODE input. Once the signal is captured by the T/H, the four Most Significant Bits (MSBs) are encoded sequentially by the MagAmp string. Then the residue signal is encoded by a flash comparator string to generate the four Least Significant Bits (LSBs). The comparator outputs are decoded and combined into the eight-bit result.

If the user has selected Single Channel Mode (OMS=HIGH) the eight bit data word is directed to an A output bank. Data are strobed to the output on the rising edge of the ENCODE input with four pipeline delays. If the user has selected Dual Channel Mode (OMS=LOW) the data are alternately directed between the A and B output banks and the data has five pipeline delays. At power up, the N sample data can appear at either the A or B port. To align the data in a known state the user must strobe DATA SYNC (DS, DS\) per the conditions described in the TIMING section.

Graphics Applications

The high bandwidth and low power of the AD9483 makes it very attractive for applications that require the digitization of pre-sampled waveforms: wherein the input signal rapidly slews from one level to another, then is relatively stable for a period of time. Examples of these include digitizing the output of computer graphic display systems, and very high speed solid state imagers.

These applications require the converter to process inputs with frequency components well in excess of the sampling rate (often with sub-nanosecond risetimes), after which the A/D must settle and sample the input in well under one pixel time. The architecture of the AD9483 is vastly superior to older flash architectures, which not only exhibit excessive input capacitance (which is very hard to drive) but can make major errors when fed a very rapidly slewing signal. The AD9483s extremely wide bandwidth Track/Hold circuit processes these signals without difficulty.

Using the AD9483

Good high-speed design practices must be followed when using the AD9483. Decoupling capacitors should be physically as close as possible to the chip to obtain maximum benefit. We recommend placing a 0.1µF capacitor at each power-ground pin pair (X total) for high frequency decoupling and including one 10 µF capacitor for local low frequency decoupling. Each of the three VREF IN pins should also be decoupled by a 0.1µF capacitor.

The part should be located on a solid ground plane and output trace lengths should be short (<1 inch) to minimize transmission line effects. This will avoid the need for termination resistors on the output bus and reduces the load capacitance that needs to be driven, which in turn minimizes on-chip noise due to heavy current flow in the outputs. We have obtained optimum performance on our evaluation board by tying all V_{DD} pins to a quiet analog power supply system, and tying all GND pins to a quiet analog system ground.

Minimum Encode Rate

The minimum sampling rate for the AD9483 is 10 MHz for the standard 140 MSPS version. To achieve this sampling rate, the Track/Hold circuit employs a very small hold capacitor. When operated below the minimum guaranteed sampling rate, the T/H droop becomes excessive. This is first observed as an increase in offset voltage, followed by degraded linearity at even lower frequencies.

Lower effective sampling rates may be easily supported by operating the converter in Dual Port output mode and using only one output channel. A majority of the power dissipated by the AD9483 is static (not related to conversion rate) so the penalty for clocking at twice the desired rate is not high.

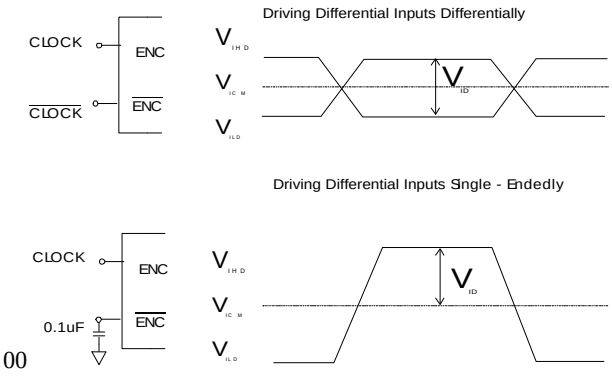
Digital Inputs

SNR performance is directly related to the sampling clock stability in A/D converters, particularly for high input frequencies and wide bandwidths

ENCODE and Data Select (DS) can be driven differentially or single-ended. For single-ended operation, the complement inputs (ENCODE\, DS\) are internally biased to $V_{DD}/3$ (~1.5V) by a high-impedance on-chip resistor divider (Figure 5), but they may be externally driven to establish an alternate threshold if desired. A 0.1µF decoupling capacitor to ground is sufficient to maintain a threshold appropriate for TTL or CMOS logic.

When driven differentially, ENCODE and DS will accommodate differential signals centered between 1.5V and 4.5V with a total differential swing ≥800mV (V_{ID} ≥400mV).

Note the 6-diode clock input protection circuitry in Figure 5. This limits the differential input voltage to ~±2.1V. When the diodes turn on, current is limited by the 300Ω series resistor. Exceeding 2.1V across the differential inputs will have no impact on the performance of the converter, but be aware of the clock signal distortion that may be produced by the nonlinear impedance at the converter.



00

Figure 34. Input Signal Level Definitions

ADC Gain Control

Each of the three ADC channels has independent gain control. The full scale signal amplitude for a given ADC is set by the dc voltage on its Vref In pin. The equation relating the full scale amplitude to Vref In is as follows: FS = (0.4)*(Vref In). The three ADC's are optimized for a full scale signal amplitude of 1V, but will accommodate up to +/- 10% variation.

ADC Offset Control

The offset for each of the three ADC's can be independently controlled. For a single ended analog input where the analog input is connected to a reference, offset can be adjusted simply by adjusting the dc voltage of the reference. For differential analog inputs, the user must provide the offset in their signal. Offset can be adjusted up or down as far as the common mode input range will allow.

Power Dissipation

Power dissipation for the AD9483 has two components, V_{CC} and V_{DD}. Power dissipation from V_{CC} is relatively constant for a given supply voltage, whereas power dissipation from V_{DD} can vary greatly. V_{CC} supplies power to the analog circuitry. V_{DD} supplies power to the digital outputs and can be approximated by the following equation:

$$P(V_{DD}) = ½C*V^2*F*N$$

C = Output Load Capacitance

V = VDD Supply Voltage

F = Encode Frequency

N = Number of Outputs Switching

Nominally, C = 10pF, V = 3.3V, F = 140 MSPS, and N = 26. N comes from the 24 output bits plus 2 clock outputs, $P(V_{DD})$ = 197 mW

Powerdown

The Powerdown (PD) function allows users to reduce power dissipation when output data is not required. A TTL/CMOS HIGH signal on pin 76, shuts down most of the chip and brings the total power dissipation to less than 100mW. The internal bandgap voltage reference remains active during power-down mode to minimize reactivation time. If the power-down function is not desired, the PD pin should be tied to ground or held to a TTL/CMOS LOW level.

Bandgap Voltage Reference

The AD9483 internal reference, Vref OUT (pin 97), provides a simple, cost effective reference for many applications. It exhibits reasonable accuracy and excellent stability over power supply and temperature variations. The reference output can be used to set the three ADC's gain and offset. The reference is capable of providing up to 1mA of additional current beyond the requirements of the AD9483.

As the ADC gain and offset are set by the reference inputs, some applications may require a reference with greater accuracy or temperature performance. In these cases, an external reference may be connected directly to the Vref In pins. Vref OUT if unused should be left floating. Note, each of the three Vref In pins will require up to 1mA of current.

Modes of Operation

The AD9483 has three modes of operation, Single Channel output mode, and a half speed Dual Channel output mode with two possible data formats, interleaved or parallel. Two pins control which mode of operation the chip is in, pin 74 Output Mode Select (OMS) and pin 75 Interleaved/Parallel Select (I/P). The following chart shows the configuration required for each mode:

MODE	OMS	I/P
Dual Channel -Parallel	LOW	LOW
Dual Channel - Interleaved	LOW	HIGH
Single Channel	HIGH	DONT CARE

Table 2. Output Mode Selection

Demuxed Outputs Mode

In demuxed mode, (pin 74 OMS = LOW), the ADC output data are alternated between the two output ports (port A and port B). This sets the data output rate at a single port to 1/2 the rate of ENCODE, and facilitates conversion rates up to 140 MSPS. Demuxed output mode is recommended for guaranteed operation above 100 MSPS, but may be enabled at any specified conversion rate.

Two data formats are possible in Dual Channel output mode, parallel data out and interleaved data out. Pin 75 I/P should be LOW for parallel format and HIGH for interleaved format.

Figures One and Two shows the timing requirements for each format. Note that the Data Sync input , (DS), is required in Dual Channel output mode for both formats. The section on Data Sync describes the requirements of the Data Sync input.

As shown in Figures One and Two, when using the interleaved data format, a sample is taken on an ENCODE rising edge N. The resulting data is produced on an output port following the fifth rising edge of ENCODE after the sample was taken, (five pipeline delays). The following sample, (N+1), will be produced on the opposite port, also five pipeline delays after it was taken. The state of Clkout when the sample was taken will determine which port the data will come out. If Clkout was LOW then the data will come out port A. If Clkout was HIGH then the data will come out port B.

In order to achieve parallel data format on the two output data ports, the data is internally aligned. This is accomplished by adding an extra pipeline delay to just the A data port. Thus data coming out port A will have six pipeline delays and data coming out port B will have five pipeline delays. As with the interleaved format, the state of Clkout when a sample is taken will determine which port the data will come out. If Clkout was LOW, then the data will come out port A. If Clkout was HIGH, then the data will come out port B.

Data Sync

The data sync input, DS, is required to be driven for most applications to guarantee which output port a given sample will appear. When DS is held high the ADC data outputs and clock outputs do not switch -they are held static. Synchronization is accomplished by the assertion (falling edge) of DS , within the timing constraints T_{SDS} and T_{HDS} relative to an encode rising edge. (On initial synchronization T_{HDS} is not relevant.) If DS falls T_{SDS} before a given encode rising edge N, the analog value at that point in time will be digitized and available at port A five cycles later (interleaved mode) . The very next sample, N+1, will be sampled by the next rising encode edge and available at port B five cycles after that encode edge (interleaved mode). In dual parallel mode the A port has a six cycle latency, the B port has a five cycle latency as described in demuxed outputs mode section.

DS can be asserted once per video line if desired by using the horizontal sync signal (HSYNC). The start of HSYNC should occur after the end of active video by at least the chip latency. The HSYNC frontporch is usually much greater than this in a typical SXGA system If this is true in a given system then DS can be reset high by the HSYNC leading edge (the samples at that point should not be required in a typical system). DS can then be reasserted (brought low) , by triggering off of HSYNC trailing edge -observing T_{SDS} of the next rising encode edge. The first pixel data (on A port) would be available 5 cycles after the first rising encode after HSYNC goes high.

It is possible to use the phase of the data clock outputs and software programming to accommodate situations where DS is not driven. The data clock outputs (CLKOUT and CLKOUT/) can be used to determine when data is valid on the output ports. In these cases DS should be grounded and DS/ left floating or connected to V_{CC}. If CLKOUT was low when a given sample was taken, the digitized value will be available on port A 5 cycles later. Data Sync has no effect when Single Channel Mode is selected, it should be grounded

Figure 2. Dual Channel Timing Diagram shows how to use DS properly. The DS rising edge does not have any special timing requirements except that no data will come out of either port while it is held HIGH. The falling edge of DS must however meet a minimum setup and hold time with respect to the rising edge of ENCODE (as shown in Figure 2).

Single Channel Outputs Mode

In Single Channel mode, (pin 74 OMS = HIGH), the timing of the AD9483 is similar to any high-speed ADC (Figure One). A sample is taken on every rising edge of ENCODE, and the resulting data is produced on the output pins following the fourth rising edge of ENCODE after the sample was taken, (four pipeline delays). The output data are valid tPD after the rising edge of ENCODE, and remain valid until at least tV after the next rising edge of ENCODE.

The maximum conversion rate in this mode should be limited to 100 MSPS. This is recommended because the guaranteed output data valid time minus the propagation delay is only 4ns at 100 MSPS. This is about as fast as standard logic is able to capture the data with reasonable design margins. The AD9483 will operate faster in this mode if the user is able to capture the data.

When operating in Single Channel mode, all data comes out the A ports while the B ports are held static in a random state.

Data Clock Outputs

The data clock outputs will switch at two potential frequency levels. In Single Channel Mode, where all data comes out of port A at the full ENCODE rate, the data clock outputs switch at the same frequency as the ENCODE. In Dual Channel Mode, where the data alternates between the two ports, each of which operate at 1/2 the ENCODE rate, the data clock outputs also switch at 1/2 the ENCODE rate.

The data clock outputs have two potential purposes. The first is to act as a latch signal for capturing output data. In order to do this, simply drive data latches with the appropriate data clock output. The second use is in Dual Channel data mode to help determine out of which data port data will come out. Refer to Figure Two for a complete timing diagram, but in this mode, a rising edge on data clock will correspond to data switching on data port B.

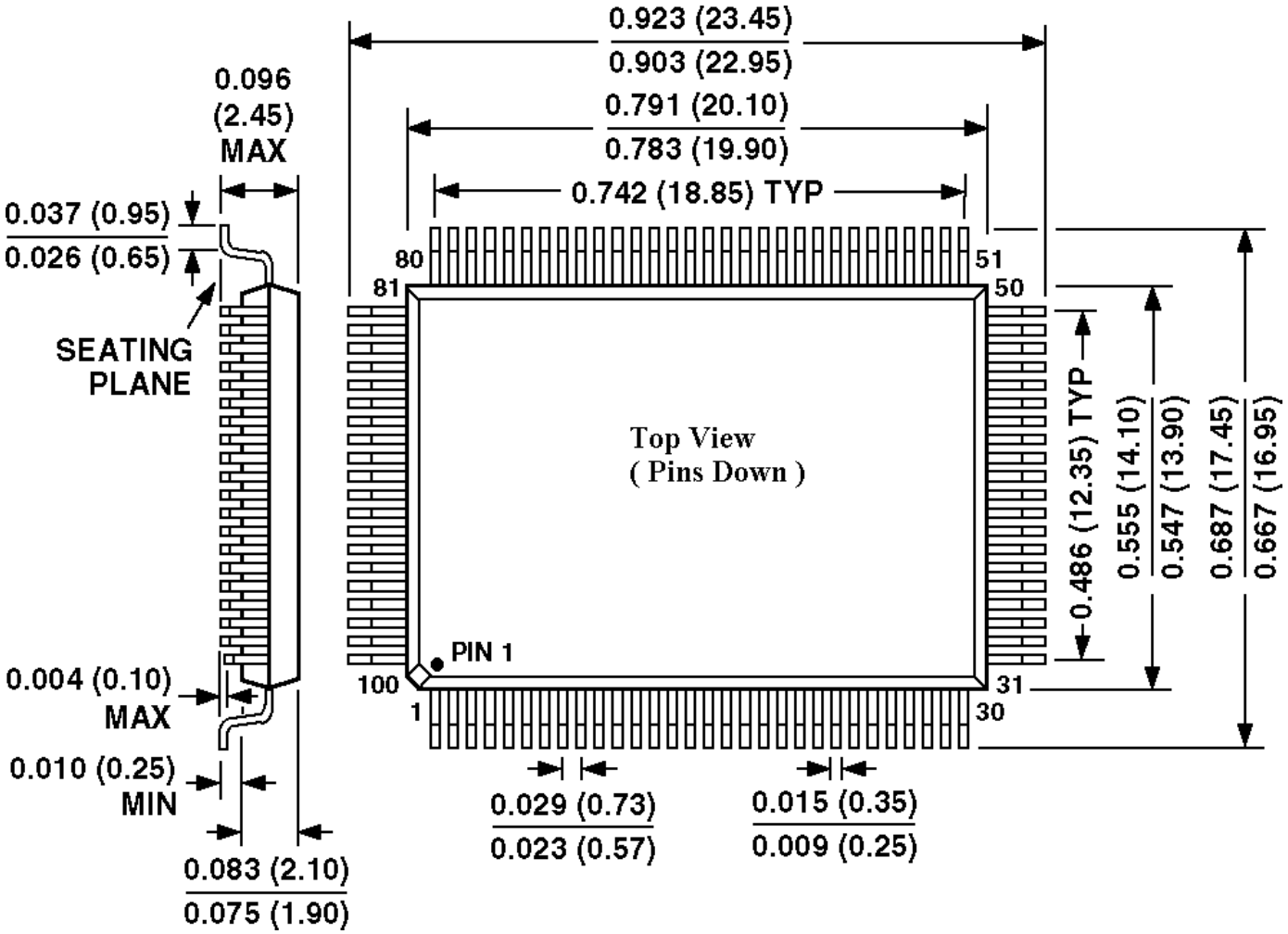
Layout and Bypassing Considerations

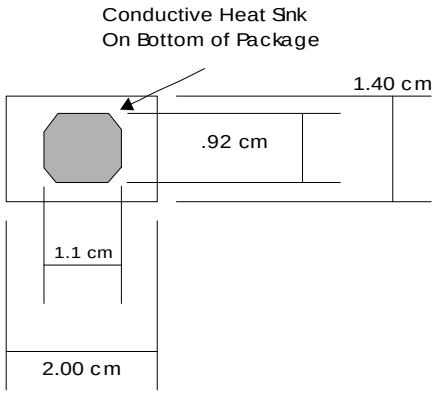
Proper high speed layout and bypassing techniques should be used with the AD9483. Each V_{CC} and V_{DD} power pin should be bypassed as close to the pin as possible with a 0.01 to 0.1 uF capacitor Also, one 10uF capacitor to ground should be used per supply per board. The VREF OUT pin and each of the three VREF IN pins should also be bypassed with a 0.01 to 0.1 uF capacitor to ground.

A single, substantial, low impedance ground plane should be place under and around the AD9483. Try to maximize the distance between the sensitive analog signals, (AIN, VREF), and the digital signals. Capacitive loading on the digital outputs should be kept to a minimum. This can be facilitated by keeping the traces short and in the case of the clock outputs by driving as few other devices as possible. Socketing the AD9483 should also be avoided. Try to match trace lengths of similar signals to avoid mismatches in propagation delays, (the encode inputs, analog inputs, digital outputs).

Power Supplies

At power up, V_{CC} must come up before V_{DD}. V_{CC} is considered the Converter Supply, nominally 5.0V (+/-5%) V_{DD} is considered Output Power Supply, nominally 3.3V (+/-10%) or 5.0V (+/-5%). At power off, V_{DD} must turn off first. Failure to observe the correct power supply sequencing may damage this device.





Note: The AD9483KS package uses a copper insert to help dissipate heat and ensure reliable operation over the full 0-85 deg C temperature range. This copper insert is exposed on the underside of the device. It is recommended that during the design of the PC board that no through-holes or signal traces be placed under the AD9483 that could come in contact with the copper insert. Commonly accepted board layout practices for high-speed converters specify that only ground planes shall be located under these devices to minimize noise or distortion of video signals.