10–Bit, 65/80/105 MSPS 3V A/D Converter

Preliminary Technical Data 2/1/00 AD9214

The AD9214 is an 10-bit monolithic sampling analog–to–digital converter with an on–chip track–and–hold circuit and is optimized for low cost, low power, small size and ease of use. The product operates up to 105 Msps conversion rate with outstanding dynamic performance over its full operating range.

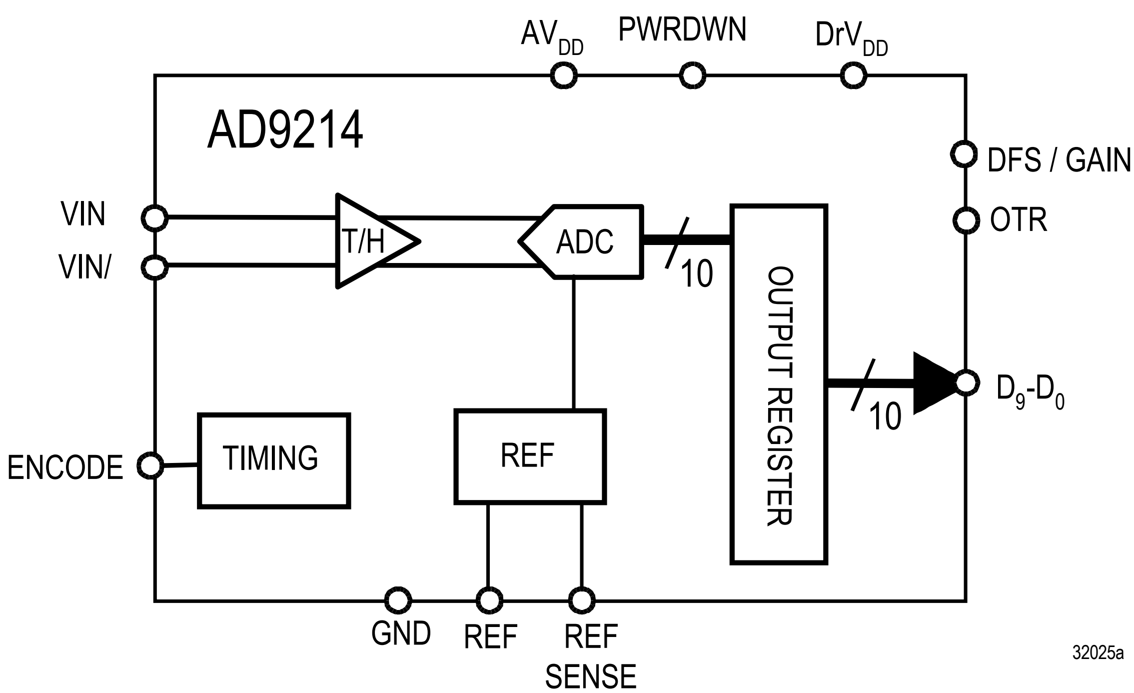
The ADC requires only a single 3.3V (2.7V to 3.6V) power supply and an encode clock for full–performance operation. No external reference or driver components are required for many applications. The digital outputs are TTL/CMOS compatible and a separate output power supply pin supports interfacing with 3.3V or 2.5V logic.

The clock input is TTL/CMOS compatible. In the power down state, the digital outputs are driven to a high-impedence state. A gain option allows support for either 1Vp-p or 2Vp-p (-65) analog signal input swing.

Fabricated on an advanced CMOS process, the AD9214 is available in a 28 pin surface mount plastic package (28 SSOP) specified over the industrial temperature range (–40°C to +85°C).

FEATURES
10–Bit, 65, 80, and 105 Msps ADC
Low Power:
- 170 mW at 65 Msps with Fin = 10.3 MHz
- 250 mW at 105 Msps with Fin = 10.3 MHz
On–Chip Reference and Track/Hold
300 MHz Analog Bandwidth
SNR = 56dB @ 41MHz
1Vp–p or 2Vp-p Analog Input Range option
Single +3.3V Supply Operation (2.7V – 3.6V)
Two's compliment data format option
Power Down mode = 5mW

APPLICATIONS
Battery Powered Instruments
Hand-Held Scopemeters
Low Cost Digital Oscilliscopes
Communications
Ultrasound Equipment



REV. PrB

One Technology Way, P.O Box 9106, Norwood, MA 02062–9106, USA
Tel: 617/329–4700 Fax: 617–326–8703

AD9214—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_{DD} = 3.0V, Input Voltage of 1Vp-p; external reference, unless otherwise noted)

Parameter	Temp	Test Level	AD9214BRS-105 Min	AD9214BRS-105 Typical	AD9214BRS-105 Max	AD9214BRS-80 Min	AD9214BRS-80 Typical	AD9214BRS-80 Max	AD9214BRS-65 Min	AD9214BRS-65 Typical	AD9214BRS-65 Max	Units
RESOLUTION				10			10			10		bits
DC ACCURACY												
Differential Nonlinearity	+25°C	I		±0.5			±0.5			±0.5		LSB
	Full	VI										LSB
Integral Nonlinearity	+25°C	I		±0.75			±0.75			±0.75		LSB
	Full	VI										LSB
No Missing Codes	Full	VI		GNT			GNT			GNT		
Gain Error [1]	+25°C	I		±2.5			±2.5			±2.5		% FS
	Full	VI										% FS
Gain Tempco[1]	Full	VI										ppm/°C
ANALOG INPUT												
Input Voltage Range (differential)	Full	V		1 or 2			1 or 2			1 or 2		V p–p
Common Mode Voltage	Full	V										V
Input Offset Voltage	+25°C	I		±10			±10			±10		mV
	Full	VI										mV
Reference Voltage	Full	VI		1.25			1.25			1.25		V
Input Resistance	+25°C	I										kΩ
	Full	VI										kΩ
Input Capacitance	+25°C	V		2			2			2		pF
Input Bias Current	+25°C	I										µA
	Full	VI										µA
Analog Bandwidth, Full Power	+25°C	V		300			300			150		MHz
SWITCHING PERFORMANCE												
Maximum Conversion Rate	Full	VI	105			80			65			Msps
Minimum Conversion Rate	+25°C	IV			10			10			10	Msps
Encode Pulse Width High(t_{EH})	+25°C	IV	3.8		1000	5.0		1000	7.0		1000	ns
Encode Pulse Width Low(t_{EL})	+25°C	IV	3.9		1000	5.0		1000	7.0		1000	ns
Aperature Delay(t_A)	+25°C	V		900			900			900		ps
Aperature Uncertainty(Jitter)	+25°C	V		5			5			5		ps rms
Output Valid Time(t_V) [2]	Full	VI		5.0			5.5			6.0		ns
Output Propagation Delay(t_{PD}) [2]	Full	VI		5			5			5		cycles
Power Up Time	+25°C	IV		60			75			105		ns
DIGITAL INPUTS												
Logic "1" Voltage	Full	VI	2.0			2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8		0.8		V
Logic "1" Current	Full	VI			±1			±1		±1		µA
Logic "0" Current	Full	VI			±1			±1		±1		µA
Input Capacitance	+25°C	V		4.5			4.5				4.5	pF
DIGITAL OUTPUTS												
Logic "1" Voltage	Full	VI	2.45			2.45			2.45			V
Logic "0" Voltage	Full	VI			0.05			0.05			0.05	V
POWER SUPPLY												
Power Dissipation[5]	Full	VI		250			240			170		mW
Power-Down Dissipation	Full	VI		5	10		5	10		5	10	mW
Power Supply Rejection Ratio (PSRR)	+25°C	I			14			14			14	mV/V

Parameter	Temp	Test Level	AD9214BRS-105 Min	AD9214BRS-105 Typical	AD9214BRS-105 Max	AD9214BRS-80 Min	AD9214BRS-80 Typical	AD9214BRS-80 Max	AD9214BRS-65 Min	AD9214BRS-65 Typical	AD9214BRS-65 Max	Units
DYNAMIC PERFORMANCE[3]												
Transient Response	+25°C	V		tbf			tbf			tbf		ns
Overvoltage Recovery Time	+25°C	V		tbf			tbf			tbf		ns
Signal-to-Noise Ratio (SNR)												
(Without Harmonics)				58			58			58		dB
fin = 10.3 MHz	+25°C	I		57			57					dB
fin = 41 MHz	+25°C	I		56								
Singal-to-Noise Ratio (SINAD)												
(With Harmonics)				56			56			56		dB
fin = 10.3 MHz	+25°C	I		56			56					dB
fin = 41 MHz	+25°C	I		55								
Effective Number of Bits												
fin = 10.3 MHz	+25°C	V		9.0			9.0			9.0		bits
fin = 41 MHz	+25°C	V		9.0			9.0					bits
2nd Harmonic Distortion												
fin = 10.3 MHz	+25°C	I		70			tbf			tbf		dBc
fin = 41 MHz	+25°C	I		66			tbf					dBc
3rd Harmonic Distortion												
fin = 10.3 MHz	+25°C	I		66			tbf			tbf		dBc
fin = 41 MHz	+25°C	I		64			tbf					dBc
Two-Tone Intermod Distortion (IMD)												
fin = 10.3 MHz	+25°C	V		64			tbf			tbf		dBc
fin = 41 MHz	+25°C	V		tbf			tbf					dBc

NOTES

1. Gain error and gain temperature coefficient are based on the ADC only (with a fixed 1.25V external reference).
2. t_V and t_{PD} are measured from the 1.5V level of the ENCODE input to the 10% / 90% levels of the digital outputs swing. The digital output load during test is not to exceed an AC load of 10pF or a DC current of +/-40µA.
3. SNR / harmonics based on an analog input voltage of –0.7 dBfs referenced to a 1.0Vp-p full–scale input range for the 80 and 105 Msps versions and to a 2.0Vp-p for the 65 Msps version.
4. Digital supply current based on V_{DD} = +2.5V output drive with <10pF loading under dynamic test conditions.
5. Power dissipation is measured under the following conditions: Analog input of 10.3 MHz, sine wave.

ORDERING GUIDE

Model	Temperature Range	Package Option
AD9214BRS-65,-80,-105	–40°C to +85°C	RS–28
AD9214-EVAL	+25°C	Evaluation Board

*RS = 28 pin Small Shrink Outline Package.

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at +25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at +25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

ABSOLUTE MAXIMUM RATINGS*

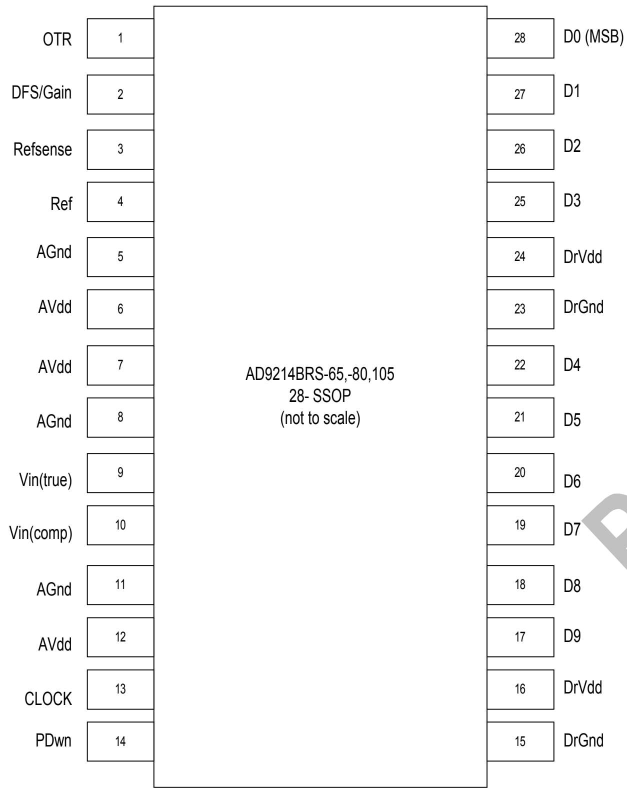
V_D ,V_{DD} .... +4 V
Analog Inputs .... -0.5V to V_D + 0.5 V
Digital Inputs .... -0.5V to V_{DD} + 0.5 V
VREF IN .... -0.5V to V_D + 0.5 V
Digital Output Current .... 20 mA
Operating Temperature .... –55°C to +125°C
Storage Temperature .... –65°C to +150°C
Maximum Junction Temperature .... +175°C
Maximum Case Temperature .... +150°C

* Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

PIN DESCRIPTIONS

Pin Number AD9214BRS-65, -80, -105	Name	Function
1	OTR	Out of Range indicator.
2	DFS/Gain	Data format select and Gain mode select. (Set HIGH to AV_{DD} = Two’s complement, 1Vp-p support; Set LOW to AGND = Offset binary, 1Vp-p support; Set to Refout = Two’s Complement, 2Vp-p support; Floating = Offset binary, 2Vp-p support)
3	REFSENSE	Reference input mode for ADC (+1.25V typ, ± 10%). (Set HIGH to AVDD = disabled. A clean and accurate 1.25V external reference is required and is connected to REF; Set LOW to AGND = internal reference is used and REF should be bypassed with 0.1 µF to ground.
4	REF	Interal Reference Output (+1.25V typ); Bypass with 0.1 µF to ground. Or, external reference input. See Pin #3 function.
5,8,11	AGND	Analog ground.
6,7,12	AV_{DD}	Analog +3V power supply.
9	VIN	Analog Input for ADC
10	VIN/	Analog Input for ADC (Can be left open if operating in single-ended mode but recommend connection to a 0.1µF capacitor and a 25Ω resistor in series to ground for better input matching.)
13	CLOCK	Encode Clock for ADC (ADC samples on rising edge of CLOCK)
14	PWRDN	Power-Down function select; Logic HIGH for Power-down Mode (digital outputs go to high impedance state)
15,23	DrGND	Digital output ground.
16,24	DrV_{DD}	Digital output power supply. Nominally +2.5V to +3.6V.
17-22,25-28	D0(msb) - D9	Digital Outputs of ADC

PIN CONFIGURATION



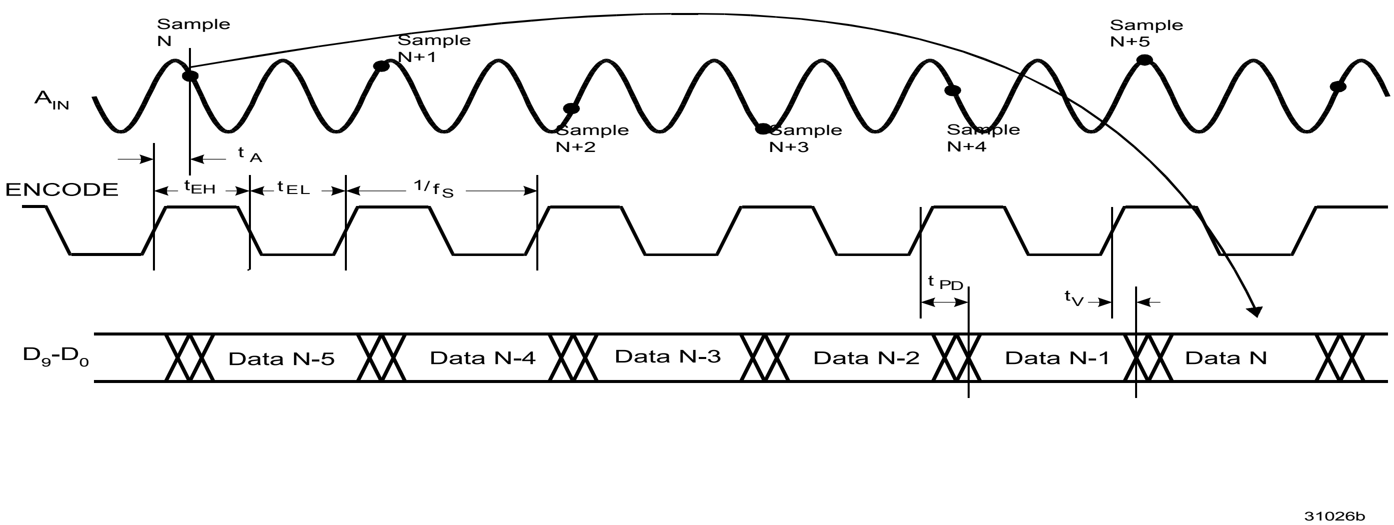


Figure 1. Timing Diagram

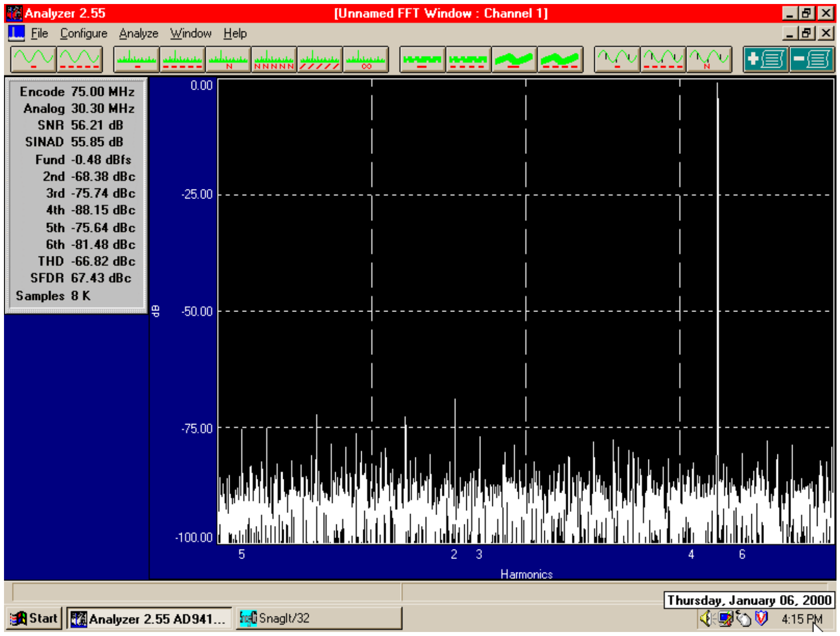


Figure 2. Preliminary Performance; Fs=75Msps, Fin=30MHz, Differential Input

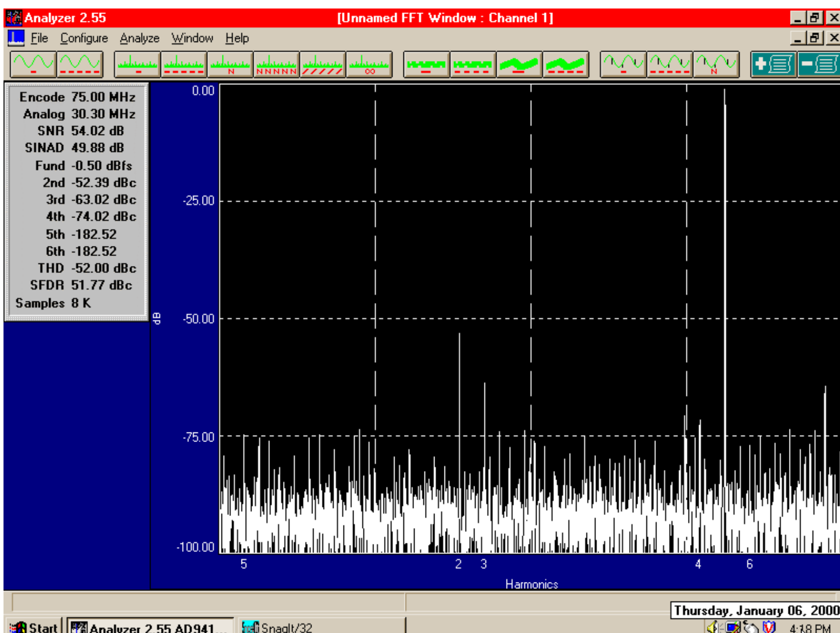


Figure 3. Preliminary Performance; Fs=75Msps, Fin=30MHz, Single-ended Input

Step	A_{IN} – A_{IN}\	Offset Binary Output	Two's Compliment Output
1024	0.512	1111 1111 11	0111 1111 11
•	•	•	•
•	•	•	•
512	0.002	1000 0000 00	0000 0000 00
511	-0.002	0111 1111 11	1111 1111 11
•	•	•	•
•	•	•	•
0	-0.512	0000 0000 00	1000 0000 00

Table 1. Output Coding (VREF = +1.25 and Input range of 1Vp-p)

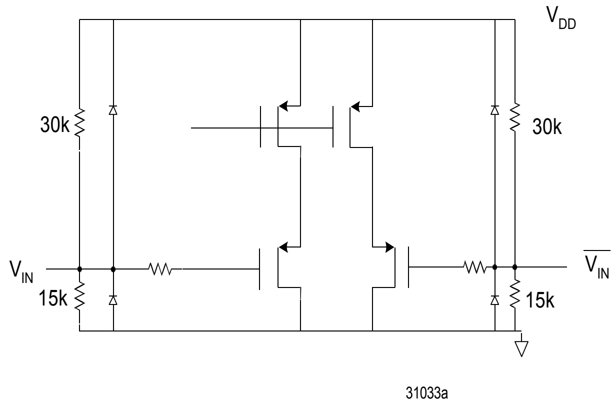


Figure 4. Equivalent Analog Input Circuit

(Tbd)

Figure 5. Equivalent Reference Input Circuit

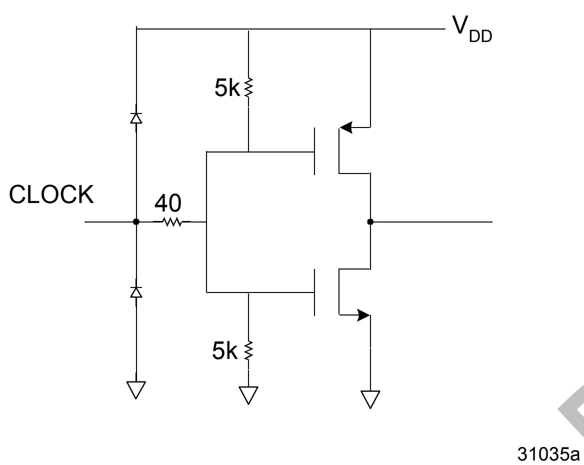


Figure 6. Equivalent Encode Input Circuit

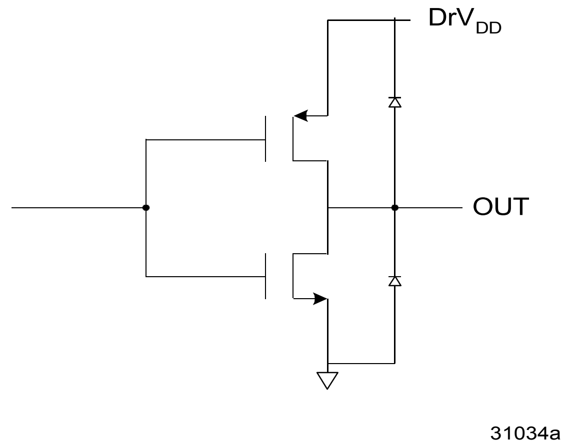


Figure 7. Equivalent Digital Output Circuit

(Tbd)

Figure 8. Equivalent Reference Output Circuit

APPLICATION NOTES

THEORY OF OPERATION

The AD9214 architecture is a bit per stage pipeline type converter utilizing switch capacitor techniques. These stages determine the 7 MSBs and drive a three bit flash. Each stage provides sufficient overlap and error correction allowing optimization of comparator accuracy. The input buffer is differential and both inputs are internally biased. This allows the most flexible use of AC or DC and differential or single ended input modes. The output staging block aligns the data, carries out the error correction and feeds the data to output buffers. The output buffers are powered from a separate supply allowing adjustment of the output voltage swing and during powerdown, go to a high impedance state.

USING THE AD9214

ENCODE Input

Any high-speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A Track/Hold circuit is essentially a mixer. Any noise, distortion, or timing jitter on the clock will be combined with the desired signal at the A/D output. For that reason, considerable care has been taken in the design of the ENCODE input of the AD9214, and the user is advised to give commensurate thought to the clock source. The ENCODE input is fully TTL/CMOS compatible.

Digital Outputs

The digital outputs are TTL/CMOS compatible for lower power consumption. The format can be selected for either offset binary or two's complement. During powerdown, the outputs transistion to a high impedance state. It takes approximately 15 clock cycles after disabling powerdown to restore full operation.

Analog Input

The analog input to the AD9214 is a differential buffer. For best dynamic performance, impedances at VIN and VIN\ should match.

Special care was taken in the design of the analog input section of the AD9214 to prevent damage and corruption of data when the input is overdriven. The nominal input range is 1.0 Vp–p for the 80 and 100 Msps versions, but can support a 2.0Vp-p input range at a slight degradation in performance. Care has been taken to optimize the 2Vp-p input range for the 65 Msps version, but a 1Vp-p is also supported.

Voltage Reference

A stable and accurate 1.25 V voltage reference is built into the AD9214 (VREF OUT) for the 80 and 100 Msps versions. A stable and accurate 2.25 V voltage reference is built into the 65 Msps version. In normal operation, the internal reference is used by strapping Pins 3 and 4 together.

The input range can be adjusted by varying the reference voltage applied to the AD9214. No appreciable degradation in performance occurs when the reference is adjusted ±5%. The full–scale range of the ADC tracks reference voltage changes linearly.

Timing

The AD9214 provides latched data outputs, with five pipeline delays. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the encode command *(Figure 1. Timing Diagrams)*. The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9214; these transients can detract from the converter's dynamic performance.

The minimum guaranteed conversion rate of the AD9214 is 10 MSPS. At clock rates below 10 MSPS, dynamic performance will degrade.

ERRATA

Date	Revision	Modification
4/2/99	R0.5	Updated Gain Error, Input Offset voltage, Reference voltage (-65), total power dissipation, and SNR (-105).
7/7/99	R0.6	Updated block diagram to reflect pin names. Updated part number and package to 28-SSOP.
9/15/99	R0.7	Defined pinouts, included some equivalent circuits and added applications section. Updated power dissipation, reference voltage on –65, t_{EH} and t_{EL}, and t_V.
9/28/99	R0.8	Changed REFOUT pin name to REF and clarified definition.
1/31/00	R0.9	Updated Tv and units on prop delay. Inserted prelim performance. Updated SNR on front page and specs (56dB)