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DC to 2.5 GHz High IP3 Active Mixer

Preliminary Technical Data AD8343

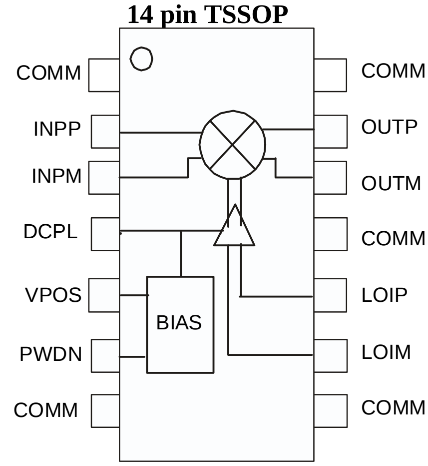
FEATURES

- **High Performance Topology**
- **Broadband Operation to 2.5 GHz**
- **Conversion Gain: +6 dB**
- **Input IP3: +16.8 dBm**
- **LO Drive: -10 dBm**
- **Noise Figure: 12.4 dB**
- **Input P1dB: +11 dBm**
- **Differential LO, IF and RF Ports**
- **50Ω LO Input Impedance**
- **Single Supply Operation: 5V @ 40 mA Typical**
- **Power down mode**

APPLICATIONS

- **Cellular Basestations**
- **Wireless LAN**
- **Satellite Converters**
- **Sonet/SDH Radio**
- **Radio Links**
- **RF Instrumentation**

Functional Block Diagram
14 pin TSSOP



PRODUCT DESCRIPTION

The AD8343 is a monolithic, high-performance broadband, active mixer. It is intended for use in conversion applications demanding very low intermodulation distortion with moderate noise figure and power consumption. The AD8343 is optimized and fully characterized as a receive mixer, but is equally suitable in transmitter applications. It's conversion gain of typically +6 dB, coupled with an integrated LO driver reduces component count in transceiver designs.

The amplification provided by the LO interface is internally amplified allows low LO drive levels. In addition to amplifying the VCO generator, this also minimizes component requirements and simplifies board layout. The 50Ω differential input LO port may be driven by either balanced or single-ended signals.

With open-emitter differential inputs, the AD8343 may be interfaced directly to a differential filter or may be driven through a balun (transformer) to provide a balanced drive from a single-ended signal chain.

The open-collector differential outputs may be used to drive a differential IF signal chain or may be converted to a single-ended signal through the use of a matching network or transformer. The outputs may swing ± 1 V centered on the VPOS supply voltage.

The internal bias and LO driver circuitry typically consume 15mA of current. An external resistor is used to set the mixer core current for required performance resulting in a total current of 20 mA to 50 mA. This corresponds to power consumption of 100 to 250 mW with a single 5 V supply.

The AD8343 is fabricated on Analog Devices' proprietary, high performance 25 GHz RF25 silicon bipolar IC process. The AD8343 is available in a 14-pin TSSOP package. It operates over-a -40 to +85 C temperature range. An evaluation board is available.

AD8343 –SPECIFICATIONS

Parameter	Conditions	Min	Typ	Max	Units
Input Interface					
DC Bias Voltage	Internally generated voltage.		1.26		V
Port Impedance			~ 10		Ω real
Output Interface					
DC Bias Voltage	Externally applied voltage.		VPOS		V
Port Impedance			~ 10k		Ω real
LO Interface					
LO Input Power		-12	-10	0	dBm
DC Bias Voltage	Internally generated voltage.		400		mV
Port VSWR				2:1	
Power-down Interface					
Power-down Threshold		TBD	V_{POS}-900mV	TBD	V
Power-down Response Time	Time delay following HI to LO transition until device meets full specification.		5		µs
PWDN Input Bias Current	PWDN=0 V		85		µA
	PWDN=5 V		0		µA
Power Supply					
Supply Voltage Range		4.5	5.0	5.5	V
Operating Current	R1=33 Ω		40	TBD	mA
	Over Temperature	TBD		TBD	mA
Powered-down Current			10	TBD	µA
	Over Temperature	TBD		TBD	µA

AD8343 –Typical Performance Tables

Typical AC Performance at Ambient

Input Frequency	Output Frequency	Conversion Gain	SSB Noise Figure	Input IP3	Input 1dB Compression Point
400	70	TBD			
1750	170	6 dB	12.4 dB	16.8 dBm	5.5 dBm
1900	425	TBD			
2400	250				
2400	425				
150	900				
150	1900				

Typical Isolation Performance at Ambient

Input Frequency	Output Frequency	LO to Input Isolation	LO to Output Isolation	2•LO to Output Isolation	Input to Output Isolation
400	70	TBD			
1750	170	TBD	-45 dB	-15 dB	-45 dB
1900	425	TBD			
2400	250				
2400	425				
150	900				
150	1900				

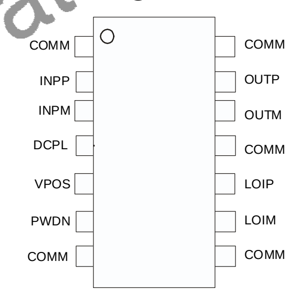
Low side LO injection used for typical performance.

Absolute Maximum Ratings *

Supply Voltage .... 5.5 V
Input power differential (re: 50Ω, 5.5 V) .... +25 dBm
Input power single-ended (re: 50Ω, 5.5 V) .... +19 dBm
Internal Power Dissipation (TSSOP) .... TBD mW
Θ_{JA} (TSSOP) .... TBD°C/W
Maximum Junction Temperature .... +125°C
Operating Temperature Range .... -40°C to +85°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature Range (Soldering 60 sec) .... +300°C

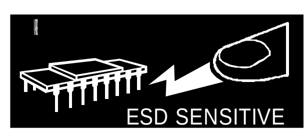
* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

Pin Configuration

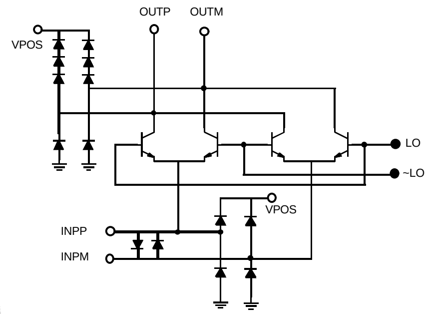
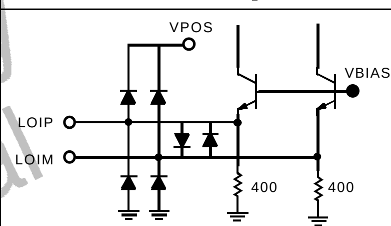
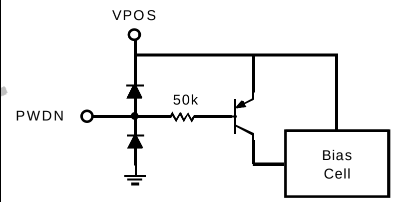
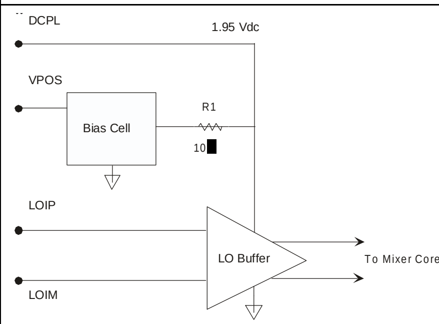


CAUTION

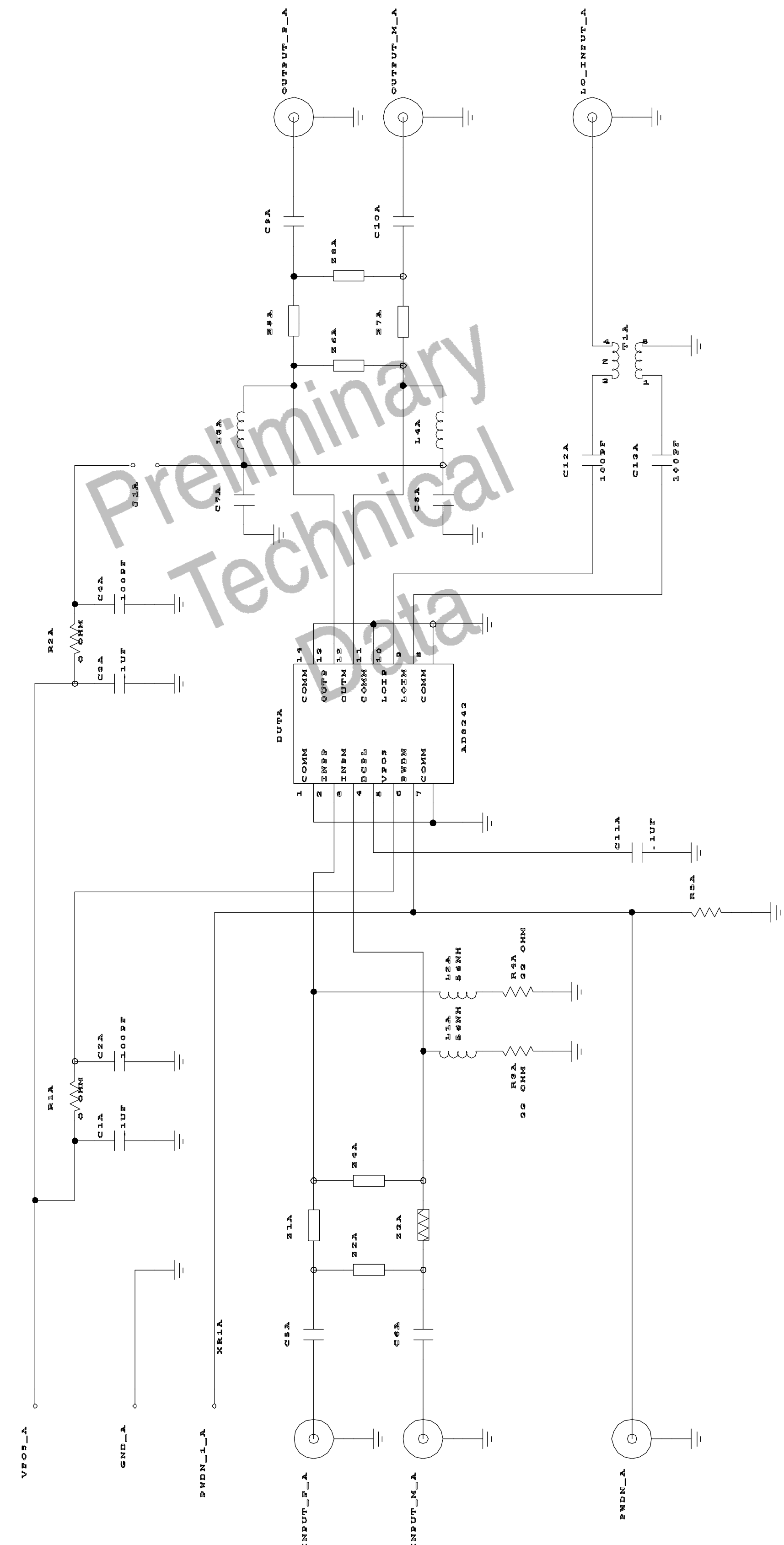
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8343 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy [>250 V HBM] electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Pin Function Descriptions

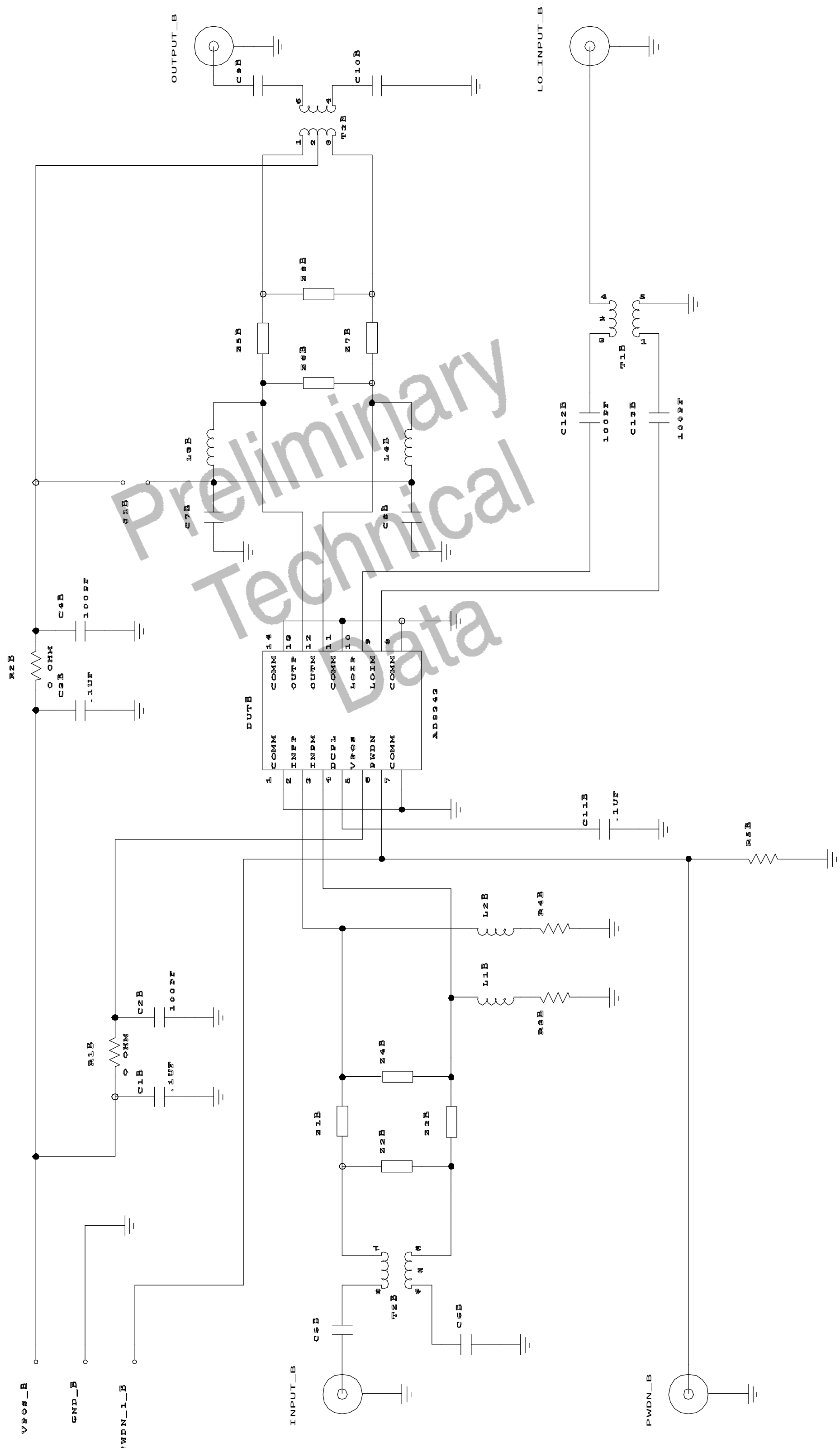
TSSOP	Name	Function	Simplified Interface Schematic
2, 3 12, 13	INPP/INPM OUTP/OUTM	Differential input pins. Need to be AC coupled and DC biased. Open collector differential output pins. Need to be AC coupled and DC biased.	
9, 10	LOIP/LOIM	Differential local oscillator (LO) input pins. Need to be AC coupled.	
6	PWDN	Power-down interface. Connect pin to ground for normal operating mode. Connect pin to supply for power-down mode.	
4	DCPL	Internal bias rail decoupling capacitor connection.	
5	VPOS	Positive supply voltage (V_{POS}), +4.5 to +5.5 V. Ensure proper supply bypassing for proper device operation as shown in Figure 1.	
1, 7, 8, 11, 14	COMM	Device common connected to paddle. Connect to low impedance circuit ground.	

AD8343 Evaluation Board – Circuit A



The A side of the evaluation board is meant to enable differential matching of the input and output ports.

Evaluation Board – Circuit A



The B side of the evaluation board is meant to be populated with the differential match achieved on the A side of the board.

Notes on Matching of the AD8343

The AD8343 requires matching on its low impedance input port and high impedance output port to achieve optimal performance. In addition to the return loss requirements, a balanced source waveform is required to drive the input and a balanced load is essential for optimal performance. A further requirement of the matching for these ports is to provide DC current for the mixer core. The decision to use transformers on this board was based on ease of evaluation. There are numerous discrete circuits that can produce the balanced waveforms, impedance match and noise performance that is required for this circuit. These discrete circuits can be employed to further reduce the component cost of the mixer. The LO port is nearly 50 Ω (< 2:1 VSWR up to 2.5 GHz) broadband and no matching is typically required.

For device evaluation, a 1:1 balun is used to generate a balanced waveform and reactive matching components (Z7 through Z10) are placed between the balun and the AD8343 to provide for a power match. Because these matching components are placed on the differential side of the balun, differential matching techniques must be employed. The fundamental concept of a virtual ground for differential signals provides some clarity to the matching process. When considering component Z9, remember that this is simply a shunt component between the two ports with a virtual ground dividing the component in half. This would mean that inductor values are doubled and capacitive values are halved from normal single-ended theory.

This differential impedance measurement is made easier through the use of a technique presented in an article written by Lutz Konstroffer in *RF Design*, January 1999, entitled "Finding the Reflection Coefficient of a Differential One-port Device." This article presents a mathematical formula for converting from a two port single-ended measurement to differential impedance. The network analyzer is configured with Port 1 and Port 2 connected to the two differential ports. The formula is straightforward and can be implemented through any major RF design package that can read network analyzer data.

$$\Gamma s = \frac{(2 \cdot S11 - S21)(1 - S22 - S12) + (1 - S11 - S21)(1 + S22 - 2 \cdot S12)}{(2 - S21)(1 - S22 - S12) + (1 - S11 - S21)(1 + S22)}$$

It is also theoretically possible to identify a differential optimal noise impedance (Γ_s), as described in the single-ended domain in *Microwave Transistor Amplifiers* (Gonzalez) and in *Microwave Circuit Design* (Vendelin, Pavio & Rohde). The input network may be designed with this Γ_s to optimize noise performance of the device.

The output port uses matching components (R3, C5 & L3) to decrease the output impedance to 200Ω real and then a 4:1 transformer to reduce its impedance into the 50 Ω range. This solution for providing an IF match is not optimal because it is lossy, and may be modified into a network of reactive components much like appears on the input port. Again, because the matching components are located on the balanced side of the port, differential matching techniques can be employed to obtain an acceptable return loss. To obtain high conversion gain, this port should be matched for maximum return loss. However, an optimal match does not usually provide the best linearity; this port may need to be "de-tuned" to obtain optimal third order intercept (IP3) or compression (P1dB) characteristics. This trade-off is intuitive, considering that the matching network provides an AC voltage gain at the output port, which drives the port into compression earlier.

Note that oscillations have been observed for certain matching structures that provide as of yet undefined source and load impedance to the core. The final datasheet will provide more information about the stability regions of this device. The most practical approach at this point is to check the output spectrum for any sign of an unstable device. If an unstable condition is found, the matching networks need to be adjusted to find a stable condition.

The DC requirements for the mixer core arise because the core consists of a pair of differential stages. The center tap of the 4:1 balun on the output is conveniently used to provide the V_{POS} voltage to the collectors of the differential stage. The inductors (L1 and L2) on the input are used as AC chokes, and the resistor (R1) is used to set the current of the stage. Refer to Figures 1 and 2 for the effect of R1 value on device performance. The internal bias of the mixer core typically produces 1.26 V_{DC} at resistor node.