590 MHz, 25mA, Triple 2:1 Multiplexers

PRELIMINARY TECHNICAL DATA

AD8183/8185

FEATURES

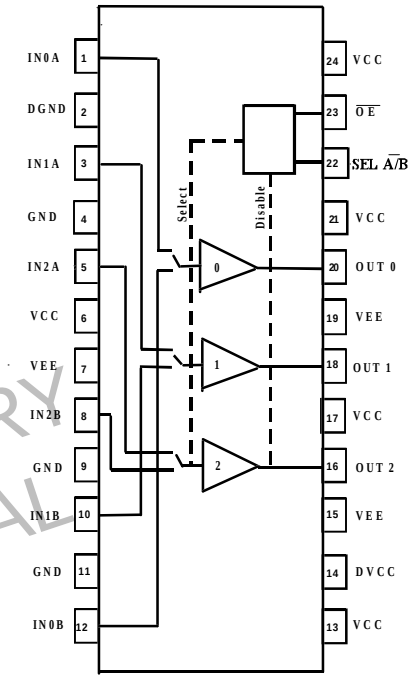
Fully Buffered Inputs and Outputs
Fast Channel Switching: 20ns
High Speed:
590MHz Bandwidth (-3dB) 200mVp-p
530 MHz Bandwidth (-3dB) 2Vp-p
1000 V/µs Slew Rate G = +1
1150 V/µs Slew Rate G = +2
Fast Settling time of 20ns to 0.1%
Low Power: 25mA (AD8183), 25mA (AD8185)
Excellent Video Specifications (R_L=150Ω):
Gain Flatness of 0.1dB to 100MHz
0.01% Differential Gain Error
0.02° Differential Phase Error Low Glitch
"All Hostile "Crosstalk -90dB @ 5MHz
-50dB @ 100MHz
High "OFF" Isolation of -100dB @ 10MHz
Low Cost
Fast Output Disable Feature for Connecting Multiple Devices

APPLICATIONS

Pixel Switching for "Picture-In-Picture"
Switching RGB in LCD & Plasma Displays
RGB Video Switchers & Routers

PACKAGE PINOUT

AD8183/AD8185



TRUTH TABLE

SEL A/B	0E	OUT
0	0	INA
1	0	INB
0	1	High Z
1	1	High Z

PRODUCT DESCRIPTION

The AD8183 (G = +1) and AD8185 (G = +2) are high speed Triple 2-to-1 multiplexers. They offer -3dB full signal bandwidth up to 590MHz along with slew rate in excess of 1000V/µs. With better than -90dB of all hostile crosstalk and isolation, they are useful in many high speed applications. The differential gain and differential phase error of 0.01% and 0.02°, along with 0.1dB flatness to 100MHz make AD8183 and AD8185 ideal for professional video and LCD multiplexing. They offer 20ns switching time making them an excellent choice for switching video signals, while consuming less than 25mA on ±5V supply voltage.

Both devices offer a high speed disable feature allowing the output to be put into a high impedance state. This allows the building of larger input arrays while minimizing "OFF" channel output loading. They operate on voltage supplies of ±5V and are offered in 24 lead TSSOP package.

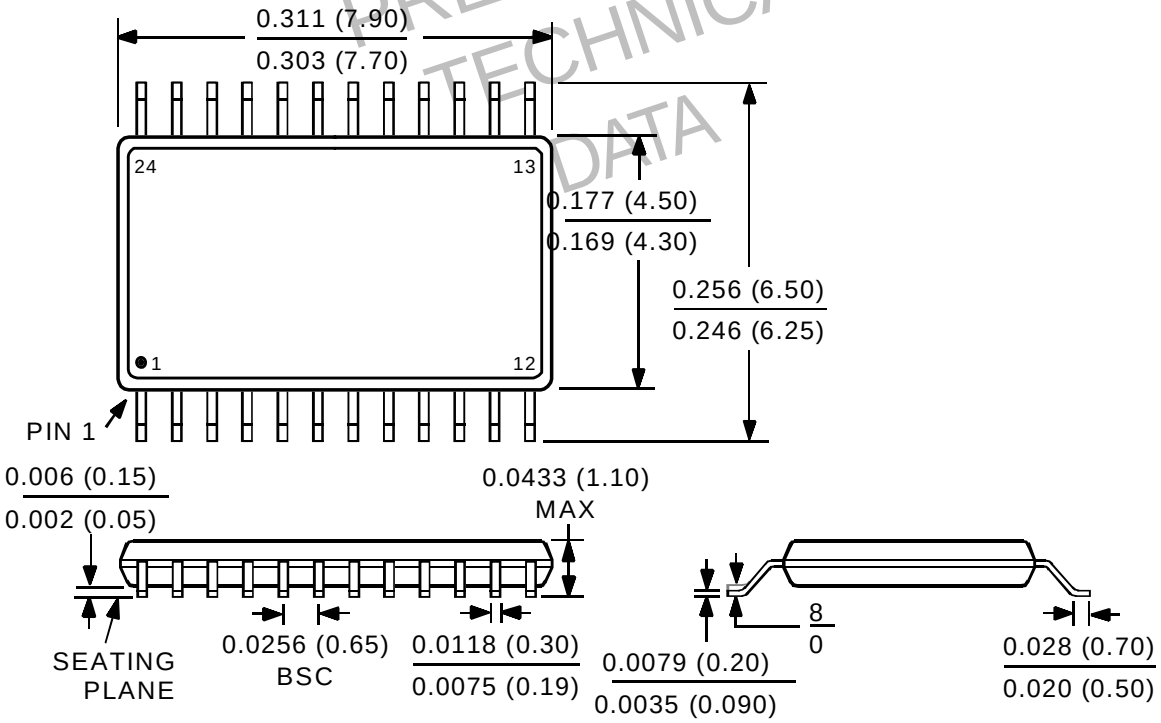
AD8183/AD8185 SPECIFICATIONS(@ Ta= +25°C, V_S=±5V, R_L=1kΩ unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
-3dB Bandwidth (Small Signal)	Vin=200mV p-p		590/360		MHz
	Vin=200mV p-p, R_L=150Ω		380/320		MHz
-3dB Bandwidth (Large Signal)	Vin=2Vp-p		530/350		MHz
	Vin=2V p-p, R_L=150Ω		310/300		MHz
0.1dB Bandwidth	Vin=200mV p-p		110/50		MHz
	Vin=200mV p-p, R_L=150Ω		100/160		MHz
Slew Rate	2V Step		1000/1150		V/µs
Settling Time to 0.1%	2V Step		20		ns
DISTORTION/NOISE PERFORMANCE					
Differential Gain	*f*= 3.58MHz, 150Ω		0.01		%
Differential Phase	*f*= 3.58MHz, 150Ω		0.02		Degrees
All Hostile Crosstalk[6]	*f*=5MHz, R_L=1kΩ		-90/-80		dB
	f=100MHz, R_L=1kΩ		-50/-45		dB
OFF Isolation[7]	*f*=5MHz,R_L=150Ω		-100		dB
Voltage Noise	*f*= 10kHz to 30MHz		20/14		nV/√Hz
DC/ TRANSFER CHARACTERISTICS					
Voltage Gain Error	No Load		0.20	0.25/0.75	%
Input Offset Voltage			5		mV
	Tmin to Tmax		10		mV
Input Offset Voltage Matching	Channel-to-Channel		1/1	25/40	mV
Input Offset Drift			15		µV/°C
Input Bias Current			6/10	10/20	µA
INPUT CHARACTERISTICS					
Input Resistance		4/1	8/5		MΩ
Input Capacitance	Channel Enabled		1.5/1.5		pF
	Channel Disabled		1.5/1.5		pF
Input Voltage Range			±3.0/±1.5		V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L=1KΩ	±2.90	±3.25		V
	R_L=150Ω	±2.65	±2.95		V
Short Circuit Current(Protected)			30/75		mA
Output Resistance	Enabled		0.8	1.1	Ω
	Disabled	4	8		MΩ
Output Capacitance	Disabled		5		pF
POWER SUPPLY					
Operating Range		±4.5		±5.5	V
Power Supply Rejection Ratio	+PSRR +V_S = +4.5 to +5.5V, -V_S= -5V	58	66/72		dB
	-PSRR -V_S = -4.5 to -5.5V, +V_S= +5V	52	56/68		dB
Quiescent Current	All Channels "ON"		25	30	mA
	All Channels "OFF"		3/7	5/10	mA
	Tmin to Tmax				mA
OPERATING TEMPERATURE RANGE					
Temperature Range	Operating (Still Air)	-40		+85	°C
θ_{JA}	Operating (Still Air)		128		°C/W
θ_{JC}	Operating (Still Air)		42		°C/W

AD8183/AD8185 SPECIFICATIONS(@ Ta= +25°C, V_S=±5V, R_L=1kΩ unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS					
Switch Time[1]	Channel-Channel				
50% Logic to 10% Output Settling	IN0=+1V, IN1=-1V, R_L=1kΩ		20/17		ns
50% Logic to 90% Output Settling	IN0=+1V, IN1=-1V, R_L=1kΩ		20/18		ns
ENABLE to Channel ON Time[2]					
50% Logic to 90% Output Settling	IN0=+1V, IN1=-1V, R_L=1kΩ		20		ns
ENABLE to Channel OFF Time[2]					
50% Logic to 90% Output Settling	IN0=+1V, IN1=-1V, R_L=1kΩ		40		ns
Channel Switching Transient (Glitch)[3]	All Inputs Grounded, R_L=1kΩ		50/70		mV
DIGITAL INPUTS					
Logic "1" Voltage	SEL and ENABLE Inputs		2.0		V
Logic "0" Voltage	SEL and ENABLE Inputs		0.8		V
Logic "1" Input Current	SEL, ENABLE= +4V		100		nA
Logic "0" Input Current	SEL, ENABLE= +0.4V		1		µA

24 PIN TSSOP PACKAGE OUTLINE



Controlling Dimension: Metric, shown in parenthesis.
Soldering Profile: J-STD-20