ANALOG DEVICES

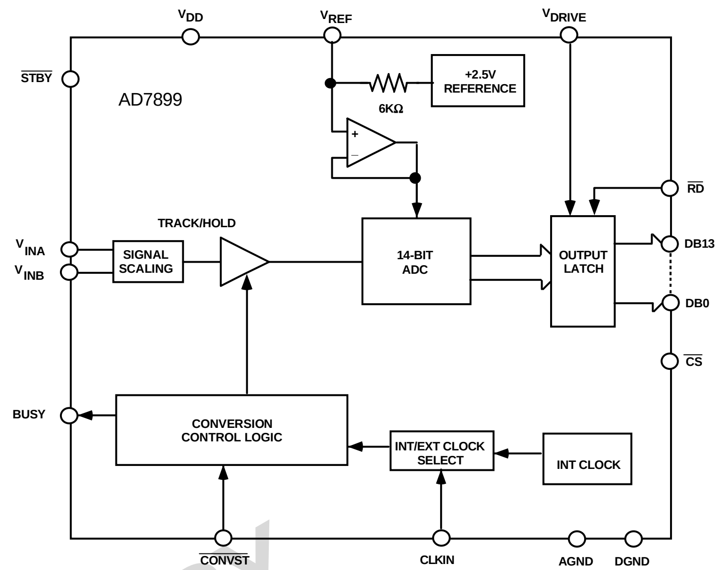
5V Single Supply 14-Bit 400kSPS ADC

Preliminary Technical Data

AD7899

FEATURES
Fast (2.0 μs) 14-Bit ADC
400kSPS Throughput Rate
0.35 μs Track/Hold Acquisition Time
Single Supply Operation
Selection of Input Ranges: ±10 V, ±5 V and ±2.5 V
0 V to +2.5 V and 0 V to +5 V
High Speed Parallel Interface
which also allows Interfacing to 3V processors
Low Power, 75mW typ
Power Saving Mode,15μW typ
Overvoltage Protection on Analog Inputs
Power-down mode via STBY pin.

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7899 is a fast, low power, 14-bit A/D converter that operates from a single +5 V supply. The part contains a 2.0μs successive approximation ADC, a track/hold amplifier, 2.5V reference, on chip clock oscillator, signal conditioning circuitry and a high speed parallel interface. The part accepts analog input ranges of ±10 V , ±5V, ±2.5V 0V to +2.5V and 0V to +5V. Overvoltage protection on the analog inputs for the part allows the input voltage to exceeded without damaging the parts or affecting a conversion in progress.

Speed of conversion can be controlled either by an internally trimmed clock oscillator or by an external clock.

A conversion start signal ($\overline{CONVST}$) places the track/hold into hold mode and initiates conversion sequence for the channel. The BUSY/$\overline{EOC}$ signal indicates the end of the conversion sequence.

Data is read from the part via a 14-bit parallel data bus using the standard $\overline{CS}$ and $\overline{RD}$ signals. Maximum throughput for the AD7899 is 400kSPS.

The AD7899 is available in a 28 pin SOIC and SSOP packages.

PRODUCT HIGHLIGHTS

1. The AD7899 features a fast (2.0μs) ADC allowing allowing throughput rates of upto 400kSPS.
2. The AD7899 operates from a single +5 V supply and consumes only 75 mW typ making it ideal for low power and portable applications.
3. The part offers a high speed parallel interface. The interface can operate in 3V and 5V mode allowing for easy connection to 3V or 5V microprocessors, microcontrollers and digital signal processors.
4. The part is offered in three versions with different analog input ranges. The AD7899-1 offers the standard industrial ranges of ±10V and ±5V; the AD7899-2 offers a unipolar range of 0V to +2.5 or 0V to +5V andthe AD7899-3 offers the common signal processing input range of ±2.5V.

REV. PrC 10/99

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AD7899–SPECIFICATIONS[1]

(V_{DD} = +5 V ±5%, AGND = DGND = 0 V, V_{REF} = Internal. Clock = Internal, All Specifications T_{MIN} to T_{MAX} and valid for V_{DRIVE} = +3V±5% and +5V±5% unless otherwise noted).

Parameter	A, S Version[1]	B Version[1]	Units	Test Conditions/Comments
SAMPLE AND HOLD				
-3dB Full Power Bandwidth	3	3	MHz typ	
Aperture Delay	20	20	ns max	
Aperture Jitter	50	50	ps typ	
Aperture Delay Matching	4	4	ns max	
DYNAMIC PERFORMANCE[2]				f_{IN} = 100 kHz, f_S = 400 ksps
Signal to (Noise+Distortion) Ratio[3]				
@ 25°C	78	78	dB min	
Tmin to Tmax	77	77	dB min	
Total Harmonic Distortion[3]	-86	-86	dB max	
Peak Harmonic or Spurious Noise[3]	-88	-88	dB max	
Intermodulation Distortion[3]				fa = 49kHz, fb = 50kHz
2nd Order Terms	-95	-95	dB typ	
3rd Order Terms	-95	-95	dB typ	
DC ACCURACY				
Resolution	14	14	Bits	
Relative Accuracy (INL)[3]	±2	±1.5	LSB max	
Differential Nonlinearity (DNL)[3]	±1	±1	LSB max	No missing codes guaranteed
Positive Gain Error[3]	±10	±8	LSB max	
Negative Gain Error[3]	±10	±8	LSB max	
Bipolar Zero Error	±12	±10	LSB max	
ANALOG INPUTS				
AD7899-1				
Input Voltage Range	±5, ±10	±5, ±10	Volts	
Input Current	0.25, 0.6	0.25, 0.6	mA max	V_{IN} = -5V and -10V respectively
AD7899-2				
Input Voltage Range	0 to +2.5, 0 to +5	0 to +2.5 0 to +5	Volts	
Input Current	200	200	nA max	V_{IN} = 0V
AD7899-3				
Input Voltage Range	±2.5	±2.5	Volts	
Input Current	0.3	0.3	mA max	V_{IN} = -2.5V
REFERENCE INPUT/OUTPUT				
V_{REF} IN Input Voltage Range	2.375/2.625	2.375/2.625	Vmin/Vmax	2.5V ± 5%
V_{REF} IN Input Capacitance[4]	10	10	pF max	
V_{REF} OUT Output Voltage	2.5	2.5	V nom	
V_{REF} OUT Error @ 25°C	±10	±10	mV max	
V_{REF} OUT Error Tmin to Tmax	±20	±20	mV max	
V_{REF} OUT Temperature Coefficient	25	25	ppm/°C typ	
V_{REF} OUT Output Impedance	6	6	kΩ typ	See Reference Section
LOGIC INPUTS				
Input High Voltage, V_{INH}	V_{DRIVE}/2 + 0.4	V_{DRIVE}/2 + 0.4	V min	V_{DD} = 5V±5%
Input Low Voltage, V_{INL}	V_{DRIVE}/2 - 0.4	V_{DRIVE}/2 - 0.4	V max	V_{DD} = 5V±5%
Input Current, I_{IN}	±10	±10	µA max	
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DRIVE} - 0.4	V_{DRIVE} - 0.4	V min	I_{SOURCE} = 400µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6mA
DB13 - DB0				
High Impedance				
Leakage Current	±10	±10	µA max	
Capacitance[4]	10	10	pF max	
Output Coding				
AD7899-1,AD7899-3		Two's Complement		
AD7899-2		Straight (Natural) Binary		

AD7899–SPECIFICATIONS

(V_{DD} = +5 V ±5%, AGND=DGND= 0V, V_{REF} = Internal, Clock = Internal. All Specifications T_{MIN} to T_{MAX} unless otherwise noted).

Parameter	A,S Version[1]	B Version[1]	Units	Test Conditions/Comments
CONVERSION RATE				
Conversion Time	2.0	2.0	µs max	
Track/Hold Acquisition Time[2,3]	0.35	0.35	µs max	
Throughput Time	400	400	ksps max	
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for specified performance
I_{DD}				(5 µA typ) Logic Inputs = 0V or V_{DD}
Normal Mode	17	17	mA max	
Standby Mode	20	20	µA max	
Power Dissipation				
Normal Mode	90	90	mW max	Typically 75 mW. V_{DD} =+5V
Standby Mode	100	100	µW max	Typically 20 µW

NOTES
[1]Temperature Ranges are as follows : A,B Versions: -40°C to +85°C. S Version: -55°C to +125°C
[2]Performance measured through full channel (SHA and ADC)
[3]See Terminology
Specifications subject to change without notice.

ORDERING GUIDE

Model	Input Ranges	Relative Accuracy	Temperature Range[1]	Package Option *
AD7899AR-1	±5V, ±10V	±2 LSB	-40°C to +85°C	R-28
AD7899BR-1	±5V, ±10V	±1.5 LSB	-40°C to +85°C	R-28
AD7899SR-1	±5V, ±10V	±2 LSB	-55°C to +125°C	R-28
AD7899AR-2	0V to 5V, 0V to 2.5V	±2 LSB	-40°C to +85°C	R-28
AD7899AR-3	±2.5V	±2 LSB	-40°C to +85°C	R-28
AD7899BR-3	±2.5V	±1.5 LSB	-40°C to +85°C	R-28
AD7899ARS-1	±5V, ±10V	±2 LSB	-40°C to +85°C	RS-28
AD7899ARS-2	0V to 5V, 0V to 2.5V	±2 LSB	-40°C to +85°C	RS-28
AD7899ARS-3	±2.5V	±2 LSB	-40°C to +85°C	RS-28

*R =28-Pin Small Outline Package
*RS=28-Pin Shrink Small Outline Package

TIMING CHARACTERISTICS[1,2]

(V_{D} = +5 V ±5%, AGND = DGND = 0V, V_{REF} = Internal, Clock = Internal, All Specifications T_{MIN} to T_{MAX} and valid for V_{DRIVE} = +3V±5% and +5V±5% unless otherwise noted).

Parameter	A, B & S Versions	Units	Test Conditions/Comments
t_{CONV}	2.0	µs max	Conversion Time, Internal Clock
	15	clock cycles	Conversion Time, External Clock
	3	µs max	CLKIN = 5MHz
t_{ACQ}	0.35	µs max	Acquisition Time
t_{EOC}	120	ns min	EOC Pulsewidth
	180	ns max	
$t_{WAKE-UP}$ - External Vref[5]	2	µs max	$\overline{\text{STBY}}$ rising edge to $\overline{\text{CONVST}}$ rising edge (See Standby Mode Operation)
t_1	35	ns min	$\overline{\text{CONVST}}$ Pulse Width
t_2	70	ns min	$\overline{\text{CONVST}}$_rising edge to BUSY rising edge
Read Operation			
t_3	0	ns min	$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Setup Time
t_4	0	ns min	$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Hold Time
t_5	35	ns min	Read Pulse Width
t_6[3]	35	ns max	Data Access Time After Falling Edge of $\overline{\text{RD}}$, V_{DRIVE} = 5V
	40	ns max	Data Access Time After Falling Edge of $\overline{\text{RD}}$, V_{DRIVE} = 3V
t_7[4]	5	ns min	Bus Relinquish Time After Rising Edge of $\overline{\text{RD}}$
	30	ns max	
t_8	0	ns min	BUSY Falling edge to $\overline{\text{RD}}$ delay
External Clock			
t_9	200	ns min	$\overline{\text{CONVST}}$ Rising edge to CLK Falling edge

NOTES
[1] Sample tested at 25°C to ensure compliance. All input signals are measured with tr = tf = 1ns (10% to 90% of +5V) and timed from a voltage level of +1.6 V.
[2] See Figures 7, 8 and 9.
[3] Measured with the load circuit of Figure 2 and defined as the time required for an output to cross 0.8 V or 2.0 V.
[4] These times are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.
[5] Refer to the section, "Standby Mode Operation". The MAX specification of 6ms is valid when using a 0.1µF decoupling capacitor on the V_{REF} pin.

Specifications subject to change without notice.

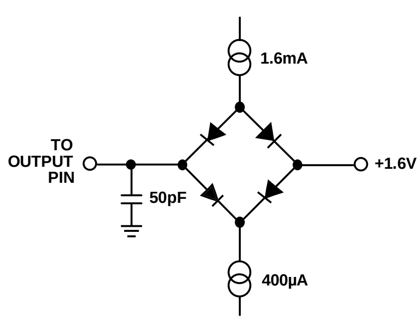


Figure 2. Load Circuit for Access Time and Bus Relinquish Time

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

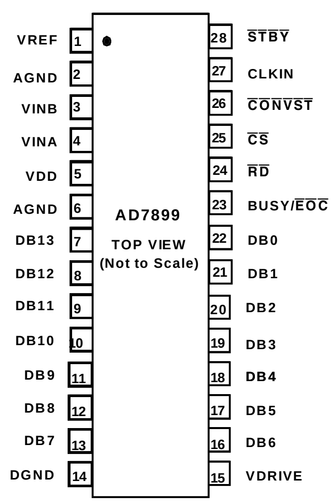
V_{DD} to AGND . . . . -0.3 V to +7V
V_{DD} to DGND . . . . -0.3 V to +7V
V_{DRIVE} to DGND . . . . V_{DD}+0.3V
Analog Input Voltage to AGND
  AD7899-1 (±10V Range) . . . . ±18V
  AD7899-1 (±5V Range) . . . . ±9V
  AD7899-2 . . . . -1V to +18V
  AD7899-3 . . . . -4 to +18V
Reference Input Voltage to AGND . . -0.3V to V_{DD}+0.3V
Digital Input Voltage to DGND . . . -0.3V to V_{DD}+0.3V
Digital Output Voltage to DGND . -0.3V to V_{DD}+0.3V
Operating Temperature Range
  Commercial (A, B Version) . . . . -40°C to +85°C
  Storage Temperature Range . . . . -65°C to +150°C
  Junction Temperature . . . . +150°C
SOIC Package, Power Dissipation 450mW
θ_{JA} Thermal Impedance . . . . 95°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . +215°C
    Infared (15 sec) . . . . +220°C
SSOP Package, Power Dissipation 450mW
θ_{JA} Thermal Impedance . . . . 95°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . +215°C
    Infared (15 sec) . . . . +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7899 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION
SOIC/ SSOP



PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	V_{REF}	Reference Input/Output. This pin is provides access to the internal reference (2.5V ± 20mV) and also allows the internal reference to be overdriven by an external refer ence source (2.5V ± 5%) . A 0.1µF decoupling capacitor should be connected be tween this pin and AGND.
2	AGND	Analog Ground. General analog ground. This AGND pin should be connected to the system's AGND plane.
3-4	V_{INB}, V_{INA}	Analog Inputs. See Analog Input Section.
5	V_{DD}	Positive Supply Voltage, +5.0 V ±5%.
6	AGND	Analog Ground. General analog ground. This AGND pin should be connected to the system's AGND plane.
7-13	DB13 - DB7	Data Bit 13 is the MSB, followed by Data Bit 12 to Data Bit 7. Three-state TTL outputs.
14	DGND	Digital Ground. General digital ground. This DGND pin should be connected to the system's DGND plane.
15	V_{DRIVE}	This pin provides the positive supply voltage for the digital inputs and outputs. It is normally tied to DV_{DD}. V_{DRIVE} should be decoupled with a 0.1µF capacitor. It allows improved performance when reading during the conversion sequence. The VDRIVE pin may be powered by a 3V±10% supply which allows the inputs and outputs to be interfaced to 3V processors and DSPs.
16-22	DB6 - DB0	Data Bit 6 to Data Bit 0. Three-state TTL Outputs.
23	BUSY/EOC	BUSY/EOC Output. Digital output pin used to signify that a conversion is in progress or that a conversion has finished. The function of the BUSY/EOC is deter mined by the state of CONVST at the end of conversion. See the Timing and Con trol Section.
24	RD	Read Input. Active low logic input which is used in conjunction with CS low to en able the data outputs.
25	CS	Chip Select Input. Active low logic input. The device is selected when this input is active.
26	CONVST	Convert Start Input. Logic Input. A low to high transition on this input puts the track/hold into hold mode and starts conversion.
27	CLKIN	Conversion Clock Input. CLKIN is an externally applied clock which allows the user to control the conversion rate of the AD7899. If the CLKIN input is high on the rising edge of CONVST an externally applied clock will be used as the conversion clock. If the CLKIN is low on the rising edge of CONVST the internal laser-trimmed oscillator is used as the conversion clock Each conversion needs sixteen clock cycles in order for the conversion to be completed. The externally applied clock should have a duty cycles which is no greater than 60/40. The CLKIN pin can be tied to DGND if an external clock is not required.
28	STBY	Standby Mode Input. Logic input which is used to put the device into the power save or standby mode. The STBY input is high for normal operation and low for standby operation.

TERMINOLOGY

Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_s/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise +distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

Signal to (Noise + Distortion) = (6.02N + 1.76) dB

Thus for a 14-bit converter, this is 86.04 dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7899 it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, and V_5 are the rms amplitudes of the second through the fifth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_s/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m,n = 0,1,2,3, etc. Intermodulation terms are those for which neither m or n are equal to zero. For example, the second order terms include (fa + fb) and (fa - fb), while the third order terms include (2fa + fb), (2fa - fb), (fa + 2fb) and (fa - 2fb).

The AD7899 is tested using two input frequencies. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dB's.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Positive Gain Error (AD7899-1, AD7899-3)

This is the deviation of the last code transition (01.....110 to 01.....111) from the ideal 4 x V_{REF} - 3/2 LSB (AD7899 at ±10 V), 2 x V_{REF} - 3/2 LSB (AD7899 at ±5 V range) or V_{REF} - 3/2 LSB (AD7899 at ±2.5 V range) after the Bipolar Offset Error has been adjusted out.

Positive Gain Error (AD7899-2)

This is the deviation of the last code transition (11.....110 to 11.....111) from the ideal 2 x V_{REF} - 3/2 LSB (AD7899 at ±10 V), 2 x V_{REF} - 3/2 LSB (AD7899 at 0 V to 5 V range) or V_{REF} - 3/2 LSB (AD7899 at 0 V to 2.5 V range) after the Unipolar Offset Error has been adjusted out.

Unipolar Offset Error (AD7899-2)

This is the deviation of the first code transition (00...00 to 00...01)from the ideal AGND +1/2 LSB

Bipolar Zero Error (AD7899-1, AD7899-2)

This is the deviation of the mid-scale transition (all 0's to all 1's) from the ideal AGND - 1/2 LSB.

Negative Gain Error (AD7899-1,AD7899-3)

This is the deviation of the first code transition (10.....000 to 10.....001) from the ideal -4 x V_{REF} + 1/2 LSB (AD7899 at ±10 V), -2 x V_{REF} + 1/2 LSB (AD7899 at ±5 V range) or -V_{REF} + 1/2 LSB (AD7899 at ±2.5 V range) after Bipolar Zero Error has been adjusted out.

Track/Hold Acquisition Time

Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track/hold returns to track mode). It also applies to situations where there is a step input change on the input voltage applied to the selected $V_{INA/VINB}$ input of the AD7899. It means that the user must wait for the duration of the track/hold acquisition time after the end of conversion or after a step input change to $V_{INA/VINB}$ before starting another conversion, to ensure that the part operates to specification.

CONVERTER DETAILS

The AD7899 is a high speed, low power, 14-bit A/D converter that operates from a single +5 V supply. The part contains a 2µs successive approximation ADC,track/hold amplifier, an internal +2.5 V reference and a high speed parallel interface. The part accepts an analog input range of ±10V or ±5V (AD7899-1), 0V to +2.5V or 0V to +5V (AD7899-2) and ±2.5V (AD7899-3). Overvoltage protection on the analog inputs for the part allows the input voltage to go to ±18V (AD7899-1 with ±10V input range), ±9V (AD7899-1 with ±5V input range), -1V to +18V (AD7899-2) and -4V to +18V (AD7899-3) without causing damage or effecting a conversion in process.

A conversion is initiated on the AD7899 by pulsing the $\overline{\text{CONVST}}$ input. On the rising edge of $\overline{\text{CONVST}}$, the on-chip track/hold is placed into hold and the conversion sequence is started the channel. The BUSY output signal is triggered high on the rising edge of $\overline{\text{CONVST}}$ and will remain high for the duration of the conversion sequence. The conversion clock for the part is generated internally using a laser-trimmed clock oscillator circuit. There is also the option of using an external clock. An external non-continuous clock is applied to the CLKIN pin. If, on the rising edge of $\overline{\text{CONVST}}$, this input is low the external clock will be used. The external clock should not start until 200nS after the rising edge of $\overline{\text{CONVST}}$. The optimum throughput is obtained by using the internally generated clock - see Using an External Clock. The BUSY signal indicates the end of the conversion and at this time the Track and Hold returns to tracking mode. The conversion results can be read at the end of the conversion (indicated by BUSY going low) via a 14-bit parallel data bus with standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals - see Timing and Control.

Conversion time for the AD7899 is 2µs and the track/hold acquisition time is 0.35 µs. To obtain optimum performance from the part, the read operation should not occur during a channel conversion or during the 100 ns prior to the next $\overline{\text{CONVST}}$ rising edge. This allows the part to operate at throughput rates up to 400 kHz and achieve data sheet specifications.

CIRCUIT DESCRIPTION

Track/Hold Section

The track/hold amplifier's on the AD7899 allows the ADC's to accurately convert an input sine wave of full-scale amplitude to 14-bit accuracy. The input bandwidth of the track/hold is greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate of 400kSPS (i.e., the track/hold can handle input frequencies in excess of 200KHz).

The track/hold amplifier's acquire input signals to 14-bit accuracy in less than 350ns. The operation of the track/hold is essentially transparent to the user. The track/hold amplifier samples the input channel on the rising edge of $\overline{\text{CONVST}}$. The aperture time for the track/hold (i.e., the delay time between the external $\overline{\text{CONVST}}$ signal and the track/hold actually going into hold) is typically 15 ns and, more importantly, is well matched from device to device. It allows multiple AD7899s to sample more than one channel simultaneously. At the end of a conversion sequence, the part returns to its tracking mode. The acquisition time of the track/hold amplifier's begin at this point.

Reference Section

The AD7899 contains a single reference pin, labelled V_{REF}, which either provides access to the part's own +2.5 V reference or allows an external +2.5 V reference to be connected to provide the reference source for the part. The part is specified with a +2.5 V reference voltage.

The AD7899 contains an on-chip +2.5 V reference. To use this reference as the reference source for the AD7899, simply connect a 0.1 µF capacitor from the V_{REF} pin to AGND. The voltage that appears at this pin is internally buffered before being applied to the ADC. If this reference is required for use external to the AD7899, it should be buffered as the part has a FET switch in series with the reference output resulting in a source impedance for this output of 6kΩ nominal. The tolerance on the internal reference is ±10 mV at 25°C with a typical temperature coefficient of 25 ppm/°C and a maximum error over temperature of ±20mV.

If the application requires a reference with a tighter tolerance or the AD7899 needs to be used with a system reference, then the user has the option of connecting an external reference to this V_{REF} pin. The external reference will effectively overdrive the internal reference and thus provide the reference source for the ADC. The reference input is buffered before being applied to the ADC with the maximum input current of ±100 µA. Suitable reference sources for the AD7899 include the AD680, AD780, REF192 and REF43 precision +2.5 V references.

Analog Input Section

The AD7899 is offered as three part types, the AD7899-1 where the input can be configured for ±10 V or a ±5 V input voltage range, the AD7899-2 where the input can be configured for 0V to 5V or a 0V to 2.5V input voltage range and the AD7899-3 which handles input voltage range ±2.5 V. The amount of current flowing into the analog input will depend on the analog input range and the analog input voltage. The maximum current flows when negative full-scale is applied.

AD7899-1

Figure 3 shows the analog input section of the AD7899-1. The input can be configured for ±5 V or ±10 V operation on the AD7899-1. For ±5 V operation, the V_{INA} and V_{INB} inputs are tied together and the input voltage is applied to both. For ±10V operation, the V_{INB} input is tied to AGND and the input voltage is applied to the V_{INA} input. The V_{INA} and V_{INB} inputs are symmetrical and fully interchangeable.

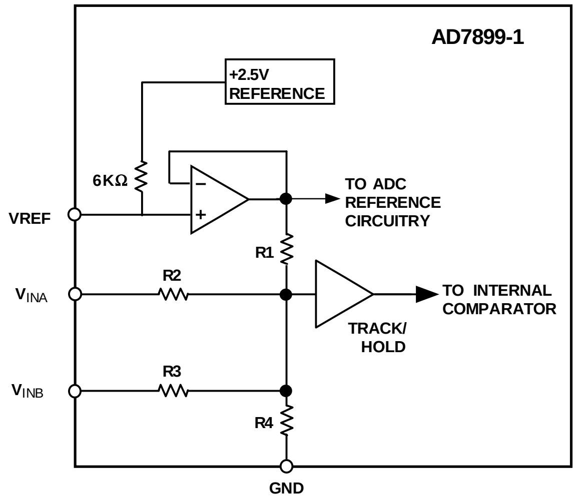


Figure 3. AD7899-1 Analog Input Structure

For the AD7899-1, R1 = 6 kΩ, R2 = 24 kΩ, R3 = 24 kW and R4 = 12 kΩ. The resistor input stage is followed by the high input impedance stage of the track/hold amplifier.

The designed code transitions take place midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs etc.) LSB size is given by the formula, 1 LSB = FSR/16384. For the ±5 V range, 1 LSB = 10 V/16384= 610.4 mV. For the ±10 V range, 1 LSB = 20 V/16384 = 1.22 mV. Output coding is 2s complement binary with 1 LSB = FSR/16384. The ideal input/output transfer function for the AD7899-1 is shown in Table I.

Table I. Ideal Input/Output Code Table for the AD7899-1

Analog Input[1]	Digital Output Code Transition
+FSR/2 – 3/2 LSB[2]	011 . . . 110 to 011 . . . 111
+FSR/2 – 5/2 LSBs	011 . . . 101 to 011 . . . 110
+FSR/2 – 7/2 LSBs	011 . . . 100 to 011 . . . 101
AGND + 3/2 LSB	000 . . . 001 to 000 . . . 010
AGND + 1/2 LSB	000 . . . 000 to 000 . . . 001
AGND – 1/2 LSB	111 . . . 111 to 000 . . . 000
AGND – 3/2 LSB	111 . . . 110 to 111 . . . 111
–FSR/2 + 5/2 LSBs	100 . . . 010 to 100 . . . 011
–FSR/2 + 3/2 LSBs	100 . . . 001 to 100 . . . 010
–FSR/2 + 1/2 LSB	100 . . . 000 to 100 . . . 001

NOTES
[1]FSR is full-scale range and is 20 V for the ±10 V range and 10 V for the ±5 V range, with VREF = +2.5 V.
[2]1 LSB = FSR/16384 = 1.22 mV (±10 V - AD7899-1) and 610.4 mV (±5 V - AD7899-1) with VREF = +2.5 V.

AD7899-2

Figure 4 shows the analog input section of the AD7899-2. Each input can be configured for 0 V to +5 V operation or 0 V to +2.5 V operation. For 0 V to +5 V operation, the V_{INB} input is tied to AGND and the input voltage is applied to the V_{INA} input. For 0 V to 2.5 V operation, the V_{INA} and V_{INB} inputs are tied together and the input voltage is applied to both. The V_{INA} and V_{INB} inputs are symmetrical and fully interchangeable. Thus for ease of PCB layout on the 0 V to +5 V range the input voltage may be applied to the V_{INB} input while the V_{INA} input is tied to AGND.

For the AD7899-2, R1 = 4 kΩ and R2 = 4 kΩ. Once again, the designed code transitions occur on successive integer LSB values. Output coding is straight (natural) binary with 1 LSB = FSR/16384 = 2.5 V/16384 = 0.153 mV, and 5V/16384 = 0.305 mV, for the 0 to 2.5V and the 0 to 5V options respectively. Table II shows the ideal input and output transfer function for the AD7899-2.

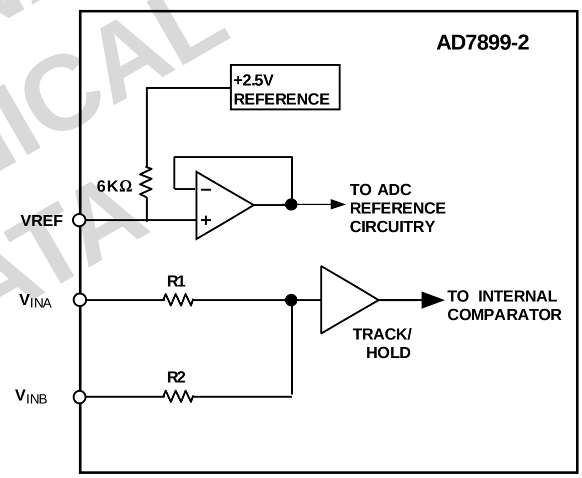


Figure 4. AD7899-2 Analog Input Structure

Table II. Ideal Input/Output Code Table for THE AD7899-2

Analog Input[1]	Digital Output Code Transition
+FSR – 3/2 LSB[2]	111 . . . 110 to 111 . . . 111
+FSR – 5/2 LSB	111 . . . 101 to 111 . . . 110
+FSR – 7/2 LSB	111 . . . 100 to 111 . . . 101
AGND + 5/2 LSB	000 . . . 010 to 000 . . . 011
AGND + 3/2 LSB	000 . . . 001 to 000 . . . 010
AGND + 1/2 LSB	000 . . . 000 to 000 . . . 001

NOTES
[1]FSR is Full-Scale Range and is 0 to 2.5 V and 0 to 5 V for AD7899-2 with VREF = +2.5 V.
[2]1 LSB = FSR/16384 and is 0.153 mV (0 to 2.5 V) and 0.305 mV (0 to 5 V) for AD7899-2 with VREF = +2.5 V.

AD7899-3

Figure 5 shows the analog input section of the AD7899-3. The analog input range is ±2.5 V on the V_{INA} input. The V_{INB} input can be left unconnected but if it is connected to a potential then that potential must be AGND.

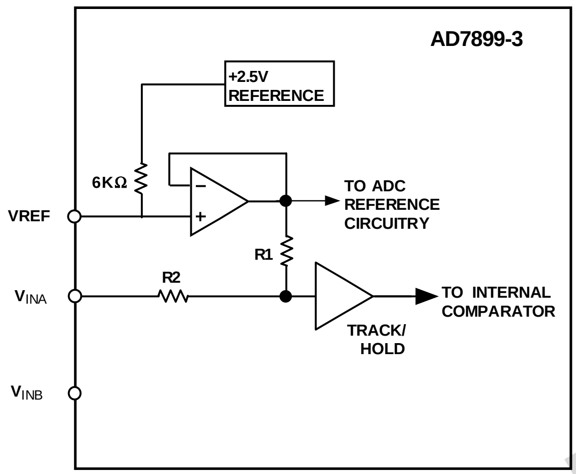


Figure 5. AD7899-3 Analog Input Structure

For the AD7899-3, R1 = 6 kΩ and R2 = 6 kΩ. As a result, the V_{INA} input should be driven from a low impedance source. The resistor input stage is followed by the high input impedance stage of the track/hold amplifier. The designed code transitions take place midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs etc.) LSB size is given by the formula, 1 LSB = FSR/16384. Output coding is 2s complement binary with 1 LSB = FSR/16384 = 5 V/16384 =610.4 mV. The ideal input/output transfer function for the AD7899-3 is shown in Table II.

Table II. Ideal Input/Output Code Table for the AD7899-3

Analog Input[1]	Digital Output Code Transition
+FSR/2 – 3/2 LSB[2]	011 . . . 110 to 011 . . . 111
+FSR/2 – 5/2 LSBs	011 . . . 101 to 011 . . . 110
+FSR/2 – 7/2 LSBs	011 . . . 100 to 011 . . . 101
AGND + 3/2 LSB	000 . . . 001 to 000 . . . 010
AGND + 1/2 LSB	000 . . . 000 to 000 . . . 001
AGND – 1/2 LSB	111 . . . 111 to 000 . . . 000
AGND – 3/2 LSB	111 . . . 110 to 111 . . . 111
–FSR/2 + 5/2 LSBs	100 . . . 010 to 100 . . . 011
–FSR/2 + 3/2 LSBs	100 . . . 001 to 100 . . . 010
–FSR/2 + 1/2 LSB	100 . . . 000 to 100 . . . 001

NOTES
[1]FSR is full-scale range is 5 V, with VREF = +2.5 V.
[2]1 LSB = FSR/16384 = 610.4 µV (±2.5 V - AD7899-3) with VREF = +2.5 V.

TIMING AND CONTROL

Starting a Conversion Sequence

The conversion sequence is initiated by applying a rising edge to the $\overline{CONVST}$ signal. This places the track/hold into hold mode and starts the conversion sequence. The status of the conversion is indicated by the dual function signal BUSY/$\overline{EOC}$. The AD7899 can operate in two conversion modes, EOC (End Of Conversion) mode and BUSY mode. The operating mode is determined by the state of $\overline{CONVST}$ at the end of the conversion.

Selecting a Conversion Clock

The AD7899 has an internal laser trimmed oscillator which can be used to control the conversion process. Alternatively an external clock source can be used to control the conversion process. The highest external clock frequency allowed is 5Mhz. This means a conversion time of 3.2 µs compared to 2µs using the internal clock. However in some instances it may be useful to use an external clock when high throughput rates are not required. For example two or more AD7899s may be synchronized by using the same external clock for all devices. In this way there is no latency between output logic signals due to differences in the frequency of the internal clock oscillators.

On the rising edge of $\overline{CONVST}$ the AD7899 will examine the status of the CLKIN pin. If this pin is low it will use the internal laser trimmed oscillator as the conversion clock. If the CLKIN pin is high the AD7899 will wait for an external clock to be supplied to this pin which will then be used as the conversion clock. The first falling edge of the external clock should not happen for at least 200nS after the rising edge of $\overline{CONVST}$ to ensure correct operation. Figure 6 shows how the various logic outputs are synchronized to the CLKIN signal. Each conversion requires 16 clocks. The result of the conversion is transferred to the output data register on the falling edge of the 16th clock cycle.

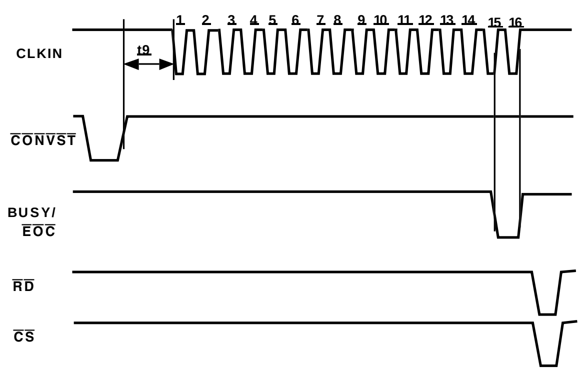


Figure 6. AD7899 Using an External Clock

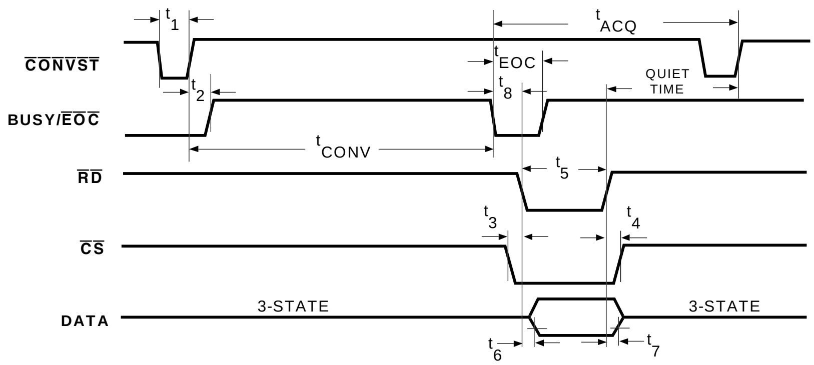


Figure 7. Conversion Sequence Timing Diagram ($\overline{\text{EOC}}$ Mode)

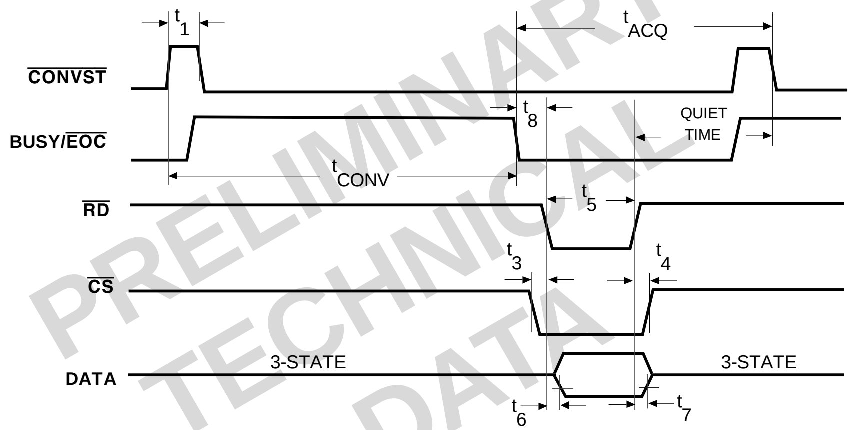


Figure 8. Conversion Sequence Timing Diagram (BUSY Mode)

EOC Mode

The $\overline{\text{CONVST}}$ signal is normally high. Pulsing the $\overline{\text{CONVST}}$ low will initiate a conversion on the its rising edge. The state of the $\overline{\text{CONVST}}$ signal is checked at the end of conversion. Since the $\overline{\text{CONVST}}$ will be high when this happens the AD7899 BUSY/$\overline{\text{EOC}}$ pin will take on its $\overline{\text{EOC}}$ function and bring the BUSY/$\overline{\text{EOC}}$ line low for one clock period before returning high again. In this mode the $\overline{\text{EOC}}$ can be tied to the $\overline{\text{RD}}$ and $\overline{\text{CS}}$ signals to allow automatic reading of the conversion result if required. The timing diagram for operation in EOC mode is shown in Figure 7.

BUSY Mode

The $\overline{\text{CONVST}}$ signal is normally low. Pulsing the $\overline{\text{CONVST}}$ high will initiate a conversion on its rising edge. The state of the $\overline{\text{CONVST}}$ signal is checked at the end of conversion. Since the $\overline{\text{CONVST}}$ will be low when this happens the AD7899 BUSY/$\overline{\text{EOC}}$ pin will take on its BUSY function will bring BUSY/$\overline{\text{EOC}}$ low, indicating that the conversion is complete. BUSY/$\overline{\text{EOC}}$ will remain low until the next rising edge of $\overline{\text{CONVST}}$ where BUSY/$\overline{\text{EOC}}$ returns high. The timing diagram for operation in BUSY mode is shown in Figure 8.

Continuous Conversion Mode

When the AD7899 is used with an external clock, connecting the CLKIN and $\overline{\text{CONVST}}$ signals together will cause the AD7899 to continuously perform conversions. As each conversion completes the BUSY/$\overline{\text{EOC}}$ pin will pulse low for one clock period ($\overline{\text{EOC}}$ function) indicating that the conversion result is available. Figure 9 shows the timing and control sequence of the AD7899 in Continuous Conversion Mode.

Reading Data From The AD7899

Data is read from the part via a 14-bit parallel data bus with standard CS and RD signals. The CS and RD inputs are internally gated to enable the conversion result onto the data bus. The data lines DB0 to DB13 leave their high impedance state when both CS and RD are logic low. Therefore CS may be permanently tied logic low and the RD signal used to access the conversion result if required. Figures 7 and 8 show a timing specification called "Quiet Time". This is the amount of time which should be left after a read operation and before the next conversion is initiated. The quiet time depends heavily on data bus capacitance but a figure of 50ns to 100ns is typical.

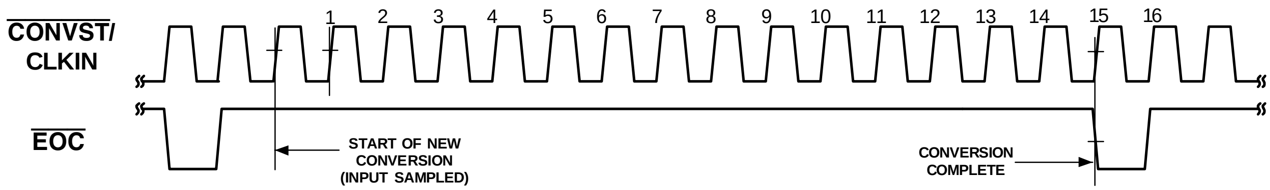


Figure 9. Continuous Conversion Mode

Standby Mode Operation

The AD7899 has a Standby Mode where by the device can be placed in a low current consumption mode (5µA typ). The AD7899 is placed in Standby by bringing the logic input STBY low. The AD7899 can be powered again up for normal operation by bringing STBY logic high. The output data buffers are still operational while the AD7899 is in Standby. This means the user can still continue to access the conversion results while the AD7899 is in Standby. This feature can be used to reduce the average power consumption in a system using low throughput rates. To reduce the average power consumption the AD7899 can be placed in Standby at the end of each conversion sequence, i.e. when BUSY goes low and taken out of Standby again prior to the start of the next conversion sequence. The time it takes the AD7899 to come out of Standby is called the "wake up" time. This wake-up time will limit the maximum throughput rate at which the AD7899 can be operated when powering down between conversions. When using the internal reference the wake-up time will depend on how much of the charge on the reference capacitor has leaked away. For standby times of less than 10mS the AD7899 will typicall wake up in less than 5µs. If all the charge on the reference capacitor has been depleted the AD7899 will still wake up in less than 10mS. The AD7899 will wake-up in approximately 1µs when using an external reference regardless of sleep time.

Figure 10 shows typical wake up times of the AD7899 for standby times greater than 1 millisecond. When operating the AD7899 in a Standby mode between conversions the power savings can be significant. For example with a throughput rate of 10kSPS and an external reference the AD7899 will be powered up for 3µs out of every 100µs (1µs for wake-up time and 2µs for conversion time). Therefore the average power consumption drops to 125mW X 3% or 3.75mW approximately.

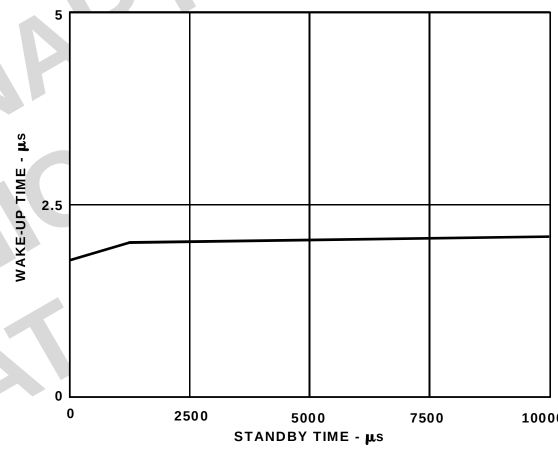


Figure 10. Wake-up Time Vs Standby Time

AD7899 DYNAMIC SPECIFICATIONS

The AD7899 is specified and 100% tested for dynamic performance specifications as well as traditional dc specifications such as Integral and Differential Nonlinearity. These ac specifications are required for the signal processing applications such as phased array sonar, adaptive filters and spectrum analysis. These applications require information on the ADC's effect on the spectral content of the input signal. Hence, the parameters for which the AD7899 is specified include SNR, harmonic distortion, intermodulation distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal to noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (fs/2) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to noise ratio for a sine wave input is given by

$$SNR = (6.02N + 1.76)\ dB \qquad (1)$$

where N is the number of bits.
Thus for an ideal 14-bit converter, SNR = 86.04 dB.

Figure 11 shows a histogram plot for 8192 conversions of a dc input using the AD7899 with 5 V supply. The analog input was set at the center of a code transition. It can be seen that all the codes appear in the one output bin indicating very good noise performance from the ADC.

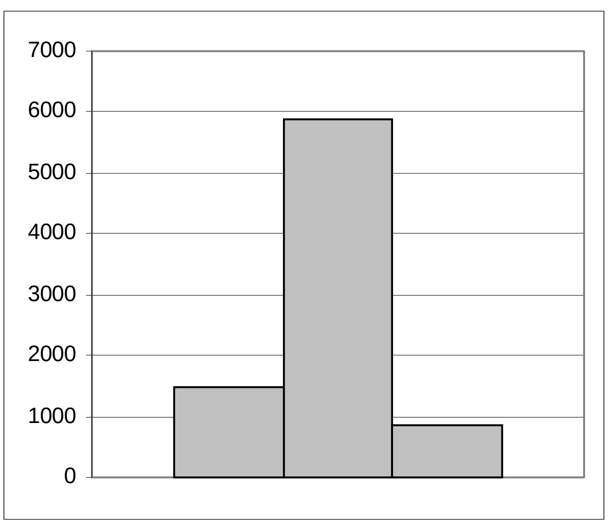


Figure 11. Histogram of 8192 Conversions of a DC Input

The output spectrum from the ADC is evaluated by applying a sine wave signal of very low distortion to the analog input. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 12 shows a typical 4096 point FFT plot of the AD7899 with an input signal of 100 kHz and a sampling frequency of 350 kHz. The SNR obtained from this graph is 80.5 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

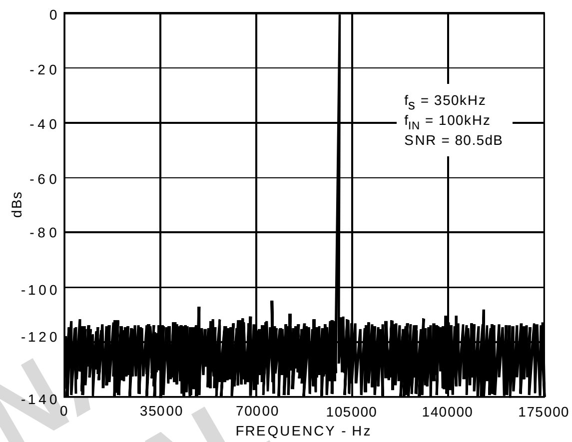


Figure 12. AD7899 FFT Plot

Effective Number of Bits

The formula given in Equation 1 relates the SNR to the number of bits. Rewriting the formula, as in Equation 2, it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \qquad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR. Figure 13 shows a typical plot of effective number of bits versus frequency for an AD7899.

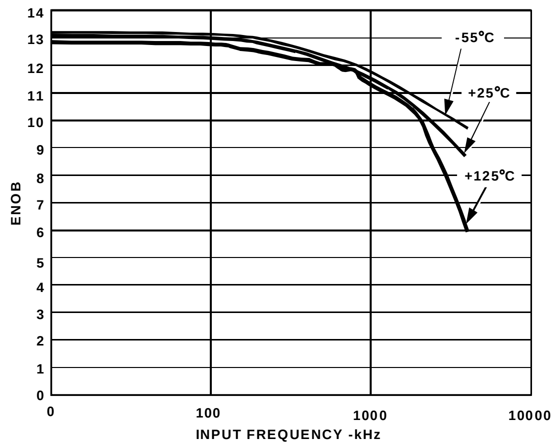


Figure 13. Effective Numbers of Bits vs. Frequency

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3 . . ., etc. Intermodulation terms are those for which neither m or n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb) while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7899 is tested using two input frequencies. In this case the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs. In this case, the input consists of two, equal amplitude, low distortion sine waves. Figure 14 shows a typical IMD plot for theAD7899

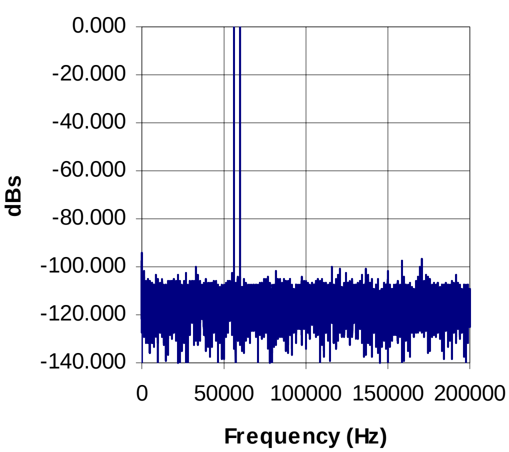


Figure 14. AD7899 IMD Plot

AC Linearity Plots

The plots shown in Figure 15 below show typical DNL and INL for the AD7899.

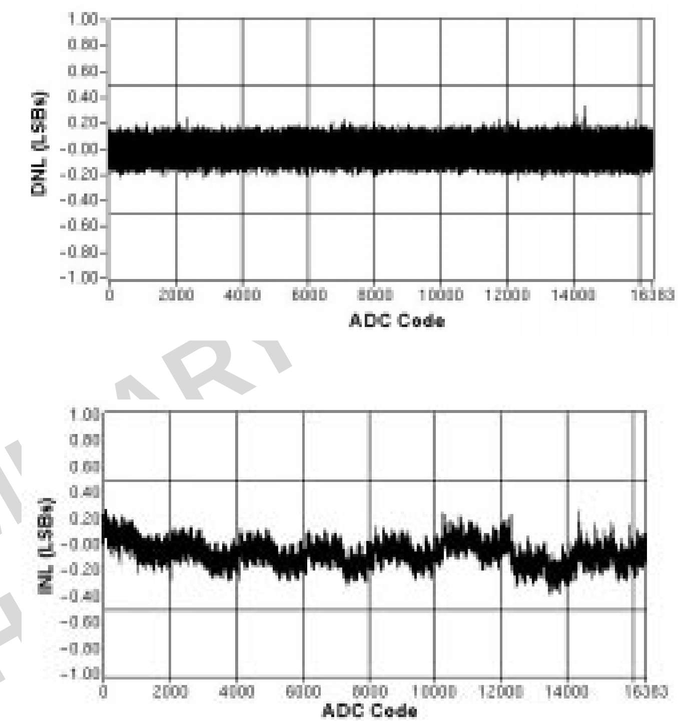


Figure 15. AD7899 Typical DNL and INL Plots

MICROPROCESSOR INTERFACING

The high speed parallel interface of the AD7899 allows easy interfacing to most DSPs and microprocessors. The AD7899 interface of the AD7899 consists of the data lines (DB0 to DB13), $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, $\overline{EOC}$ and BUSY.

AD7899–ADSP-21xx Interface

Figure 20 shows an interface between the AD7899 and the ADSP-21xx. The $\overline{CONVST}$ signal can be generated by the ADSP-21xx or from some other external source. Figure 16 shows the $\overline{CS}$ being generated by a combination of the $\overline{DMS}$ signal and the address bus of the ADSP21xx. In this way the AD7899 is mapped into the data memory spcae of the ADSP21xx.

The AD7899 BUSY/$\overline{EOC}$ line provides an interrupt to the ADSP-21xx when the conversion is complete. The conversion result can then be read from the AD7899 using a read operation. The AD7899 is read using the following instruction

MR0 = DM(ADC)

where MR0 is the ADSP-21xx MR0 register and ADC is the AD7899 address.

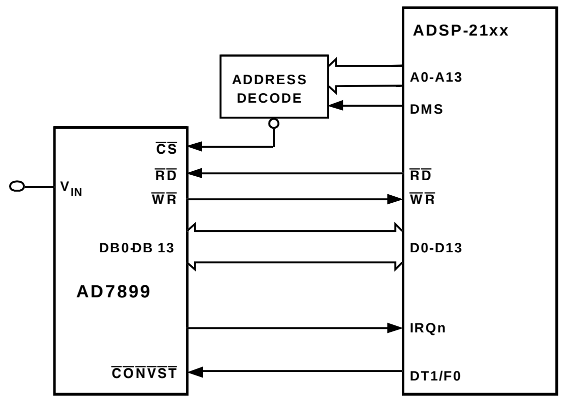


Figure 16. AD7899–ADSP-2100 Interface

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AD7899–TMS320C5x Interface

Figure 17 shows an interface between the AD7899 and the TMS320C5x. As with the previous interfaces, conversion can be initiated from the TMS320C5x or from an external source and the processor is interrupted when the conversion sequence is completed. The $\overline{CS}$ signal to the AD7899 drived from the DS signal and a decode of the address bus. This maps the AD7899 into external data memory. The RD signal from the TMS320 is used to enable the ADC data onto the data bus. The AD7899 has a fast parallel bus so there are no wait state requirements. The following instruction is used to read the conversion results from the AD7899:

IN D,ADC

where D is Data Memory address and ADC is the AD7899 address.

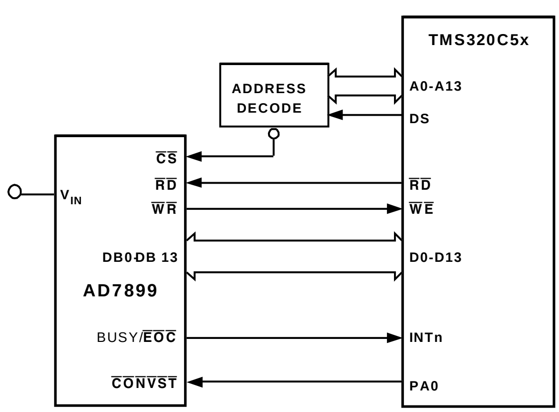
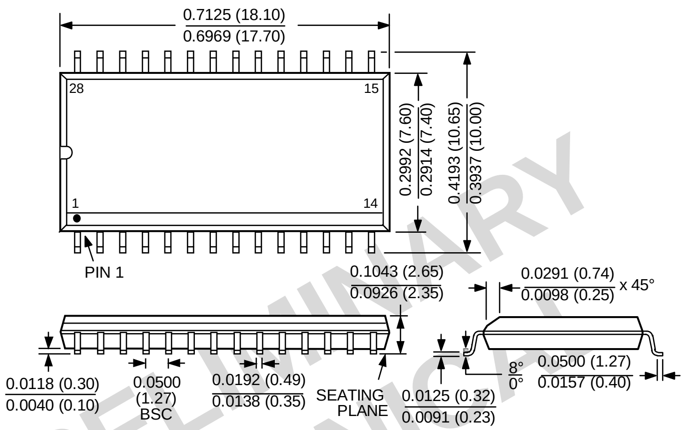


Figure 17. AD7899–TMS320C5x Interface

28-Pin Small Outline Package
(R-28)



28-Pin Shrink Small Outline Package
(RS-28)