REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Inactivate device type 02 for new design. Add device types 03 and 04. Alter electrical performance characteristics and associated waveforms Editorial changes throughout.	1989 APR 24	M. A. Frye

REV																			
SHEET																			
REV	A	A	A	A	A	A	A	A	A	A	A	A							
SHEET	15	16	17	18	19	20	21	22	23	24	25	26							

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
25 FEBRUARY 1988

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MICROPROCESSOR OPTIMIZED FOR DIGITAL SIGNAL PROCESSING, MONOLITHIC SILICON

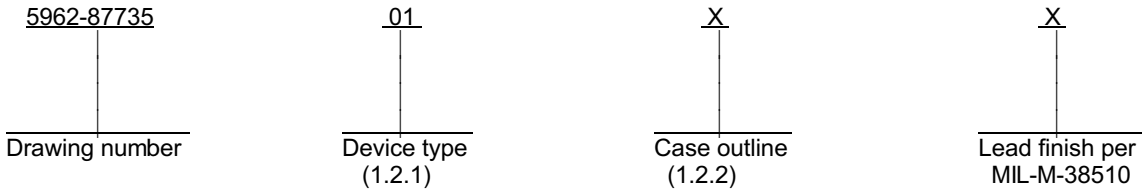
SIZE	CAGE CODE	
A	**67268**	**5962-87735**

SHEET 1 OF 26

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Frequency
01	2100SG	Digital signal processor	6 MHz
02	2100TG	Digital signal processor	8 MHz
03	2100ASG	Digital signal processor	8 MHz
04	2100ATG	Digital signal processor	10 MHz

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	P-BE (100-pin, 1.335" x 1.335" x .345"), pin grid array package

1.3 Absolute maximum ratings.

Supply voltage range	-0.3 V dc to +7 V dc
Input voltage	-0.3 V dc to V_{CC} + 0.3 V dc
Output voltage swing	-0.3 V dc to V_{CC} + 0.3 V dc
Maximum power dissipation (P_D)	.750 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+165°C

1.4 Recommended operating conditions.

Operating supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

	13	12	11	10	9	8	7	6	5	4	3	2	1
N	PMD18	PMD20	PMD21	PMD23	BG	V_{CC}	GND	GND	PMS	TRAP	HALT	RESET	DMA0
M	PMD16	PMD17	PMD19	PMD22	PMRD	BR	DMRD	DMWR	DMS	PMDA	DMACK	GND	DMA2
L	PMD14	PMD15				CLKOUT	CLKIN	PMWR				DMA1	DMA3
K	PMD12	PMD13										DMA4	DMA5
J	PMD10	PMD11										DMA6	GND
H	GND	PMD8	PMD9								DMA7	DMA8	V_{CC}
G	V_{CC}	PMD7	PMD6				Top view pins down				DMA10	DMA11	DMA9
F	PMD5	PMD4	PMD3								DMD15	DMA13	DMA12
E	GND	PMD2										DMD13	DMD14
D	PMD1	PMD0										DMD11	DMD12
C	PMA0	PMA2				PMA11	IRQ2	IRQ0			Index pin	DMD9	DMD10
B	PMA1	PMA4	PMA6	PMA7	PMA9	PMA12	IRQ3	IRQ1	DMD1	DMD3	DMD6	DMD7	DMD8
A	PMA3	PMA5	GND	PMA8	PMA10	PMA13	V_{CC}	GND	DMD0	DMD2	DMD4	DMD5	GND

FIGURE 1. Terminal connections.

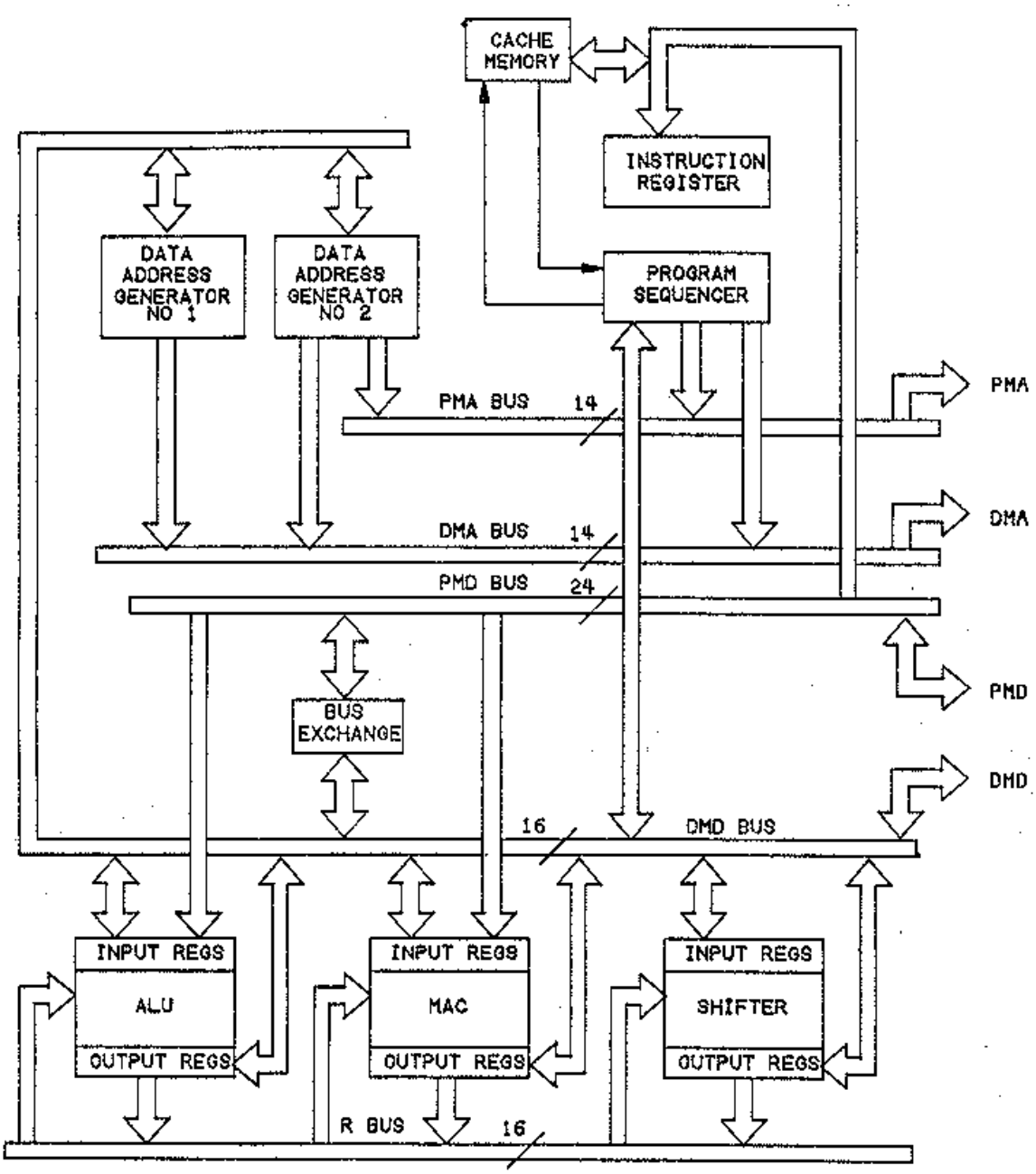


FIGURE 2. Block diagram.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
High level input voltage 1/	V_{IH1}	V_{CC} = maximum	All	1, 2, 3	2.2		V
	V_{IH2}	V_{CC} = maximum, at CLKIN	03,04	1, 2, 3	2.4		V
Low level input voltage 1/	V_{IL}	V_{CC} = minimum	All	1, 2, 3		0.8	V
High level output voltage 2/	V_{OH}	V_{CC} = minimum, I_{OH} = -1 mA	All	1, 2, 3	2.4		V
Low level output voltage 2/	V_{OL}	V_{CC} = minimum, I_{OL} = 4 mA	All	1, 2, 3		0.6	V
High level input current 3/	I_{IH}	V_{CC} = maximum, V_{IN} = 5 V	All	1, 2, 3		10	µA
Low level input current 3/	I_{IL}	V_{CC} = maximum, V_{IN} = 0 V	All	1, 2, 3		10	µA
Three-state leakage current 4/	I_{OZH}	V_{CC} = maximum, $V_{IN} = V_{CC}$ maximum 5/	All	1, 2, 3		10	µA
Three-state leakage current 6/	I_{OZL}	V_{CC} = maximum, V_{IN} = 0 V 5/	All	1, 2, 3		10	µA
Three-state pull-up leakage current 7/	I_{OZL}	V_{CC} = maximum, V_{IN} = 0 V 5/	01 02,03 04	1, 2, 3		150 150 180	µA
Supply current (power down) 8/	I_{CC}	V_{CC} = maximum, V_{IN} = 0 V 5/7/	All	1, 2, 3		15	mA
Supply current (dynamic)	I_{CC}	V_{CC} = maximum, maximum clock rate 9/	01 02,03 04	1, 2, 3		100 130 180	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Input capacitance	C_{IN}	See 4.3.1c V_{IN} = 200 mV T_C = +25°C f_{IN} = 100 kHz	All	4		10	pF
Functional tests		See 4.3.1d		7, 8			
Clock signals	See figure 3 and table III						
CLKIN period 10/	1	A	01 02,03 04	9, 10, 11	40.5 30.5 24.4		ns
CLKIN width low	2	A	01 02,03 04	9, 10, 11	11 8 7		ns
CLKIN width high	3	A	01 02,03 04	9, 10, 11	18 12 9		ns
CLKIN low (3-4) to CLKOUT low	4	B	01 02,03 04	9, 10, 11		34 29 24	ns
CLKIN low (7-8) to CLKOUT high	5	B	01 02,03 04	9, 10, 11		24 20 20	ns
CLKOUT width low 11/	6	A	01 02,03 04	9, 10, 11	60 45 36		ns
Control signals	See figure 3 and table III						
$\overline{\text{RESET}}$ low to CLKIN high	7	B	All	9, 10, 11	2		ns
CLKIN high to $\overline{\text{RESET}}$ high 11/	8	B	01 02,03 04	9, 10, 11	6 6 4	36 26 20	ns
$\overline{\text{RESET}}$ width low 11/	9	A	01 02,03 04	9, 10, 11	170 128 98		ns
$\overline{\text{HALT}}$ valid to CLKIN low (3-4)	10	B	01 02,03,04	9, 10, 11	0 2		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Control signals	See figure 3 and table III						
CLKIN low (3-4) to HALT invalid	11	B	01 02,03,04	9, 10, 11	12 10		ns
CLKIN low (7-8) to TRAP valid	12	B	01 02,03 04	9, 10, 11		25 20 18	ns
CLKIN low (7-8) to IRQ valid	13	B	All	9, 10, 11		1	ns
CLKIN low (7-8) to IRQ invalid	14	B	01 02,03 04	9, 10, 11	21 17 14		ns
BUS request/grant	See figure 3 and table III						
$\overline{BR}$ valid to CLKIN low (3-4)	15	B	01,02,03 04	9, 10, 11	1 4		ns
CLKIN low (3-4) to $\overline{BR}$ invalid	16	B	01 02,03,04	9, 10, 11	10 7		ns
CLKIN low (3-4) to $\overline{BG}$ low	17	B	01 02,03 04	9, 10, 11		38 30 26	ns
CLKIN low (7-8) to $\overline{BG}$ high	18	B	01 02,03 04	9, 10, 11		31 25 24	ns
$\overline{BG}$ low to xMxx disable 12/	19	C	01 02,03 04	9, 10, 11		22 17 16	ns
xMxx enable to $\overline{BG}$ high 12/	20	D	01 02,03,04	9, 10, 11		12 10	ns
$\overline{BR}$ low to $\overline{BG}$ low during RESET	21	A	01 02,03 04	9, 10, 11		28 23 18	ns
$\overline{BR}$ high to $\overline{BG}$ high during RESET	22	A	01 02,03 04	9, 10, 11		21 18 16	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Program memory	See figure 3 and table III						
$\overline{PMRD}$ width low 11/	23	A	01 02,03 04	9, 10, 11	60 45 36		ns
PMA valid to $\overline{PMRD}$ low 11/	24	A	01 02,03 04	9, 10, 11	18 14 6		ns
$\overline{PMRD}$ high to PMA invalid 11/	25	A	01 02,03 04	9, 10, 11	20 10 8		ns
PMDA valid to PMRD low 11/	26	A	01 02,03 04	9, 10, 11	41 24 20		ns
$\overline{PMRD}$ high to PMDA invalid 11/	27	A	01 02,03 04	9, 10, 11	22 12 10		ns
$\overline{PMS}$ valid to PMRD low 11/	28	A	01 02,03 04	9, 10, 11	55 40 32		ns
$\overline{PMRD}$ high to PMS invalid 11/	29	A	01 02,03,04	9, 10, 11	16 8		ns
$\overline{PMRD}$ low to PMD in valid 11/	30	A	01 02,03 04	9, 10, 11		45 33 28	ns
PMA valid to PMD in valid 11/	31	A	01 02,03 04	9, 10, 11		57 50 46	ns
$\overline{PMS}$ valid to PMD in valid 11/	32	A	01 02,03 04	9, 10, 11		90 65 50	ns
$\overline{PMRD}$ high to PMD in invalid	33	A	All	9, 10, 11	0		ns
$\overline{PMWR}$ width low 11/	34	A	01 02,03 04	9, 10, 11	60 45 36		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Program memory	See figure 3 and table III						
PMA valid to PMWR low 11/	35	A	01 02,03 04	9, 10, 11	16 12 8		ns
$\overline{\text{PMWR}}$ high to PMA invalid 11/	36	A	01 02,03 04	9, 10, 11	19 10 8		ns
PMDA valid to PMWR low 11/	37	A	01 02,03 04	9, 10, 11	39 28 20		ns
$\overline{\text{PMWR}}$ high to PMDA invalid 11/	38	A	01 02,03 04	9, 10, 11	21 12 10		ns
$\overline{\text{PMS}}$ valid to PMWR low 11/	39	A	01 02,03 04	9, 10, 11	54 40 32		ns
$\overline{\text{PMWR}}$ high to PMS invalid 11/	40	A	01 02,03 04	9, 10, 11	14 8 6		ns
$\overline{\text{PMWR}}$ low to PMD out enable 11/	41	D	01 02,03,04	9, 10, 11	15 8		ns
$\overline{\text{PMWR}}$ high to PMD out disable 11/	42	C	01 02,03 04	9, 10, 11		43 38 32	ns
$\overline{\text{PMWR}}$ low to PMD out valid 11/	43	A	01 02,03 04	9, 10, 11		40 32 29	ns
$\overline{\text{PMWR}}$ high to PMD out invalid 11/	44	A	01 02,03 04	9, 10, 11	21 12 10		ns
PMD out valid to PMWR high 11/	45	A	01 02,03 04	9, 10, 11	33 25 16		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Data memory	See figure 3 and table III						
$\overline{DMRD}$ width low 11/	46	A	01 02,03 04	9, 10, 11	60 45 36		ns
DMA valid to $\overline{DMRD}$ low 11/	47	A	01 02,03 04	9, 10, 11	21 14 6		ns
$\overline{DMRD}$ high to DMA invalid 11/	48	A	01 02,03 04	9, 10, 11	19 10 8		ns
$\overline{DMS}$ valid to $\overline{DMRD}$ low	49	A	01 02,03 04	9, 10, 11	35 27 18		ns
$\overline{DMRD}$ high to $\overline{DMS}$ invalid	50	A	01 02,03 04	9, 10, 11	21 10 8		ns
$\overline{DMRD}$ low to DMACK valid 11/	51	A	01 02,03 04	9, 10, 11		31 21 16	ns
DMA valid to DMACK valid 11/	52	A	01 02,03 04	9, 10, 11		57 42 30	ns
$\overline{DMRD}$ low to DMD in valid 11/	53	A	01 02,03 04	9, 10, 11		55 37 28	ns
DMA valid to DMD in valid 11/	54	A	01 02,03 04	9, 10, 11		79 59 46	ns
$\overline{DMS}$ valid to DMD in valid	55	A	01 02,03 04	9, 10, 11		96 67 50	ns
$\overline{DMRD}$ high to DMD in invalid	56	A	All	9, 10, 11	0		ns
$\overline{DMWR}$ width low 11/	57	A	01 02,03 04	9, 10, 11	60 45 36		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Data memory	See figure 3 and table III						
DMA valid to DMWR low 11/	58	A	01 02,03 04	9, 10, 11	24 17 8		ns
$\overline{\text{DMWR}}$ high to DMA invalid 11/	59	A	01 02,03 04	9, 10, 11	19 10 8		ns
$\overline{\text{DMS}}$ valid to $\overline{\text{DMWR}}$ low	60	A	01 02,03 04	9, 10, 11	37 28 20		ns
$\overline{\text{DMWR}}$ high to $\overline{\text{DMS}}$ invalid	61	A	01 02,03 04	9, 10, 11	22 8 6		ns
$\overline{\text{DMWR}}$ low to DMD out enable 11/	62	D	01 02,03 04	9, 10, 11	14 8 8		ns
$\overline{\text{DMWR}}$ high to DMD out disable 11/	63	C	01 02,03 04	9, 10, 11		40 38 32	ns
$\overline{\text{DMWR}}$ low to DMD out valid 11/	64	A	01 02,03 04	9, 10, 11		38 32 29	ns
$\overline{\text{DMWR}}$ high to DMD out valid 11/	65	A	01 02,03 04	9, 10, 11	19 12 10		ns
DMD out valid to DMWR high 11/	66	A	01 02,03 04	9, 10, 11	33 25 16		ns
$\overline{\text{DMWR}}$ low to DMACK valid 11/	67	A	01 02,03 04	9, 10, 11		31 20 16	ns
DMACK width 11/	68	A	01 02,03 04	9, 10, 11	81 61 50		ns
DMACK low to CLKOUT high 11/	69	A	01 02,03 04	9, 10, 11	45 37 36		ns

See footnotes on next page.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Data memory	See figure 3 and table III						
CLKOUT low to DMACK high 11/	70	A	01 02,03 04	9,10,11		28 19 17	ns

1/ Applies to pins: PMD_{0-23}, DMD_{0-15}, BR, $\overline{IRQ}_{0-3}$, DMACK, $\overline{RESET}$, $\overline{HALT}$, $\overline{CLKIN}$ (49 input pins).

2/ Applies to pins: PMA_{0-13}, $\overline{PMS}$, $\overline{PMD}_{0-23}$, $\overline{PMRD}$, $\overline{PMWR}$, $\overline{PMDA}$, BG, DMA_{0-13}, DMS, $\overline{DMD}_{0-15}$, DMRD, DMWR, TRAP, CLKOUT (78 output pins).

3/ Applies to pins: BR, $\overline{IRQ}_{0-3}$, DMACK, $\overline{RESET}$, $\overline{HALT}$, $\overline{CLKIN}$ (9 input only pins).

4/ Applies to pins: PMA_{0-13}, $\overline{PMS}$, $\overline{PMD}_{0-23}$, $\overline{PMRD}$, $\overline{PMWR}$, $\overline{PMDA}$, DMA_{0-13}, DMS, $\overline{DMD}_{0-15}$, DMRD, $\overline{DMWR}$ (75 three-stateable pins).

5/ Additional test conditions: V_{IN} = 0 V on BR and $\overline{RESET}$, $\overline{CLKIN}$ active, forces three-state condition.

6/ Applies to pins: PMA_{0-13}, PMDA, DMA_{0-13}, (29 three-stateable pins without pullup).

7/ Applies to pins: PMD_{0-23}, $\overline{PMS}$, $\overline{PMRD}$, $\overline{PMWR}$, $\overline{DMD}_{0-15}$, DMS, $\overline{DMRD}$, $\overline{DMWR}$ (46 three-stateable pins with pullup).

8/ Power down refers to an idle state. While the device does not have any special standby or low-power mode, these conditions represent a low-power consumption state.

9/ Additional test conditions: Outputs loaded TTL loads with 100 pF capacitance, V_{IH} = 2.4 V, V_{IL} = 0.4 V, clock rate = 6.144 MHz for device type 01, 8.192 MHz for device types 02 and 03, 10.24 MHz for device type 04.

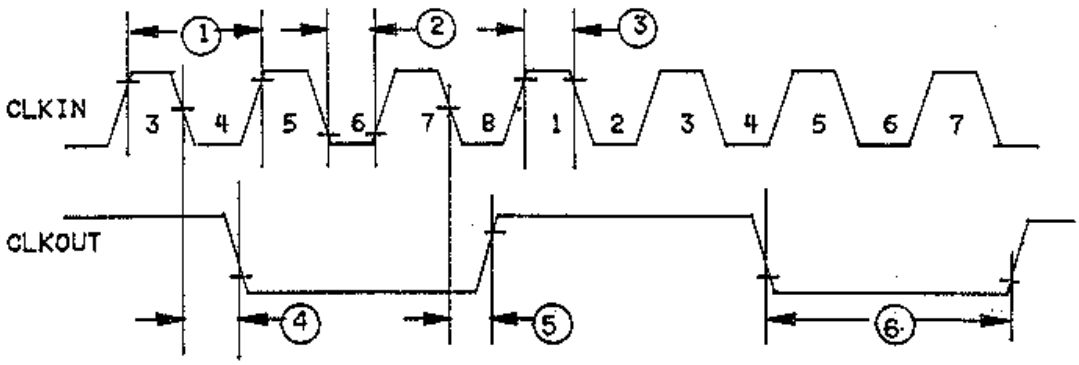
10/ Rise and fall times $\le$ 5 ns.

11/ These items are cycle time dependent.

12/ xMxx refers to PMA_{0-13}, $\overline{PMS}$, $\overline{PMRD}$, $\overline{PMWR}$, $\overline{PMDA}$, DMA_{0-13}, DMS, $\overline{DMRD}$, and $\overline{DMWR}$.

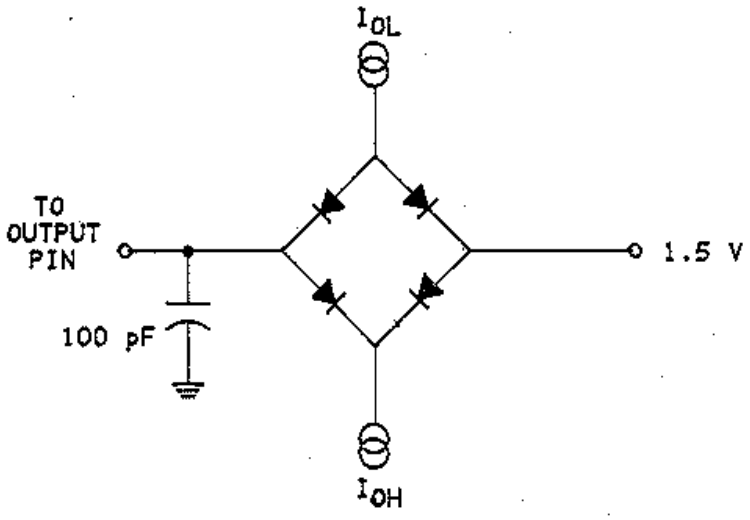
3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.



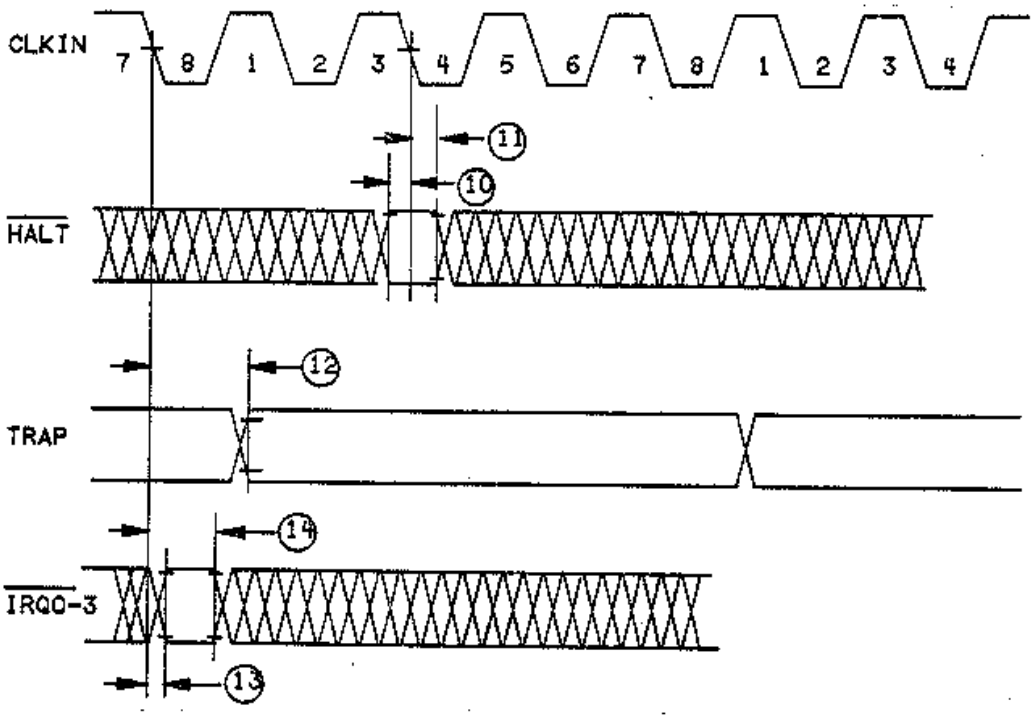
NOTE: The processor cycle is divided into eight internal states determined by the rising and falling edges of CLKIN. CLKOUT is synchronized to the processor states as shown above.

Clock signals



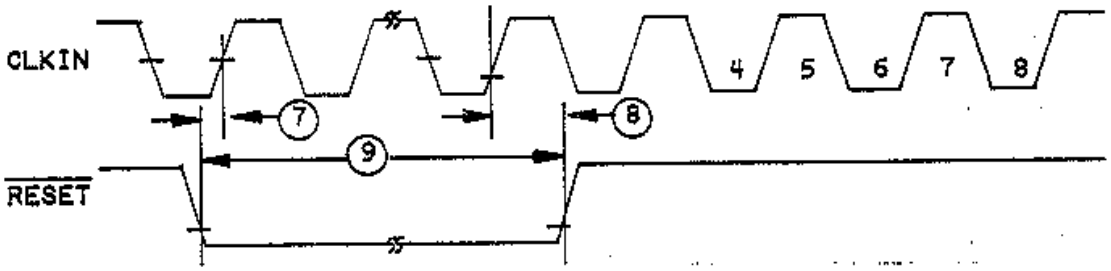
Normal load for ac measurements.

FIGURE 3. AC test circuit and waveforms.



NOTE: The control signals are shown in relationship to the processor states in which they are recognized or asserted as defined by CLKIN. There is no implied relationship between HALT, TRAP, and $\overline{IRQ}_{0-3}$.

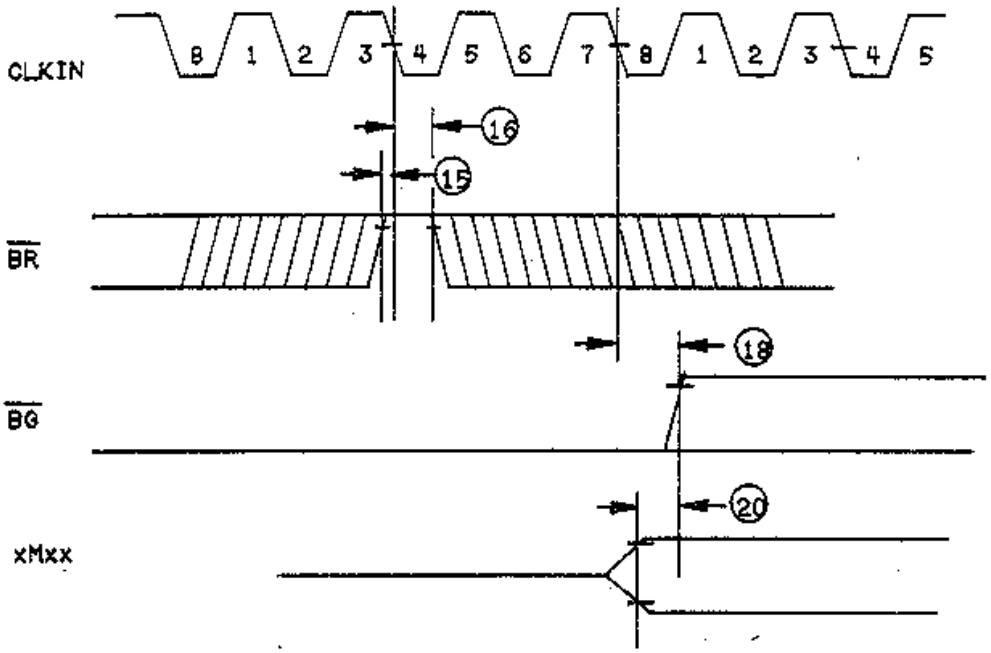
Control signals



NOTE: The $\overline{RESET}$ signal determines the phase of the processor cycle. The processor starts from state 4 after the release of the $\overline{RESET}$ signal.

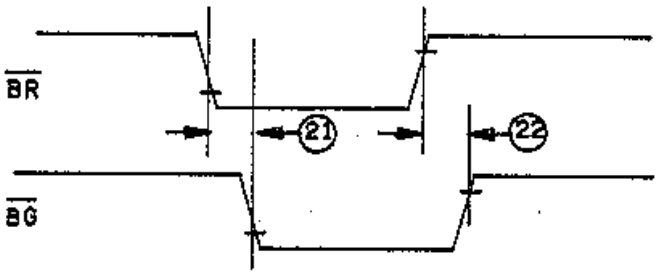
$\overline{RESET}$ signal

FIGURE 3. AC test circuit and waveforms - Continued.



NOTE: xMxx refers to PMA_{0-13}, $\overline{PMS}$, $\overline{PMRD}$, $\overline{PMWR}$, PMDA, DMA_{0-13}, $\overline{DMS}$, $\overline{DMRD}$, and $\overline{DMWR}$.

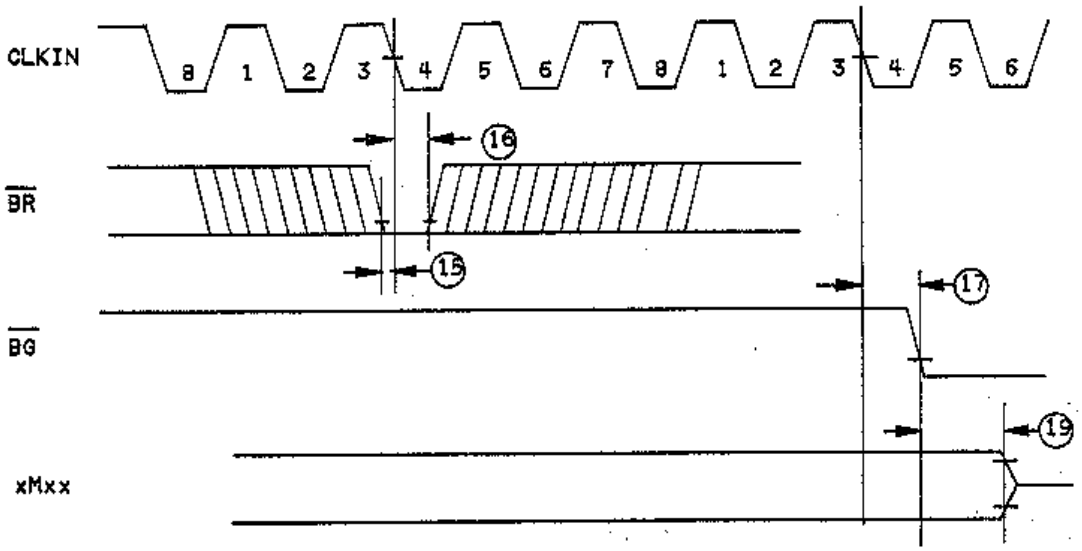
Bus request negated



NOTE: During $\overline{RESET}$, the processor bus ignores the CLKIN signal and therefore the bus request/grant signals operate asynchronously.

Bus request grant with $\overline{RESET}$ low

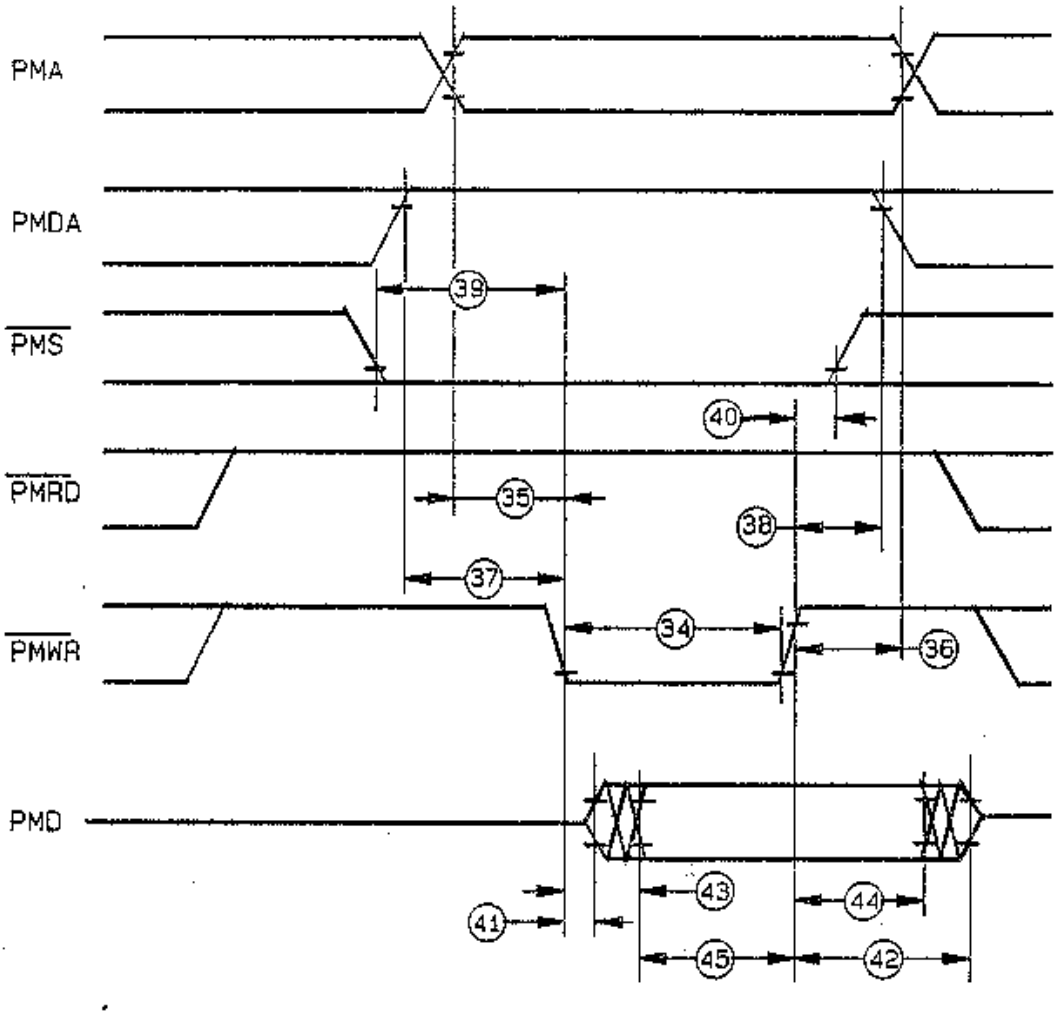
FIGURE 3. AC test circuit and waveforms - Continued.



NOTE: xMxx refers to PMA_{0-13}, $\overline{PMS}$, $\overline{PMRD}$, $\overline{PMWR}$, PMDA, DMA_{0-13}, $\overline{DMS}$, $\overline{DMRD}$, and $\overline{DMWR}$.

Bus request asserted

FIGURE 3. AC test circuit and waveforms - Continued.



Program memory write

FIGURE 3. AC test circuit and waveforms - Continued.

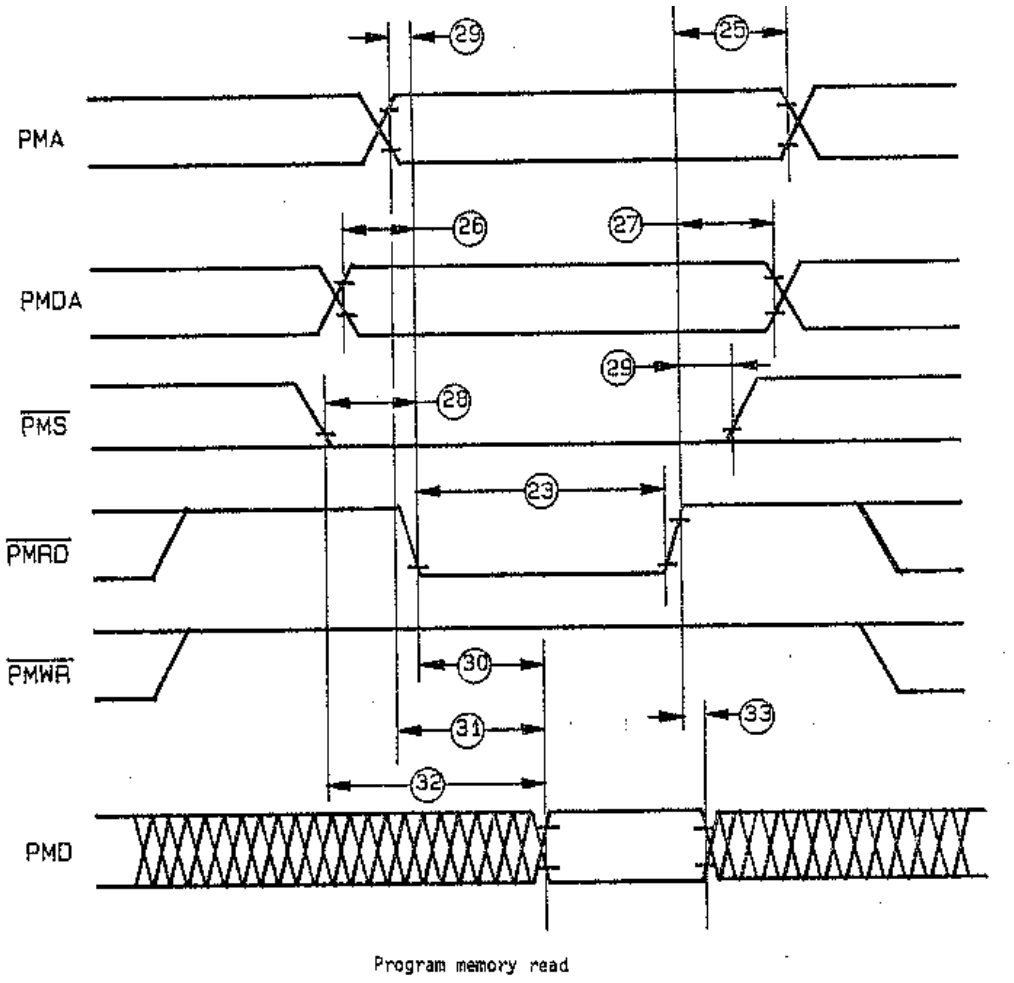


FIGURE 3. AC test circuit and waveforms - Continued.

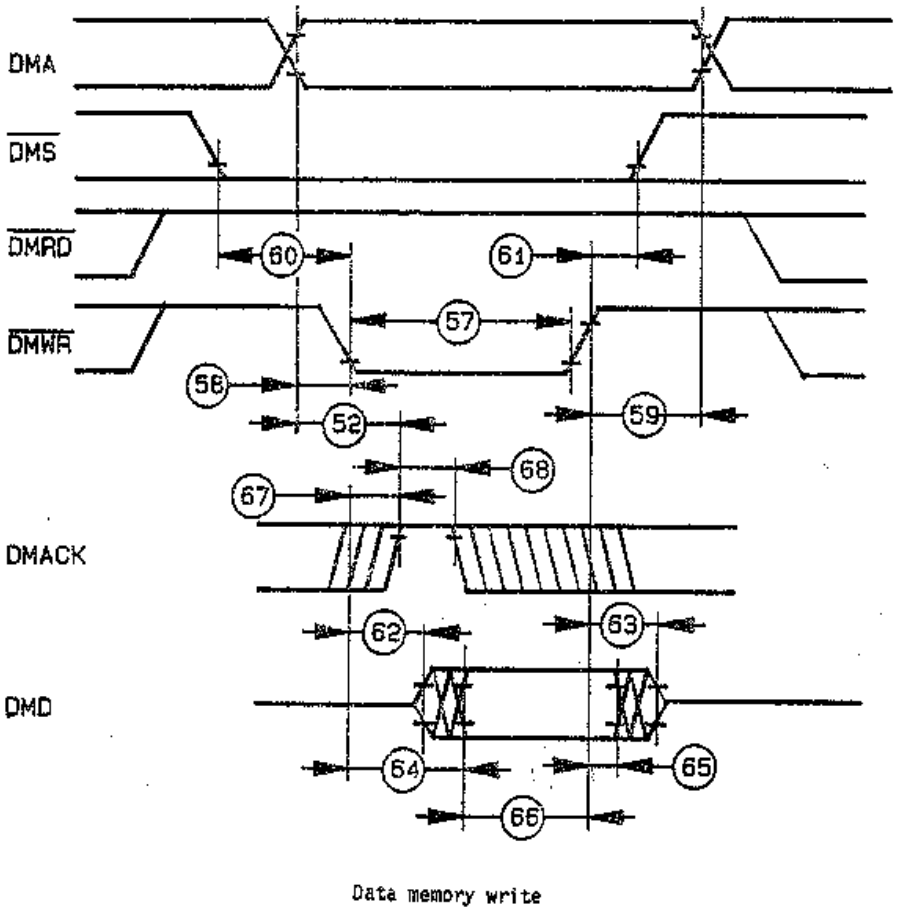


FIGURE 3. AC test circuit and waveforms - Continued.

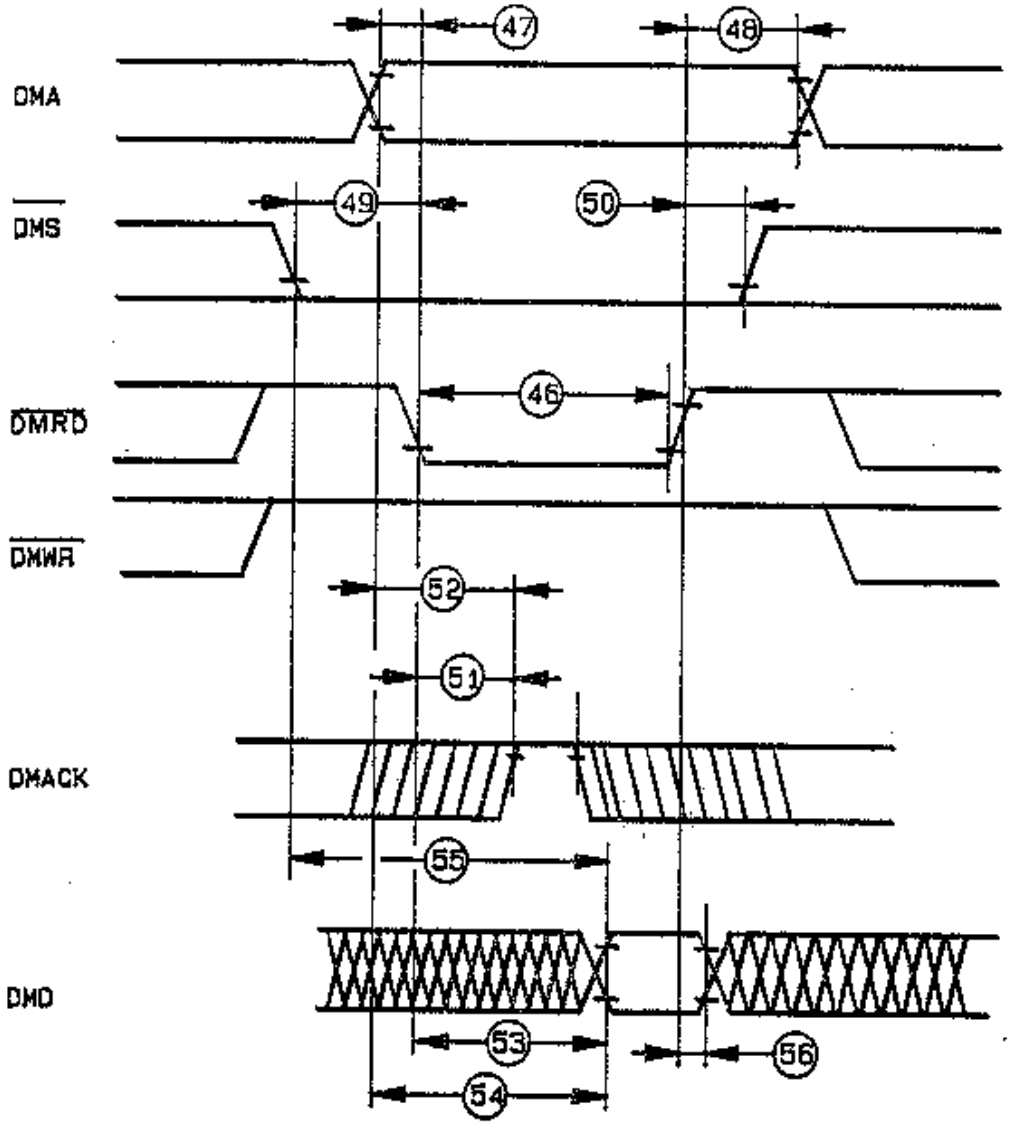


FIGURE 3. AC test circuit and waveforms - Continued.

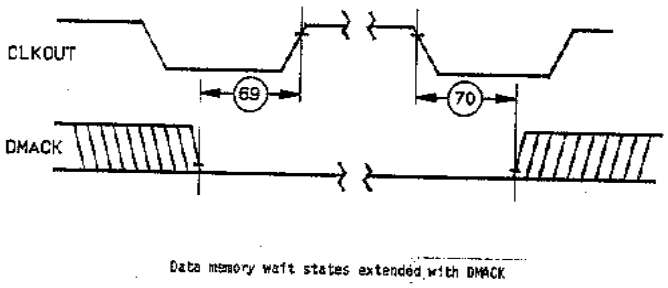


FIGURE 3. AC test circuit and waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of three devices with zero rejects shall be required.

d. Subgroups 7 and 8 tests shall verify the instruction set. The instruction set forms a part of the vendor's test tape and shall be maintained and available for review from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883 conditions:

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method, 5005, table I)
Interim electrical parameters (method 5004)	1, 7, 9
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8, 9, 10, 11

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

TABLE III. Test codes.

Code	Test type	Level references
A	Inputs, outputs	Low = 0.8 V, high = 2.0 V
B	CLKIN To or from inputs, outputs	1.5 V Low = 0.8 V, high = 2.0 V
C	Output To output disable	Low = 0.8 V, high = 2.0 V Low = V_{OL} +0.5 V, high = V_{OH} -0.5 V
D	Output To or from output enable	Low = 0.8 V, high = 2.0 V Low = V_T -0.1 V, high = V_T +0.1 V 1/

1/ V_T = 1.5 V, the voltage to which three-stated outputs are forced.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8773501XX	51640	ADSP-2100SG/883B
5962-8773502XX	2/	ADSP-2100TG/883B
5962-8773503XX	51640	ADSP-2100ASG/883B
5962-8773504XX	51640	ADSP-2100ATG/883B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Inactive for new design. Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
51640	Analog Devices, Incorporated Semiconductor Division 804 Woburn Street Wilmington, MA 01887