REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add vendor, CAGE 01295 for devices 01EX and 012X. Update format. Editorial changes throughout.	1990 APR 9	M. A. Frye

REV																			
SHEET																			
REV	A																		
SHEET	15																		

REV STATUS OF SHEETS														
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
14 DECEMBER 1987

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, CMOS, 8-BIT MULTIPLYING DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON

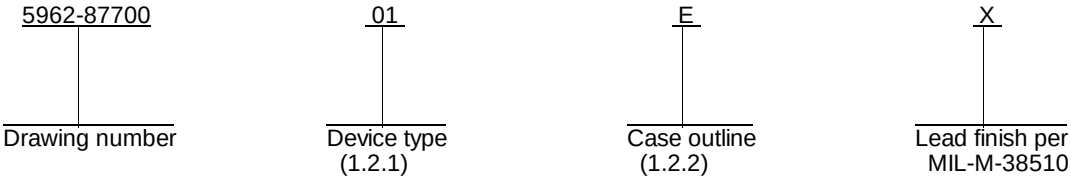
SIZE	CAGE CODE	
A	67268	5962-87700

SHEET 1 OF 15

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	7524	CMOS 8-bit multiplying buffered DAC with .5 LSB
02	7524	CMOS 8-bit multiplying buffered DAC with .25 LSB
03	7524	CMOS 8-bit multiplying buffered DAC with .125 LSB

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

V_{DD} to GND	-.3 V, +17 V
V_{RFB} to GND	±25 V
Digital input voltage to GND	-0.3 V to V_{DD}
V_{REF} to GND	±25 V
V_{OUT1}, V_{OUT2}, 0 to GND	-0.3 V to V_{DD}
Power dissipation (P_D):	
Up to +75°C	450 mW
Derates above +75°C	6 mW/°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Thermal resistance, junction-to-ambient (θ_{JA})	120°C/W

1.4 Recommended operating conditions.

Ambient operating temperature range (T_A)	-55°C to +125°C
Supply voltage range (V_{DD})	+5 V to +15 V

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections and mode selection. The terminal connections and mode selection shall be as specified on figure 1.

3.2.2 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Resolution	RES	V_{DD} = +5 V		All	1, 2, 3	8		Bits
		V_{DD} = +15 V		All	1, 2, 3	8		
Relative accuracy	RA	V_{DD} = +5 V		All	1, 2, 3		±.5	LSB
		V_{DD} = +15 V		01	1, 2, 3		±.5	
				02	1		±.5	
					2, 3		±.25	
		V_{DD} = +15 V 2/ T_A = +25°C		02	12		±.25	
		V_{DD} = +15 V		03	1		±.5	
					2, 3		±.125	
		V_{DD} = +15 V 2/ T_A = +25°C		03	12		±.125	
Gain error 3/	A_E		V_{DD} = +5 V	All	1		±1.0	%FSR
					2, 3		±1.4	
			V_{DD} = +15 V	All	1		±0.5	
					2, 3		±0.6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Power supply rejection	PSRR	ΔV_{DD} = ±10%	V_{DD} = +5 V	All	1		±.08	%/%
					2, 3		±.16	
			V_{DD} = +15 V	All	1		±.02	
					2, 3		±.04	
Output leakage current I_{OUT1}	I_{OL}	DB0 - DB7 = 0 V, $\overline{WR}$ = $\overline{CS}$ = 0 V	V_{DD} = +5 V	All	1		±50	nA
					2, 3		±400	
			V_{DD} = +15 V	All	1		±50	
					2, 3		±200	
Output leakage current I_{OUT2}		DB0 - DB7 = V_{DD}, $\overline{WR}$ = $\overline{CS}$ = 0 V	V_{DD} = +5 V	All	1		±50	
					2, 3		±400	
			V_{DD} = +15 V	All	1		±50	
					2, 3		±200	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Input resistance V_{REF} pin	R_{IN}	= +5 V	V_{DD}	All	1, 2, 3	5	20	kΩ
			V_{DD} = +15 V	All	1, 2, 3	5	20	
Digital input high voltage	V_{IH}		V_{DD} = +5 V	All	1, 2, 3	2.4		V
			V_{DD} = +15 V	All	1, 2, 3	13.5		
Digital input low voltage	V_{IL}		V_{DD} = +5 V	All	1, 2, 3		0.8	
			V_{DD} = +15 V	All	1, 2, 3		1.5	
Digital input leakage current	I_{IN}	V_{IN} = 0 V or V_{DD}	VDD = +5 V	All	1		±1	µA
					2,3		±10	
			V_{DD} = +15 V	All	1		±1	
					2,3		±10	
Supply current	I_{DD}	All digital inputs V_{IL} or V_{IH}	V_{DD} = +5 V	All	1, 2, 3		2	mA
			V_{DD} = +15 V	All	1, 2, 3		2	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Supply current	I_{DD}	All digital inputs = 0 V or V_{DD}	V_{DD} = +5 V	All	1		100	µA
					2, 3		500	
			V_{DD} = +15 V	All	1		100	
					2, 3		500	
Gain temperature coefficient	TC_{AE}	4/	V_{DD} = +5 V	All	1, 2, 3		±40	ppm/°C
			V_{DD} = +15 V	All	1, 2, 3		±10	
Feedthrough error	FT	4/ 5/ V_{REF} = +10 V, 100 kHz sinewave; DB0 - DB7 = 0 V; $\overline{WR}$ = $\overline{CS}$ = 0 V	V_{DD} = +5 V	All	4, 5, 6		50	mV p-p
			V_{DD} = +15 V	All	4, 5, 6		50	
Digital input capacitance	C_{IN}	V_{IN} = 0 V 6/ DB0-DB7 T_A = +25°C	V_{DD} = +5 V	All	4		5	pF
			V_{DD} = +15 V	All	4		20	
		V_{IN} = 0 V 6/ $\overline{WR}$, $\overline{CS}$ T_A = +25°C	V_{DD} = +5 V	All	4		5	
			V_{DD} = +15 V	All	4		20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Output capacitance	C_{OUT1}	6/ $\overline{DB0}$ - $\overline{DB7}$ = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0 V T_A = +25°C	V_{DD} = +5 V	All	4		120	pF
			V_{DD} = +15 V	All	4		120	
Output capacitance	C_{OUT2}		V_{DD} = +5 V	All	4		30	
			V_{DD} = +15 V	All	4		30	
Output capacitance	C_{OUT1}	6/ $\overline{DB0}$ - $\overline{DB7}$ = 0 V; $\overline{WR}$ = $\overline{CS}$ = 0 V T_A = +25°C	V_{DD} = +5 V		4		30	
			V_{DD} = +15 V		4		30	
Output capacitance	C_{OUT2}		V_{DD} = +5 V	All	4		120	
			V_{DD} = +15 V	All	4		120	
Chip select to write setup time	t_{CS}	7/	V_{DD} = +5 V	All	9,10,11	240		ns
			V_{DD} = +15 V	All	9,10,11	150		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Chip select to write hold time	t_{CH}	7/	V_{DD} = +5 V	All	9,10,11	0		ns
			V_{DD} = +15 V	All	9,10,11	0		
Write pulse width	t_{WR}	7/ $t_{CS} \ge t_{WR}$, $t_{CH} \ge 0$	V_{DD} = +5 V	All	9,10,11	240		
			V_{DD} = +15 V	All	9,10,11	150		
Data setup time	t_{DS}	7/	V_{DD} = +5 V	All	9,10,11	170		
			V_{DD} = +15 V	All	9,10,11	100		
Data hold time	t_{DH}	7/	V_{DD} = +5 V	All	9,10,11	10		
			V_{DD} = +15 V	All	9,10,11	10		
Output current settling time	t_{SL}	4/ 8/	V_{DD} = +5 V	All	9,10,11		500	
			V_{DD} = +15 V	All	9,10,11		350	

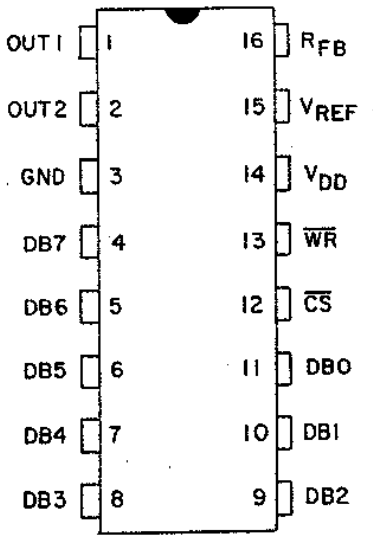
1/ $V_{OUT1} = V_{OUT2} = 0$ V; V_{REF} = +10 V unless otherwise specified.
2/ See 4.3.1d.
3/ Measured using internal feedback R_{FB} and includes effect of leakage current and gain TC.
4/ Guaranteed, if not tested.
5/ Feedthrough error can be reduced by connecting the metal lid to ground.
6/ See 4.3.1c.
7/ Timing in accordance with figure 2.
8/ R_{OUT1} load = 100Ω, C_{EXT} = 13 pF.

$\overline{WR}$, $\overline{CS}$ = 0 V, DBO-DB7 = 0 V to V_{DD} or V_{DD} to 0 V.

Extrapolated: t_s (±1/2 LSB) = t_{pD} + 6.2 T, where T = the measured first time constant of the final RC delay.

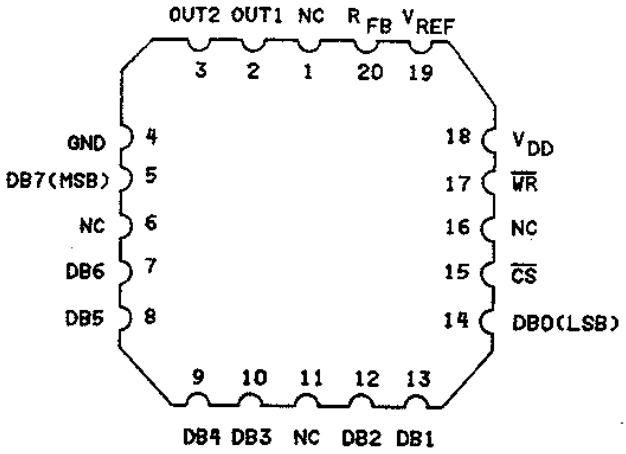
Device types 01, 02, and 03

Case E



Device types 01, 02, and 03

Case 2

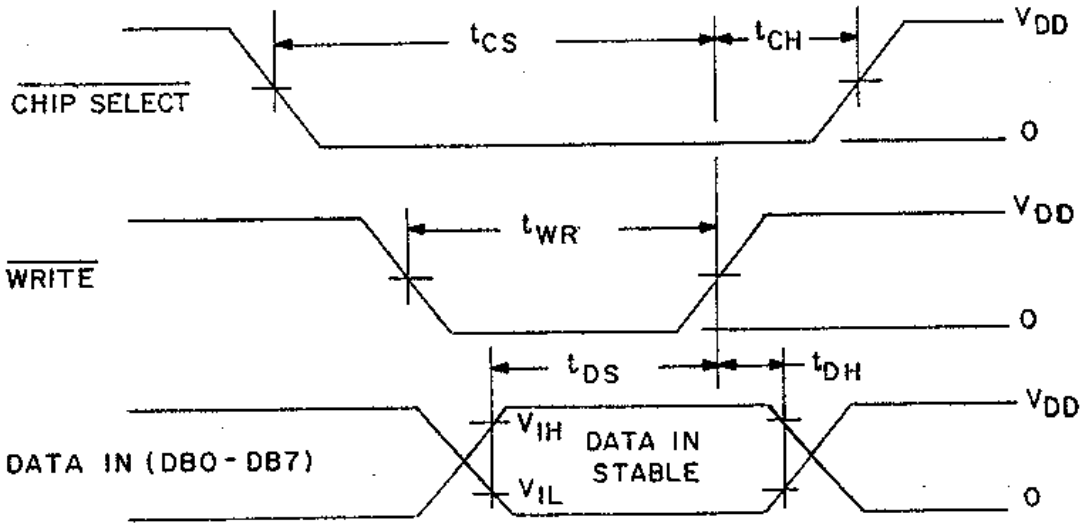


Mode selection table

$\overline{CS}$	$\overline{WR}$	Mode	DAC response
L	L	Write	DAC responds to data bus (DBO - DB7) inputs
H	X	Hold	Data bus (DBO - DB7) is locked out
X	H	Hold	DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed HIGH state.

L = Low state
H = High state
X = Don't care

FIGURE 1. Terminal connections and mode selection.



NOTES:

1. All input signal rise and fall times measured from 10 percent to 90 percent to V_{DD}. V_{DD} = +5 V, $t_r = t_f$ = 20 ns; V_{DD} = +15 V, $t_r = t_f$ = 40 ns.
2. Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.
3. $t_{DS} + t_{DH}$ is approximately constant at 145 ns minimum at +25°C, V_{DD} = +5 V and t_{wr} = 170 ns minimum. The devices are specified for a minimum t_{DH} of 10 ns, however, in applications where t_{DH} > 10 ns, t_{DS} may be reduced accordingly up to the limit t_{DS} = 65 ns, t_{DH} = 80 ns.

FIGURE 2. Write cycle timing diagram.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. Optional subgroup 12 is used for grading and part selection at +25°C, and it is not included in PDA.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.

d. Optional subgroup 12 is used for grading and part selection at +25°C.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,12
Group A test requirements (method 5005)	1,2,3,4,5,6, 9,10**,11**, 12
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved sources of supply listed below are for information purposes only and are current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8770001EX	24355 06665 01295	AD7524SQ/883B PM7524BQ/883 AD7524MJ
5962-87700012X	24355 06665 01295	AD7524SE/883B PM7524BRC/883 AD7524MFK
5962-8770002EX	24355 06665	AD7524TQ/883B PM7524BQ/883
5962-87700022X	24355 06665	AD7524TE/883B PM7524BRC/883
5962-8770003EX	24355 06665	AD7524UQ/883B PM7524AQ/883
5962-87700032X	24355 06665	AD7524UE/883B PM7524ARC/883

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallax, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448
06665	Precision Monolithics, Incorporated 1500 Space Park Drive P.O. Box 58020 Santa Clara, CA 95050-8020
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 804 Woburn Street Wilmington, MA 01887