

<b>NOTICE OF REVISION (NOR)</b>		1. DATE (YYMMDD) 94-08-12	Form Approved OMB No. 0704-0188
This revision described below has been authorized for the document listed.			
Public reporting burden for this collection is estimated to average 2 hours per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503. PLEASE DO NOT RETURN YOUR COMPLETED FORM TO EITHER OF THESE ADDRESSES. RETURN COMPLETED FORM TO THE GOVERNMENT ISSUING CONTRACTING OFFICER FOR THE CONTRACT/ PROCURING ACTIVITY NUMBER LISTED IN ITEM 2 OF THIS FORM.			2. PROCURING ACTIVITY NO.
			3. DODAAC
4. ORIGINATOR	b. ADDRESS (Street, City, State, Zip Code)  Defense Electronics Supply Center 1507 Wilmington Pike Dayton, OH 45444-5270	5. CAGE CODE  67268	6. NOR NO.  5962-R231-94
a. TYPED NAME (First, Middle Initial, Last)		7. CAGE CODE  67268	8. DOCUMENT NO.  <b>5962-87591</b>
9. TITLE OF DOCUMENT  MICROCIRCUIT, LINEAR, HIGH-SPEED, ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON		10. REVISION LETTER	
		a. CURRENT  A	b. NEW  B
11. ECP NO.  5962-87591ECP-1			
12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES  ALL			
13. DESCRIPTION OF REVISION  Sheet 1: Revisions ltr column; add "B". Revisions description column; add "Changes in accordance with NOR 5962-R231-94". Revisions date column; add "94-08-12". Revision level block; delete "A" and substitute "B". Rev status of sheets; For sheets 1, 4, 5, and 6, delete "A" and substitute "B".  Sheet 4: TABLE I. Internal reference voltage output test. Under the max limit column, delete "+5.2 V" and substitute "-5.2 V". Revision level block; delete "A" and substitute "B".  Sheet 5: TABLE I. Data access time after RD, (C <sub>L</sub> = 60 pF) test. Add new footnote "4/" which states; "If not tested, shall be guaranteed to the limits specified in table I herein." Revision level block; delete "A" and substitute "B".  Sheet 6: TABLE I. Bus relinquish time test. Under the symbol column, renumber footnote "4/" as footnote "5/" which states; "Time t <sub>7</sub> is defined as the time required for the delta lines to change 0.5 V when loaded with the circuits of figure 3." Delay between successive read operations test. Under group A subgroups column, add subgroup "9". Add new footnote "4/" which states; "If not tested, shall be guaranteed to the limits specified in table I herein." Renumber footnote "4/" as footnote "5/" which states; "Time t <sub>7</sub> is defined as the time required for the delta lines to change 0.5 V when loaded with the circuits of figure 3." Revision level block; delete "A" and substitute "B".			
14. THIS SECTION FOR GOVERNMENT USE ONLY			
a. (X one)	X	(1) Existing document supplemented by the NOR may be used in manufacture.	
		(2) Revised document must be received before manufacturer may incorporate this change.	
		(3) Custodian of master document shall make above revision and furnish revised document.	
b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT DESC-ELDS		c. TYPED NAME (First, Middle Initial, Last) MICHAEL A. FRYE	
d. TITLE BRANCH, CHIEF MICROELECTRONICS	e. SIGNATURE MICHAEL A. FRYE		f. DATE SIGNED (YYMMDD) 94-08-12
15a. ACTIVITY ACCOMPLISHING REVISION DESC-ELDS	b. REVISION COMPLETED (Signature) RICK C. OFFICER		c. DATE SIGNED (YYMMDD) 94-08-12

**REVISIONS**

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correct title to read ANALOG TO DIGITAL. Change conditions for timing tests, table I. Change figure 3. Editorial changes throughout	1990 JAN 24	M. A. Frye

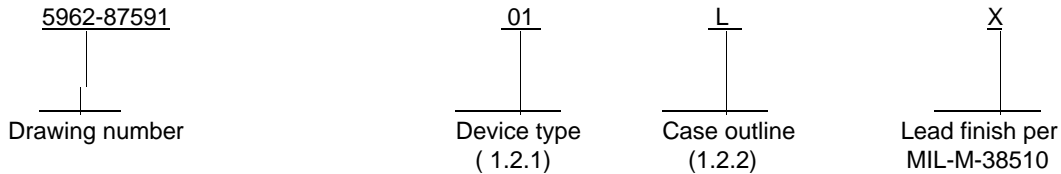
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REV																					
SHEET																					
REV	A	A	A																		
SHEET	15	16	17																		
REV STATUS OF SHEETS				REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
				SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14			
PMIC N/A				PREPARED BY Joseph A. Kerby				<p align="center"><b>DEFENSE ELECTRONICS SUPPLY CENTER</b></p> <p align="center"><b>DAYTON, OHIO 45444</b></p>													
<b>STANDARDIZED MILITARY DRAWING</b>				CHECKED BY Charles E. Besore																	
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE				APPROVED BY Michael A. Frye				<p align="center">MICROCIRCUIT, LINEAR, HIGH-SPEED, ANALOG</p> <p align="center">TO DIGITAL CONVERTER, MONOLITHIC SILICON</p>													
				DRAWING APPROVAL DATE 18 AUGUST 1987																	
AMSC N/A				REVISION LEVEL A				SIZE A	CAGE CODE <b>67268</b>	<b>5962-87591</b>											
								SHEET 1 OF 17													

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type(s). The device type shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	AD7572	12.5-microsecond, 11-bit linearity, 12-bit resolution CMOS A/D converter with 45 ppm/°C reference.
02	AD7572	12.5-microsecond, 11-bit linearity, 12-bit resolution CMOS A/D converter with 25 ppm/°C reference.
03	AD7572	12.5-microsecond, 12-bit linearity, 12-bit resolution CMOS A/D converter with 25 ppm/°C reference.
04	AD7572	5-microsecond, 11-bit linearity, 12-bit resolution CMOS A/D converter with 45 ppm/°C reference.
05	AD7572	5-microsecond, 11-bit linearity, 12-bit resolution CMOS A/D converter with 25 ppm/°C reference.
06	AD7572	5-microsecond, 12-bit linearity, 12-bit resolution CMOS A/D converter with 25 ppm/°C reference.

1.2.2 Case outline(s). The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

<u>Outline letter</u>	<u>Case outline</u>
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-terminal, .460" x .460" x .100"), leadless ceramic square chip carrier package

1.3 Absolute maximum ratings (T<sub>A</sub> = +25°C, unless otherwise noted).

V <sub>DD</sub> to DGND .....	-0.3 V dc to +7 V dc
V <sub>SS</sub> to DGND .....	+0.3 V dc to -17 V dc
AGND to DGND .....	-0.3 V dc, V <sub>DD</sub> +0.3 V dc
A <sub>IN</sub> to DNG .....	-15 V dc to +15 V dc
Digital input voltage to DGND .....	-0.3 V dc, V <sub>DD</sub> +0.3 V dc
Digital output voltage to DGND .....	-0.3 V dc, V <sub>DD</sub> +0.3 V dc
Storage temperature range .....	-65°C to +150°C
Power dissipation ≤ +75°C .....	1000 mW 1/
Thermal resistance (θ <sub>JC</sub> ):	
Case L .....	See MIL-M-38510, appendix C
Case 3 .....	See MIL-M-38510, appendix C
Junction temperature (T <sub>J</sub> ) .....	+175°C

1/ Derate power dissipation above +75°C by 10 mW/°C.

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1.4 Recommended operating conditions.

Operating voltage range:	
Positive supply (V <sub>DD</sub> ) .....	+4.5 V dc to +5.25 V dc
Negative supply (V <sub>SS</sub> ) .....	-14.5 V dc to -15.75 V dc
Clock frequency (f <sub>CLK</sub> ) .....	1.0 MHz for device types 01, 02, and 03 2.5 MHz for device types 04, 05, and 06
Analog input voltage range (A <sub>IN</sub> ) (specifications apply to slow memory mode) .....	
Ambient operating temperature range (T <sub>A</sub> ).....	0 to +5.0 V dc -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD- 883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Load circuits. The load circuits shall be as specified on figures 2 and 3.

3.2.3 Timing diagrams. Timing diagrams and tables shall be as specified on figures 4, 5, 6, and 7.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Integral linearity error	LE	V <sub>DD</sub> = 5 V, V <sub>SS</sub> = -15 V	01, 02	1		±1	LSB
			04, 05			±1	
			03, 06	2, 3		±3/4	
			03, 06	12		±1/2	
Differential linearity error	DLE	V <sub>DD</sub> = 5 V, V <sub>SS</sub> = -15 V	All	1, 2, 3		±1	
Offset error	V <sub>OS</sub>	V <sub>DD</sub> = 5 V V <sub>SS</sub> = -15 V	All	1		±4	LSB
			01, 04	2, 3		±6	
			02, 05			±5	
			03, 06			±4	
			02, 05 03, 06	12		±3	
Full scale error including internal voltage reference error, (Ideal last code transition = FS-3/2LSB's)	AE	V <sub>DD</sub> = 5 V	All	1		±15	LSB
		V <sub>SS</sub> = -15 V Full scale = 5 V	02, 03 05, 06	12		±10	
Full scale temperature coefficient, including internal voltage reference drift	dAE/dT	V <sub>DD</sub> = 5 V V <sub>SS</sub> = -15 V	01, 04	2, 3		45	ppm/°C
			02, 03 05, 06			25	
Analog input current	I <sub>IN</sub>	A <sub>IN</sub> = 5 V	All	1, 2, 3		3.5	mA
Internal reference voltage output	V <sub>REF</sub>	V <sub>DD</sub> = 5 V, V <sub>SS</sub> = -15 V	All	1	-5.3	+5.2	V
Internal reference output current sink capability		Constant external load during conversion	All	13, 14, 15		550	μA
Digital input low voltage	V <sub>INL</sub>	CS, RD, HBEN, CLK IN.	All	1, 2, 3		0.8	V
Digital input high voltage	V <sub>INH</sub>	V <sub>DD</sub> = 4.75 V				2.4	
Digital input capacitance	C <sub>IN</sub>	V <sub>SS</sub> = -15 V		13		10	pF
Digital input current	I <sub>IN</sub>	CS, RD, HBEN. V <sub>DD</sub> = 5.25 V, V <sub>SS</sub> = -15 V A <sub>IN</sub> = 0 TO V <sub>DD</sub>	All	1, 2, 3		±10	μA
		CLK IN. V <sub>DD</sub> = 5.25 V, V <sub>SS</sub> = -15 V, A <sub>IN</sub> = 0 to V <sub>DD</sub>	All			±20	

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Digital output low voltage	V <sub>OL</sub>	D11-DO/8, BUSY, CLK OUT V <sub>DD</sub> = 4.75 V, V <sub>SS</sub> = -15 V	All	1, 2, 3		<u>0.4</u>	V
Digital output high voltage	V <sub>OH</sub>	Isink = 1.6 mA Is <sub>source</sub> = 200 μA			4.0		
Floating state leakage current	V <sub>OL</sub>	D11-DO/8. V <sub>DD</sub> = 5.25 V, V <sub>SS</sub> = -15 V	All	1, 2, 3		±10	μA
Floating state output capacitance	C <sub>OUT</sub>		All	13, 14, 15		15	pF
Conversion time using synchronous clock	t <sub>CONV</sub>		04,05,06	13,14,15		5	μs
			01,02,03			12.5	
Conversion time using 1/ asynchronous clock			04,05,06	9, 10,11	4.8	5.2	
			01,02,03		12.0	13.0	
Power supply current from V <sub>DD</sub>	I <sub>DD</sub>	V <sub>DD</sub> = 5.25 V V <sub>SS</sub> = -15.75 V	All	1, 2, 3		7	mA
Power supply current from V <sub>SS</sub>	I <sub>SS</sub>	CS = RD = BUSY = HIGH A <sub>IN</sub> = 5 V				12	
CS to RD setup time	t <sub>1</sub>	See figures 4, 5, 6, and 7	All	9, 14, 15	0		ns
RD to BUSY propagation delay	t <sub>2</sub>	2/		9		190	
				14, 15		270	
Data access time after RD, C <sub>L</sub> = 60 pF (see figure 2)	t <sub>3</sub> 3/			9		110	
				14, 15		150	
Data access time after RD, C <sub>L</sub> = 100 pF (see figure 2)	t <sub>3</sub> 3/			9		125	
				14, 15		170	
RD pulse width	t <sub>4</sub>			9, 14, 15	t <sub>3</sub>		
CS to RD hold time	t <sub>5</sub>			9, 14, 15	0		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Data setup time after —— BUSY, C <sub>L</sub> = 60 pF (see figure 2)	t <sub>6</sub> 3/	See figures 4, 5, 6, and 7 2/	All	9		70	ns
				14, 15		100	
Bus relinquish time  (see figure 3)	t <sub>7</sub> 4/		All	9	35	90	
				14, 15	20	90	
HBEN to RD setup time	t <sub>8</sub>		All	9, 14, 15	0		
HBEN to RD hold time	t <sub>9</sub>			9, 14, 15	0		
Delay between successive read operations	t <sub>10</sub>			9, 14, 15	500		

- 1/ Conversion time using asynchronous clock is measured by setting the clock frequency at the appropriate value (see 1.4) and checking all remaining tested specifications.
- 2/ All input control signals are specified with t<sub>r</sub> = t<sub>f</sub> = 5 ns (10 percent to 90 percent of +5 V) and timed from a voltage level of 1.6 V. Time t<sub>6</sub> and t<sub>10</sub> are measured only for the initial test and after process or design changes which may affect switching parameters.
- 3/ Time t<sub>3</sub> and t<sub>6</sub> are measured with the load circuits of figure 2 and defined as the time required for an output to cross 0.8 V or 2.4 V.
- 4/ Time t<sub>7</sub> is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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CASE L

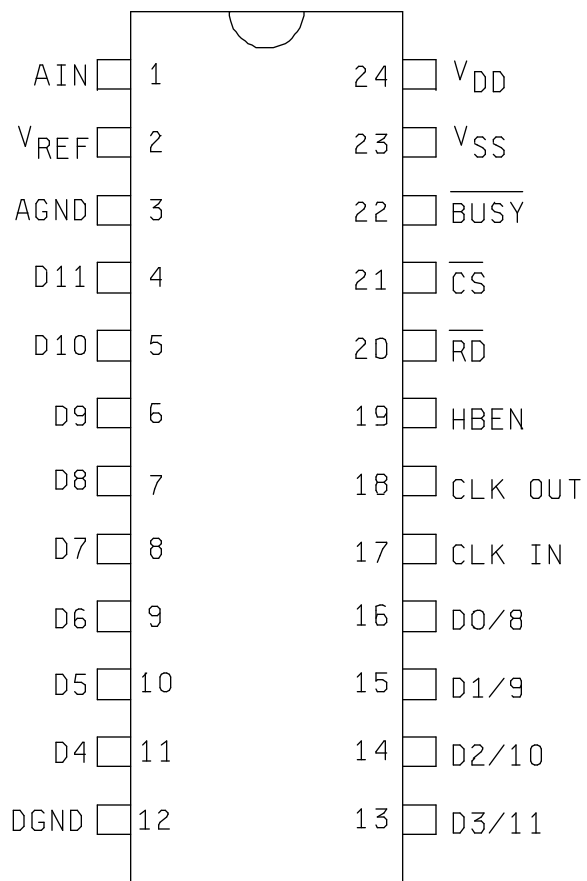


FIGURE 1. Terminal connections.

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CASE 3

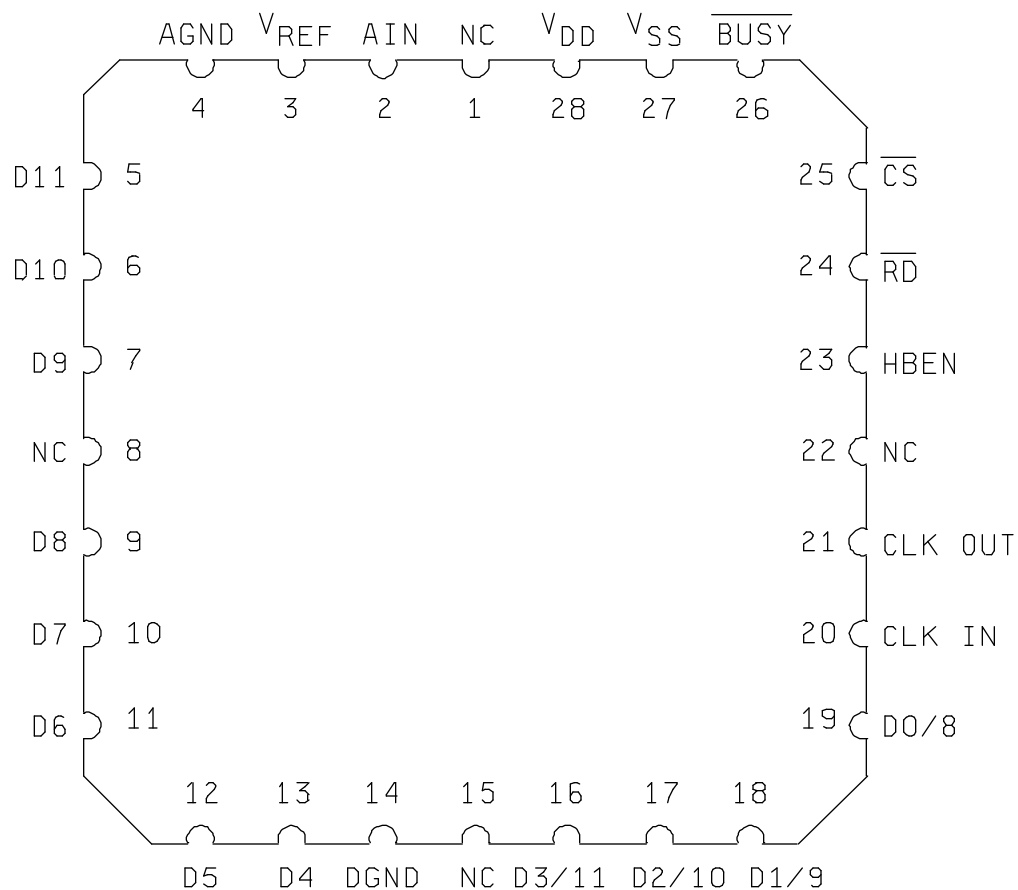


FIGURE 1. Terminal connections - Continued.

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		REVISION LEVEL A	SHEET <b>8</b>

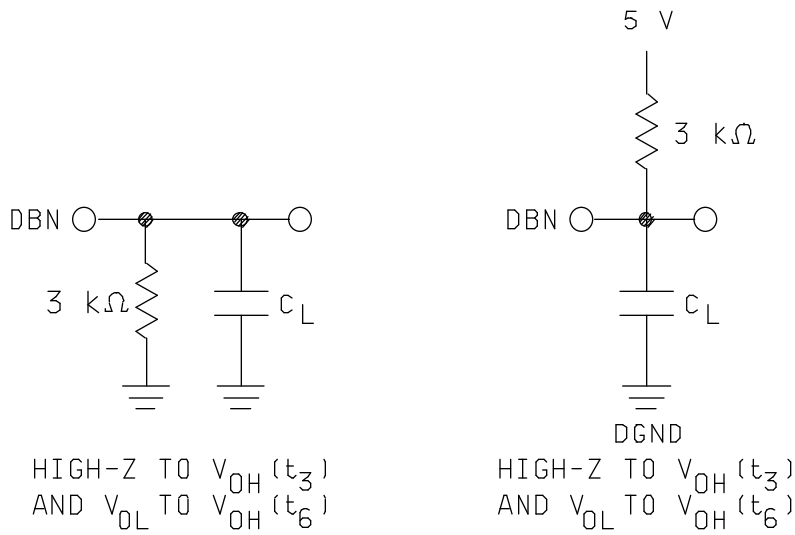


FIGURE 2. Load circuit for access time.

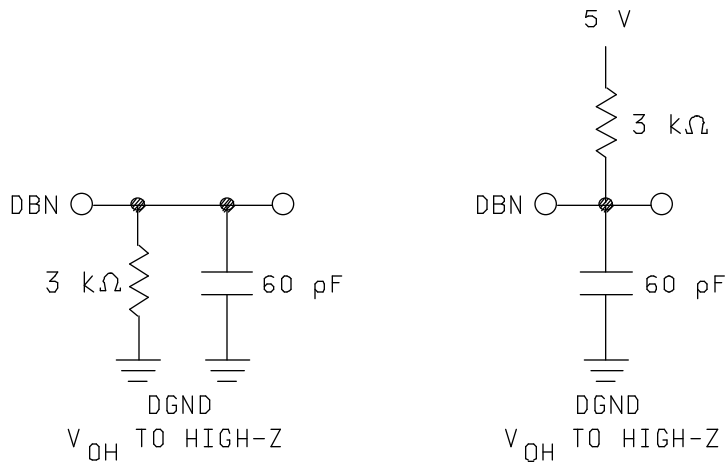


FIGURE 3. Load circuit for bus relinquish time.

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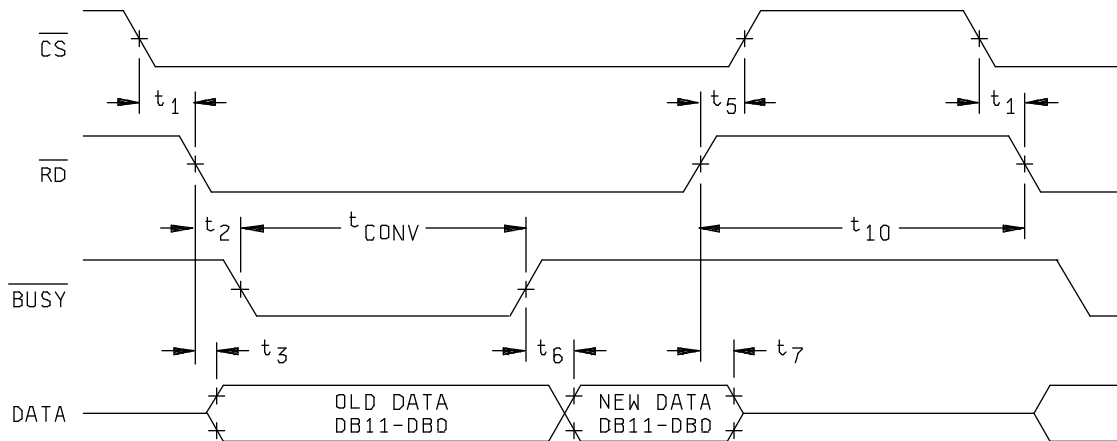


FIGURE 4. Slow memory mode, parallel read timing diagram.

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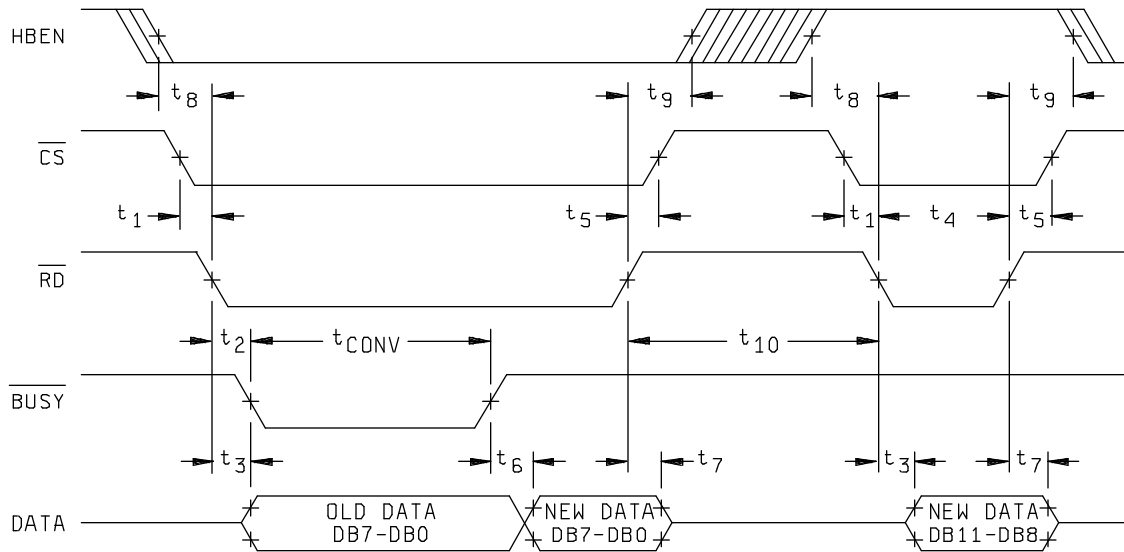


FIGURE 5. Slow memory mode, two byte read timing diagrams.

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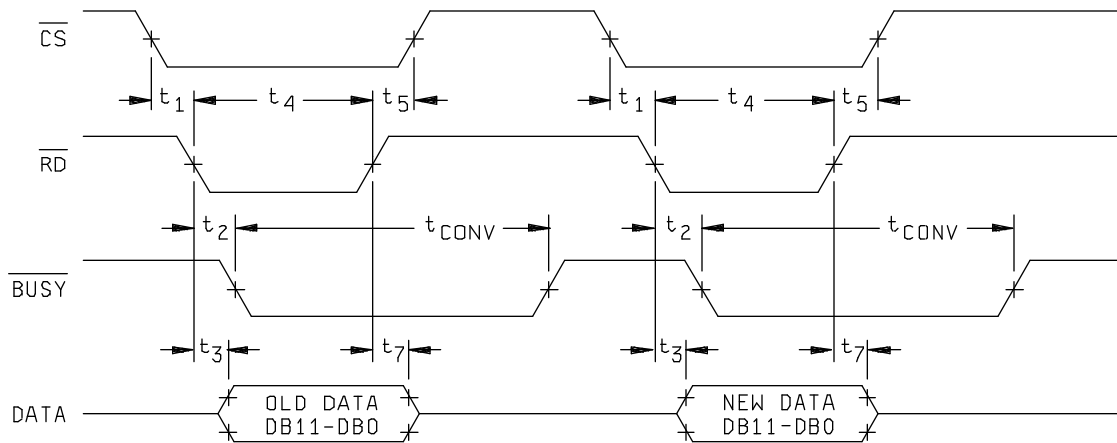


FIGURE 6. Rom mode, parallel read data bus timing diagrams.

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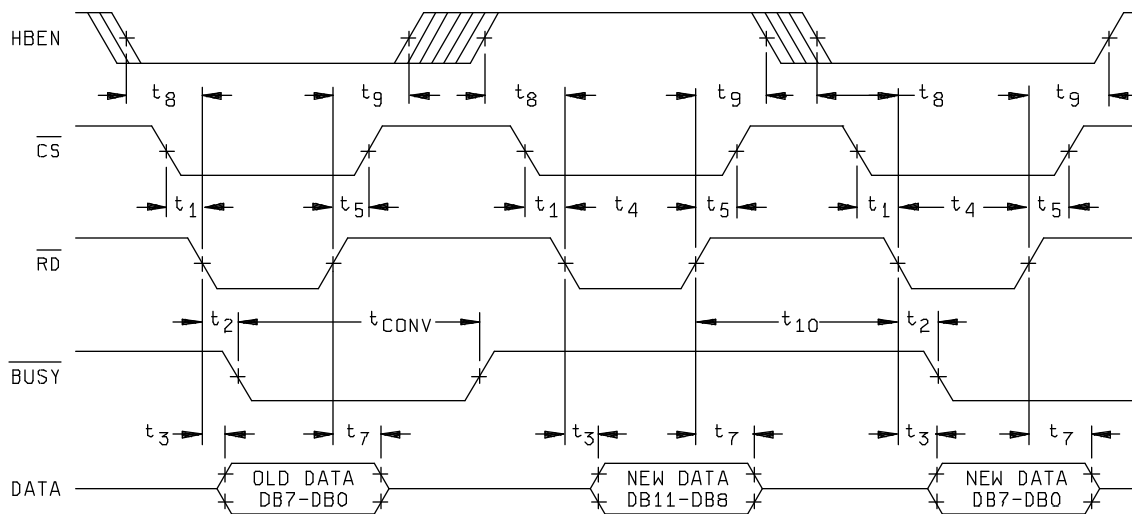


FIGURE 7. Rom mode, two byte read timing diagrams.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
  - (1) Test condition A or B using the circuit submitted with the certificate of compliance (see 3.6 herein).
  - (2)  $T_A = +125^\circ\text{C}$ , minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.
- c. Special subgroup 12 (as referenced in table I) added for grading and selection tests at  $+25^\circ\text{C}$  not included in PDA.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883, shall be omitted.
- c. Special subgroup 12 (as referenced in table I) added for grading and selection tests at  $+25^\circ\text{C}$ .

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition A or B using the circuit submitted with the certificate of compliance (see 3.6 herein).
  - (2)  $T_A = +125^\circ\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD- 883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 9, 10, 11, 12
Group A test requirements (method 5005)	1, 2, 3, 9, 10, 11, 12, 13**, 14**, 15**
Groups C and D end-point electrical parameters (method 5005)	1, 12

\* PDA applies to subgroup 1.

\*\* Special subgroups 13, 14, and 15 shall be measured only for initial test and after process or design changes and shall be guaranteed to the limits specified in table I. Subgroup 13 is +25°C, 14 is +125°C, and 15 is -55°C.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS , Dayton, Ohio 5444, or telephone (513) 296-5375.

<b>STANDARDIZED MILITARY DRAWING</b>	SIZE <b>A</b>		<b>5962-87591</b>
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6.6 Approved sources of supply. An approved source is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1/</u>
5962-8759101LX	24355	AD7572SQ12/883B
5962-87591013X	24355	AD7572SE12/883B
5962-8759102LX	24355	AD7572TQ12/883B
5962-87591023X	24355	AD7572TE12/883B
5962-8759103LX	24355	AD7572UQ12/883B
5962-87591033X	24355	AD7572UE12/883B
5962-8759104LX	24355	AD7572SQ05/883B
5962-87591043X	24355	AD7572SE05/883B
5962-8759105LX	24355	AD7572TQ05/883B
5962-87591053X	24355	AD7572TE05/883B
5962-8759106LX	24355	AD7572UQ05/883B
5962-87591063X	24355	AD7572UE05/883B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

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Vendor CAGE  
number

24355

Vendor name  
and address

Analog Devices  
Route 1 Industrial Park  
P.O. Box 9106  
Norwood, MA 02062  
Point of contact:: 804 Woburn Street  
Wilmington, MA 01887

<b>STANDARDIZED MILITARY DRAWING</b>	SIZE <b>A</b>		<b>5962-87591</b>
		REVISION LEVEL A	SHEET <b>17</b>