NOTIC THIS REVISION DESCRIBED BELC	CE OF REVISION (NOR) W HAS BEEN AUTHORIZED FOR TH	HE DOCUMENT LISTED.	1. DATE (YYMMDD) 97-06-23	Form Approved OMB No. 0704-0188
Public reporting burden for this collection is estima sources, gathering and maintaining the data need estimate or any other aspect of this collection of in	ated to average 2 hours per response, includ ed, and completing and reviewing the collect formation, including suggestions for reducing	ing the time for reviewing instructions ion of information. Send comments r g this burden, to Department of Defen	, searching existing data egarding this burden ise, Washingtion	2. PROCURING ACTIVITY NO.
Office of Management and Budget, Paperwork Re PLEASE DO NOT RETURN YOUR COMPLETE CONTRACTING OFFICER FOR THE CONTRA	o Operations and Reports, 1215 Jefferson D duction Project (0704-0188), Washington, D ED FORM TO EITHER OF THESE ADDRE CCT/ PROCURING ACTIVITY NUMBER LIS	avis Highway, Suite 1204, Arlington, C 20503. ESSED. RETURN COMPLETED F STED IN ITEM 2 OF THIS FORM.	VA 22202-4302, and to the ORM TO THE GOVERNME	N ³ DODAAC
4. ORIGINATOR	b. ADDRESS (Street, City, State Defense Supply Center Columbu	e, Zip Code) s	5. CAGE CODE 67268	6. NOR NO. 5962-R368-97
a. TYPED NAME <i>(First, Middle Initial, Last)</i>	Columbus, OH 43216-5000		7. CAGE CODE 67268	8. DOCUMENT NO. 5962-85127
9. TITLE OF DOCUMENT MCROCIRCUIT, LINEAR, MCROPROC	ESSOR COMPATIBLE, 12-BIT	10. REVISION LETTER	R	11. ECP NO.
ANALOG-TO-DIGITAL CONVERTERS, M	DNOLITHIC SILICON	a. CURRENT C	b. NEW D	N/A
12. CONFIGURATION ITEM (OR SYSTEM All) TO WHICH ECP APPLIES			
13. DESCRIPTION OF REVISION				
Sheet 1: Revisions lit column; add D. Revisions description column; add Revisions date column; add "97-0 Revision level block; change from ' Rev status of sheets; for sheets 1, Sheet 5: 3.10; delete this paragraph in its er Revision level block; change from ' Sheet 19: TABLE IIA; delete entire table and Revision level block; change from Sheet 20: 4.4.1 <u>Group Ainspection</u> ; for MIL-STD-883 shall be omitted". Revision level block; change from	"Changes in accordance with NOR 5962. 5-23". C" to "D". 5, 19, and 20 change from "C" to "D". tirrety. C" to "D". 4 substitute with table on sheet 2, block 13 "C" to "D". 4.4.1b, delete "and 8" in two places. Add Add 4.4.1d "Optional subgroup 12, for dev "C" to "D".	-R368-97". continuation sheet. 4.4.1c "Subgroups 5, 6, and 8 in ta <i>i</i> ce type 01, is used for grading the	ble I, method 5005 of part selection at 25	° C.
14. THIS SECTION FOR GOVERNMENT U	JSE ONLY			
a. (X one) X (1) Existing docu	ment supplemented by the NOR may be u	sed in manufacture.		
(2) Revised docu	ment must be received before manufacture	er may incorporate this change.		
(3) Custodian of	master document shall make above revisio	n and furnish revised document.		
b. ACTIVITY AUTHORIZED TO APPROVE	CHANGE FOR GOVERNMENT	c. TYPED NAME (First	t, Middle Initial, Last)	
DSCC-VAS		Raymond Monnin		
d. TITLE Chief, Custom Mcroelectronics	e. SIGNATURE Ravmond Mo	nnin		f. DATE SIGNED (YYMMDD) 97-06-23
15a. ACTIVITY ACCOMPLISHING REVISIO	N b. REVISION C	COMPLETED (Signature)		c. DATE SIGNED
DSCC-VAS	Dan Wonnell	,		(YYMMDD) 97-06-23

DD Form 1695, APR 92

Previous editions are obsolete.

Sheet 19: Add the following:

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subg (in accorda MIL-PRF-38	roups ance with 535, table III)
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 4, 12 <u>1</u> /	1, 2, 3, 4, 12 <u>1</u> /	1, 2, 3, 4, 12 <u>1</u> / <u>2</u> /
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 9, 10, 11, 12	1, 2, 3, 4, 7, 9, 10, 11, 12	1, 2, 3, 4, 7, 9, 10, 11, 12
Group C end-point electrical parameters (see 4.4)_	1, 4	1, 4	1, 4 <u>2</u> /
Group D end-point electrical parameters (see 4.4)	1, 4	1, 4	1, 4

TABLE IIA. Electrical test requirements .

1/ PDA applies to subgroup1.

2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous interim electrical parameters.

								I	REVIS	IONS			_				-			
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A	Add throu figur 01X table	two pa ughout. e 2 ha X and e.	ickage For s beer 02XX	es, C-5 case X n replac for nev	and C (, the d ced wit w desig	C-4. M limensi th D-10 gn. ปร	ake ch ons ha) confi se M38	anges ve bee guratio 3510 d	to tabl en char n. Ina evice.	le I, an nged a ictivate Add a	d nd device truth	es		90-0	01-24			M. A	A. Frye	
В	Add OH9	device 9K9, ai	types nd 332	05, 00 256. E	6, 07, Editoria	and 08 al chan	. Add ges thr	vendo ougho	ors CA	GES 1	ES66	3		93-0	03-15			M. A	A. Frye	
С	Add	class \	√ devi	ces. A	vdd Z p	backag	e. Edi	torial c	hange	s throu	ighout.			97-0	04-15			R. N	1onnin	
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DESC FORM 193

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DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 <u>Scope</u>. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.





1.2.1 <u>RHA designator</u>. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	574AU	Monolithic, high performance, 12-bit A/D converter with
		microprocessor interface
02	574AT	Monolithic, medium performance, 12-bit A/D converter with microprocessor interface
03	574AU	Multi-chip, high performance, 12-bit A/D converter with microprocessor interface
04	574AT	Multi-chip, medium performance, 12-bit A/D converter with microprocessor interface
05	574ZA	Monolithic, high performance, low power, 12-bit A/D converter with microprocessor interface
06	574ZB	Monolithic, medium performance, low power, 12-bit A/D converter with microprocessor interface
07	574AU	Monolithic, high performance, low power, 12-bit A/D converter with microprocessor interface
08	574AT	Monolithic, medium performance, low power, 12-bit A/D converter with microprocessor interface

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1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device. Device class Device requirements documentation Vendor self-certification to the requirements for MIL-STD-883 compliant, M non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A Q or V Certification and qualification to MIL-PRF-38535 1.2.4 <u>Case outline(s)</u>. The case outline(s) are as designated in MIL-STD-1835 and as follows: Outline letter Descriptive designator Terminals Package style Х GDIP1-T28 or CDIP2-T28 28 dual-in-line Y CQCC1-N44 44 square leadless chip carrier Ζ GDFP2-F28 28 flat pack 3 28 square leadless chip carrier CQCC1-N28 1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M. 1.3 Absolute maximum ratings . 1/ $V_{\mbox{CC}}$ to digital common $\hfill \hfill \$ VEE to digital common0 to -16.5 V dc VLOG to digital common0 to +7 V dc Analog common to digital common: 10 ms short to V_{CC} Power dissipation at 75 °C: Lead temperature (soldering, 10 seconds)+300°C Thermal resistance, junction-to-ambient (Θ_{JA}): 1.4 <u>Recommended operating conditions</u>. Power supply Operating voltage range: 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. For cases X and 3, derate linearly above T $_{A}$ = +75° C at 20.8 mW/° C. For case Y, derate linearly above T $_{A}$ = +75° C at 22.7 mW/° C. For case Z, derate linearly above T $_{A}$ = +115° C at 17 mW/° C. 2/ SIZE **STANDARD** 5962-85127 Α **MICROCIRCUIT DRAWING** DEFENSE SUPPLY CENTER COLUMBUS **REVISION LEVEL** SHEET

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2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883	-	Test Methods and Procedures for Microelectronics.
MIL-STD-973	-	Configuration Management.
MIL-STD-1835	-	Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 -	List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 -	Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 <u>Item requirements</u>. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 <u>Case outline(s)</u>. The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections . The terminal connections shall be as specified on figure 1.

3.2.3 <u>Truth table(s)</u>. The truth table(s) shall be as specified on figure 2.

3.2.4 <u>Block or logic diagram(s)</u>. The block or logic diagram(s) shall be as specified on figure 3.

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3.3 <u>Electrical performance characteristics and postirradiation parameter limits</u>. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 <u>Marking</u>. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 <u>Certification/compliance mark</u>. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 <u>Certificate of compliance</u>. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 <u>Certificate of conformance</u>. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 <u>Notification of change for device class M</u>. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 <u>Verification and review for device class M</u>. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 <u>Microcircuit group assignment for device class M</u>. Device class M devices covered by this drawing shall be in microcircuit group number 81 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 <u>Sampling and inspection</u>. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 <u>Screening</u>. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M _.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
 - (2) $T_{\Delta} = +125^{\circ} C$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Optional subgroup 12, for device 01, is used for grading the part selection at 25 °C.

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		TABLE I. Electrical perfo	ormance characte	eristics				
Test	Symbol	Conditions $-55^{\circ}C \le T_{A} \le +125^{\circ}C$ VCC = +15 V. VI OC = +15	Grou subgr	ip A roups	Device types	Limit	s	Unit
		VEE = -15 V unless otherwise specified	1			Min	Max	
Power supply current from V _{LOG}	ILOG		1, 2,	3	01, 02, 03, 04		40	mA
					05, 06 07, 08		1	_
Power supply current	ICC		1, 2,	3	01,02		5	
					03, 04		15	
					05, 06 07, 08		9	_
Power supply current from VEE	IEE		1, 2,	3	01, 02, 03, 04	-30		
					05, 06 07, 08	0		_
Resolution			1, 2,	3	All	12		Bits
Integral linearity	ILE		1		All	-0.5	0.5	LSB
error			2, 3		All	-1.0	1.0	_
Differential linearity error	DLE		1		All	12		Bits
(minimum resolution for which no missing codes guaranteed)			2, 3			12		
Unipolar offset voltage error	VIO	T _A = +25° C	1		All	-2.0	2.0	LSB
			12		01	-1.0	1.0	
Unipolar offset drift	$\frac{\Delta V_{\text{IO}}}{\Delta T}$	Using internal reference	2, 3		All	-1.0	1.0	
Bipolar zero offset	BZ	T _A = +25° C	1		All	-4.0	4.0	
entit			12		01	-2.0	2.0	_
See footnotes at end of tak	ble.	1			1	1	ŀ	+
MICROO	STANDARD	AWING	SIZE A					5962-85127
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	TA	BLE I. Electrical performanc	e characteristic	s Continued			
Test	Symbol	Conditions -55° C ≤ T _A ≤ +125° C Vcc = +15 V. V cc = +5	Grou subgi	p A Device roups types	Limit	s	Unit
		$V_{EE} = -15 V$ unless otherwise specified	- ,		Min	Max	
Bipolar zero offset drift	Δ B _Z	Using internal reference	2, 3	8 01, 03 05, 07	, -1.0	1.0	LSB
				02, 04 06, 08	, -2.0	2.0	
Gain error	ΔΑΕ	With 50Ω resistor from RE OUT to REF IN	F 1	01, 02		0.25	% of F.S.
		$T_{A} = +25^{\circ}C$		03, 04 05, 06 07, 08		0.30	
			12	01		0.125	
Gain error drift ΔA _E Using in ΔA _E		Using internal reference	2, 3	3 01, 03 05, 07	, -12.5	12.5	ppm/°C
			02, 04 06, 08	, -25.0	25.0	-	
Power supply +Ps sensitivity (Maximum change in full scale +Ps calibration)	+PSS1	+13.5 V≤ V _{CC} ≤+16.5 V T _A = +25° C	/ 1	All	-1.0	1.0	LSB
	+PSS2	+11.4 V≤ V _{CC} ≤+12.6 V T _A = +25° C	V				
	+PSS3	$T_{A} = +25^{\circ}C$ $3 +4.5 V \le V_{LOG} \le +5.5 V$ $T_{A} = +25^{\circ}C$	1	All	-0.5	0.5	
	-PSS1	-16.5 V≤ V _{EE} ≤-13.5 V T _A = +25°C	1	All	-1.0	1.0	_
	-PSS2	-12.6 V≤ V _{EE} ≤ -11.4 V T _A = +25° C					
Input impedance	Z _{IN}	10 V span, T _A = +25° C	4	All	3	7	kΩ
		20 V span, T _A = +25° C	4	01, 02 03, 04	, 6	14	
				05, 06 07, 08	15	25	
See footnotes at end of ta	able.						
			0.75				
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Test	Symbol	$\begin{array}{c c} Symbol & Conditions \\ -55^\circC \leq T_A \leq +125^\circC \\ V_{CC} = +15V,V_{I-OG} = +5V, \end{array}$		Device type	Limit	Unit	
		VEE = -15 V unless otherwise specified			Min	Max	
Internal reference voltage	VREF	$T_{A} = +25^{\circ}C 1/$	1	01, 02	9.98	10.02	V
				03, 04 <u>07, 08</u>	9.90	10.10	
				05, 06	9.97	10.03	
			12	01	9.99	10.01	
Output current <u>2</u> /	IO	Available for external loads $T_A = +25^{\circ}C$	1	01, 02, 03, 04		1.5	mA
				05, 06 07, 08		2.0	
Input voltage (CE, CS, 12/8, R/C, A _O) <u>3</u> /	VIH	Logic "1" T _A = +25° C	1	01, 02, 05, 06 <u>07, 08</u>	2.0	5.5	V
				03, 04	2.4	5.5	
	VIL	Logic "0" T _A = +25° C	1	All	-0.5	0.8	
Input current	IIN	T _A = +25° C	1	01, 02 03, 04 07, 08	-20	+20	μA
				05, 06	-1	1	
Output voltage (DB11-DB0, STS)	V _{OL}	Logic "0" T _A = +25° C I _{sink} = +1.6 mA	1	All		0.4	Volts
Output voltage (DB11-DB0)	VOH	Logic "1" T _A = +25° C I _{source} = +500 µA			2.4		

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	TA	BLE I. Electrical performance	e charact	eristics -	Continued.			
Test	Symbol	Conditions $-55^{\circ}C \leq T_{A} \leq +125^{\circ}C$ $V_{CC} = +15 V, V_{LOG} = +5 V$	V,	Group A subgroups	Device s type	Limit	s	Unit
		VEE = -15 V unless otherwise specified				Min	Max	
High impedance state output current	ΙZ	High-Z state T _A = +25° DB11 - DB0 only	С	1	01, 02 03, 04 <u>07, 08</u>	-20	+20	μA
					05, 06	-5	+5	
Functional tests		See section 4.4.1b T _A = $-$	+25° C	7	All			
Low R/C pulse width	tHRL	See figure 4		9, 10, 11	01, 02	250		ns
<u>4</u> /					03, 04	350		-
					05, 06 <u>07, 08</u>	50		-
STS delay from R/\overline{C}	tDS				01, 02 03, 04		600	
<u>4</u> /					05, 06 07, 08		200	-
Data valid after R/C low	^t HDR				01, 02, 05, 06 <u>07, 08</u>	25		
<u>4</u> /					03, 04	15		
STS delay after valid data	tHS				01, 02, 05, 06 <u>07, 08</u>	300	1000	_
<u>4</u> /					03, 04	300	1200	_
High R/C pulse width <u>5</u> /	^t HRH				01, 02, 03, 04	300		
					05, 06 07, 08	150		
See footnotes at end of tab	ole.							
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	TA	BLE I. Electrical performance	characteristics -	Continued.			
Test	Symbol	Conditions $-55^{\circ}C \le T_{A} \le +125^{\circ}C$ VCC = +15 V. VLCC = +5 V	Group A subgroups	s type	Limit	S	Unit
		$V_{EE} = -15 V$ unless otherwise specified	,		Min	Max	
Data access time <u>5</u> /	^t DDR	See figure 4	9, 10, 11	01, 02, 03, 04		250	ns
				05, 06 07, 08		150	
STS delay from CE <u>5</u> /	^t DSC	See figure 5	9, 10, 11	01, 02, 03, 04		350	ns
				05, 06 <u>07, 08</u>		200	_
CE pulse width <u>5</u> /	^t HEC			01, 02, 03, 04	300		
				05, 06 <u>07, 08</u>	50		
Conversion time <u>6</u> /	tC	8-bit cycle		01,02 <u>4</u> /	10	24	hs
				03, 04 05, 06 <u>07, 08</u>	10	17	_
		12-bit cycle		01,02 <u>4</u> /	15	35	_
				03, 04 05, 06 <u>07, 08</u>	15	25	
Access time (from CE)	tDD	See figure 6		01, 02		200	ns
<u>4</u> /				03, 04		250	-
				05, 06 07, 08		150	
See footnotes at end of tab	le.						
S MICROC	TANDARD	AWING	SIZE A			5	962-85127
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	TA	BLE I. Electrical performance chara	<u>cteristics</u> - C	Continued.			
Test	Symbol	Conditions -55° C $\leq T_A \leq +125°$ C	Group A subgroups	Device type	Limit	S	Unit
		$V_{CC} = +15 V$, $V_{LOG} = +5 V$, $V_{EE} = -15 V$ unless otherwise specified			Min	Max	
Data valid after CE low	tHD	See figure 6	9, 10, 11	01, 02, 05, 06 <u>07, 08</u>	25		ns
<u>4</u> /				03, 04	15		
Output float delay	tHL	See figure 6	9, 10, 11	01, 02		100	
<u>4</u> /				03, 04, 05, 06 07, 08		150	

1/ The reference voltage external load current shall be a constant dc and shall not exceed 1.5 mA.

2/ Reference should be buffered for operation on ±12 V supplies. External load should not change during conversion.

 $\underline{3}$ / For devices 01 and 02, 12/ $\overline{8}$ is not TTL compatible and must be hard wired to V LOG or digital common.

4/ Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits.

 $\underline{5}$ / Parameters t _{HRH}, t_{DDR}, t_{DSC}, and t_{HEC}, if not tested, shall be guaranteed to the specified limits.

 $\underline{6}$ / For devices 03 and 04, time is measured from 50 percent level of digital transitions, tested with a 50 pF and 3.0 k Ω load.

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Device types	All	02	01, 02, 05, 06, 07	7, 08 01, 02, 03,	04
Case outlines	Х	Z	3	Y	
Terminal number	Terminal s	ymbol	Terminal symbo	I Terminal sy	mbol
1	YLOG		Log	Чод	
$\begin{array}{c} 2\\ 3\\ 4\\ 5\\ 6\\ 7\\ 8\\ 9\\ 10\\ 11\\ 12\\ 13\\ 14\\ 15\\ 16\\ 17\\ 18\\ 19\\ 20\\ 21\\ 22\\ 23\\ 24\\ 25\\ 26\\ 27\\ 28\\ 29\\ 30\\ 31\\ 32\\ 33\\ 34\\ 35\\ 36\\ 37\\ 38\\ 39\\ 40\\ 41\\ 42\\ 43\\ 44 \end{array}$	12/8 CS AO R/C CE V _{CC} REF OL AGND REF IN VEE BIP OFF 10 V _N 20 V _N DGND DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 DB8 DB7 DB8 DB9 DB10 DB11 (N STS - - - - - - - - - - - - -	IT ISB) FIGURE 1. <u>Te</u>	12/8 CS AO R/C CE V _C C REF OUT AGND REF IN VEE BIP OFF 10 V _N 20 V _N DGND DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 DB8 DB9 DB10 DB11 (MSB) STS - - - - - - - - - - - - -	12/8 CS AO NC NC NC R/C CE VCC REF OU AGND REF IN VEE NC BIP OFF 10 VN 20 VN NC NC NC DGND NC NC DB0 DB1 DB2 NC DB3 DB4 DB5 DB6 DB7 DB8 DB9 NC NC <td>T</td>	T
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CE	CS	R/C	12/8	Ao	Operation
0 X	X 1	X X	X X	X X	None None
1	0 0	0 0	X X	0 1	Initiate 12-bit conversion Initiate 8-bit conversion
1	0	1	1	x	Enable 12-bit parallel output
1	0	1	0 0	0	Enable 8 most significant bits Enable 4 LSBs + 4 trailing zeros

FIGURE 2. Truth table.

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TABLE IIA. Electrical test requirements .

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1, 2, 3, 4, 12 <u>1</u> / <u>2</u> /
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 9 10, 11, 12
Group C and D end-point electrical parameters (method 5005)	1, 4 <u>2</u> /

 <u>1</u>/ PDA applies to subgroup 1.
 <u>2</u>/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous interim electrical parameters.

TABLE IIB. 240 hour burn-in and group C end-point electrical parameters ____.

Test title	Endpoint limits		Delta limits	Units
	Min	Max		
Uni Vio	-1	2	±0.5	LSB
Bpze	-5.5	4.5	±1	LSB
Ae	-0.35	0.35	±.10	%FSR

4.2.2 Additional criteria for device classes Q and V .

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

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4.3 <u>Qualification inspection for device classes Q and V</u>. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 <u>Conformance inspection</u>. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection .

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 <u>Group C inspection</u>. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M_. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- b. $T_A = +125^{\circ}C$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 <u>Additional criteria for device classes Q and V</u>. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 <u>Group D inspection</u>. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 <u>Group E inspection</u>. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T $_{A}$ = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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6. NOTES

6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 <u>Record of users</u>. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 <u>Comments</u>. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 <u>Abbreviations, symbols, and definitions</u>. The abbreviations, symbols, and definitions used herein are listed below and defined in MIL-PRF-38535 and MIL-HDBK-1331.

12/8	Data mode select input
CS	Chip select input
A0	Byte address/short cycle input
R/C	Read/convert input
CE	Chip enable input
VCC	Positive power supply
REF OUT	Reference output
AGND	Analog ground
REF IN	Reference input
VEE	Negative power supply
BIP OFF	Bipolar offset input
VIN	Span input
DGND	Digital ground
D0-D11	Three-state data outputs
STS	Status output
NC	No connection

6.6 Sources of supply .

6.6.1 <u>Sources of supply for device classes Q and V</u>. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 <u>Approved sources of supply for device class M</u>. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 97-04-15

Approved sources of supply for SMD 5962-85127 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /	Reference military specification PIN
5962-8512701XA	24355	AD574AUD/883B MX574AUD/883B OR MX574AUQ/883B	M38510/14001BXA
5962-85127013A	24355	AD574AUE/883B	
5962-8512702XA	24355	AD574ATD/883B MX574ATD/883B OR MX574ATQ/883B	M38510/14002BXA
5962-8512702VXA	24355	AD547ATD/QMLV	
5962-8512702VZA	24355	AD547ATF/QMLV	
5962-85127023A	24355	AD574ATE/883B MX574ATE/883B	
5962-8512703XA	34371	HI1-574AUD/883	M38510/14001BXA
5962-8512703YA	34371	HI4-574AUE/883	
5962-8512704XA	34371	HI1-574ATD/883	M38510/14002BXA
5962-8512704YA	34371	HI4-574ATE/883	
5962-8512705XC	0H9K9	HADC574ZAMJ/883	M38510/14001BXA
5962-85127053A	0H9K9	HADC574ZAMC/883	
5962-8512706XC	0H9K9	HADC574ZBMJ/883	M38510/14002XA
5962-85127063A	0H9K9	HADC574ZBMC/883	
5962-8512707XC	33256	HS574AU/B	M38510/14001XA
5962-85127073C	33256	HS574AU/B-LCC	
5962-8512708XC	33256	HS574AT/B	M38510/14002XA
5962-85127083C	33256	HS574AT/B-LCC	

 $\frac{1}{2}$ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information. $\frac{2}{2}$ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing. 1 of 2

STANDARD MICROCIRCUIT DRAWING BULLETIN - continued

Vendor CAGE <u>number</u>	Vendor name and address
24355	Analog Devices Incorporated Route 1 Industrial Park PO Box 9106 Norwood, MA 02062-9106 Point of contact: 1500 Space Park Drive PO Box 58020 Santa Clara, CA 95050-8020
34371	Harris Corporation PO Box 883 Melbourne, FL 32902-0883
1ES66	Maxim Integrated Products 120 San Gabriel Drive Sunnyvale, CA 94086-5126
0H9K9	Signal Processing Technologies, Inc 4755 Forge Road Colorado Springs, CO 80907-3519
33256	Sipex Corporation 22 Linnell Circle Billerica, MA 01821-3985

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