ANALOG DEVICES

Single Supply, Low Power Triple Video Amplifier

AD813

FEATURES

Low Cost
Three Video Amplifiers in One Package
Optimized for Driving Cables in Video Systems
Excellent Video Specifications (R_L = 150 Ω)
- **Gain Flatness 0.1 dB to 50 MHz**
- **0.03% Differential Gain Error**
- **0.06° Differential Phase Error**

Low Power
- **Operates on Single +3 V to ±15 V Power Supplies**
- **5.5 mA/Amplifier Max Power Supply Current**

High Speed
- **125 MHz Unity Gain Bandwidth (–3 dB)**
- **500 V/µs Slew Rate**

High Speed Disable Function per Channel
- **Turn-Off Time 80 ns**

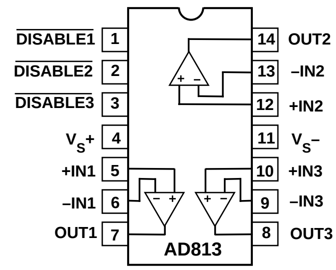
Easy to Use
- **50 mA Output Current**
- **Output Swing to 1 V of Rails**

APPLICATIONS

Video Line Driver
LCD Drivers
Computer Video Plug-In Boards
Ultrasound
RGB Amplifier
CCD Based Systems

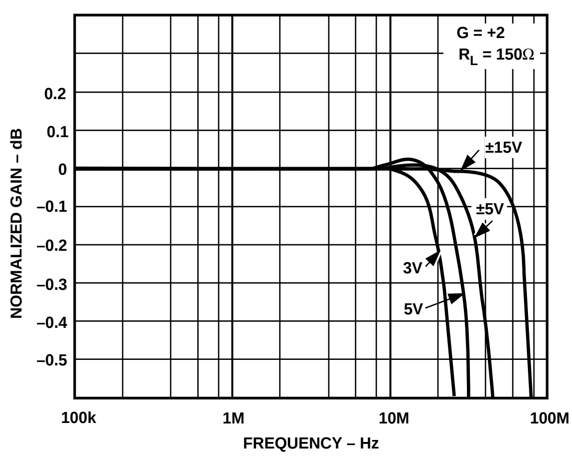
PIN CONFIGURATION

14-Pin DIP & SOIC Package



PRODUCT DESCRIPTION

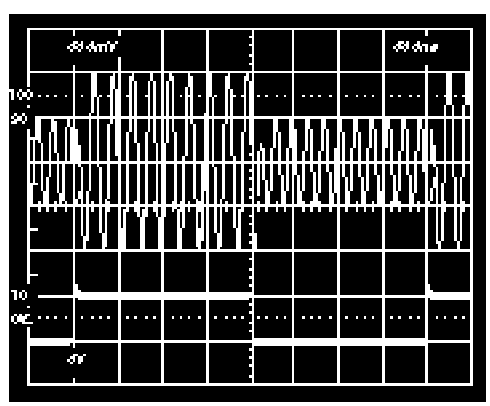
The AD813 is a low power, single supply triple video amplifier. Each of the three current feedback amplifiers has 50 mA of output current, and is optimized for driving one back terminated video load (150 Ω). The AD813 features gain flatness of 0.1 dB to 50 MHz while offering differential gain and phase error of 0.03% and 0.06°. This makes the AD813 ideal for broadcast and consumer video electronics.



Fine-Scale Gain Flatness vs. Frequency, G = +2, R_L = 150 Ω

The AD813 offers low power of 5.5 mA per amplifier max and runs on a single +3 V power supply. The outputs of each amplifier swing to within one volt of either supply rail to easily accommodate video signals. While operating on a single +5 V supply the AD813 still achieves 0.1 dB flatness to 20 MHz and 0.05% & 0.05° of differential gain and phase performance. All this is offered in a small 14-pin plastic DIP or SOIC package. These features make this triple amplifier ideal for portable and battery powered applications where size and power are critical.

The outstanding bandwidth of 125 MHz along with 500 V/µs of slew rate make the AD813 useful in many general purpose, high speed applications where a single +3 V or dual power supplies up to ±15 V are needed. Furthermore the AD813 contains a high speed disable function for each amplifier in order to power down the amplifier or high impedance the output. This can then be used in video multiplexing applications. The AD813 is available in the industrial temperature range of –40°C to +85°C in plastic DIP and SOIC packages as well as chips.



Channel Switching Characteristics for a 3:1 Mux

REV. A

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AD813–SPECIFICATIONS

Dual Supply (@ T_A = + 25°C, R_L = 150 Ω, unless otherwise noted)

Model	Conditions	V_S	AD813A Min	AD813A Typ	AD813A Max	Units
DYNAMIC PERFORMANCE						
–3 dB Bandwidth	G = +2, No Peaking	±5 V	45	65		MHz
		±15 V	75	100		MHz
Bandwidth for 0.1dB Flatness	G = +2	±5 V	15	25		MHz
		±15 V	25	50		MHz
Slew Rate[1]	G = +2, R_L= 1 kΩ	±5 V		150		V/µs
		±15 V	150	250		V/µs
	G = –1, R_L= 1 kΩ	±5 V		225		V/µs
		±15 V		450		V/µs
Settling Time to 0.1%	G = –1, R_L = 1 kΩ					
	V_O = 3 V Step	±5 V		50		ns
	V_O = 10 V Step	±15 V		40		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion	f_C = 1 MHz, R_L = 1 kΩ	±15 V		–90		dBc
Input Voltage Noise	f = 10 kHz	±5 V, ±15 V		3.5		nV√Hz
Input Current Noise	f = 10 kHz, +In	±5 V, ±15 V		1.5		pA√Hz
	–In	±5 V, ±15 V		18		pA√Hz
Differential Gain Error	NTSC, G = ±2, R_L = 150 Ω	±5 V		0.08		%
		±15 V		0.03	0.09	%
Differential Phase Error		±5 V		0.13		Degrees
		±15 V		0.06	0.12	Degrees
DC PERFORMANCE						
Input Offset Voltage		±5 V, ±15 V		2	5	mV
	T_{MIN}–T_{MAX}				12	mV
Offset Drift		±5 V, ±15 V		15		µV/°C
–Input Bias Current		±5 V, ±15 V		5	30	µA
	T_{MIN}–T_{MAX}				35	µA
+Input Bias Current		±5 V, ±15 V		0.5	1.5	µA
	T_{MIN}–T_{MAX}				2	µA
Open-Loop Voltage Gain	V_O = ±2.5 V, R_L = 150 Ω	±5 V	69	76		dB
	T_{MIN}–T_{MAX}		66			dB
	V_O = ±10 V, R_L = 1 kΩ	±15 V	76	82		dB
	T_{MIN}–T_{MAX}		75			dB
Open-Loop Transresistance	V_O = ±2.5 V, R_L = 150 Ω	±5 V	300	500		kΩ
	T_{MIN}–T_{MAX}		200			kΩ
	V_O = ±10 V, R_L = 1 kΩ	±15 V	500	900		kΩ
	T_{MIN}–T_{MAX}		370			kΩ
INPUT CHARACTERISTICS						
Input Resistance	+Input	±15 V		15		MΩ
	–Input	±15 V		65		Ω
Input Capacitance	+Input	±15 V		1.7		pF
Input Common Mode Voltage Range		±5 V		±4.0		V
		±15 V		±13.5		V
Common-Mode Rejection Ratio						
Input Offset Voltage	V_{CM} = ±2.5 V	±5 V	54	58		dB
–Input Current				2	3	µA/V
±Input Current				0.07	0.15	µA/V
Input Offset Voltage	V_{CM} = ±10 V	±15 V	57	62		dB
–Input Current				1.5	2.5	µA/V
+Input Current				0.05	0.1	µA/V

Model	Conditions	V_S	AD813A Min	Typ	Max	Units
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_L = 150 Ω, T_{MIN}–T_{MAX}	±5 V	3.5	3.8		±V
	R_L = 1 kΩ, T_{MIN}–T_{MAX}	±15 V	13.6	14.0		±V
Output Current		±5 V	25	40		mA
		±15 V	30	50		mA
Short Circuit Current	G = +2, R_F = 715 Ω V_{IN} = 2 V	±15 V		100		mA
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	G = +2, f = 5 MHz	±5 V, ±15 V		–65		dB
Gain Flatness Match	G = +2, f = 40 MHz	±15 V		0.1		dB
DC						
Input Offset Voltage	T_{MIN}–T_{MAX}	±5 V, ±15 V		0.5	2.5	mV
–Input Bias Current	T_{MIN}–T_{MAX}	±5 V, ±15 V		2	10	µA
POWER SUPPLY						
Operating Range			±1.2		±18	V
Quiescent Current	Per Amplifier	±5 V		3.5	4.0	mA
		±15 V		4.5	5.5	mA
	T_{MIN}–T_{MAX}	±15 V			6.7	mA
Quiescent Current, Powered Down	Per Amplifier	±5 V		0.5	0.6	mA
		±15 V		0.75	0.9	mA
Power Supply Rejection Ratio						
Input Offset Voltage	V_S = ±1.5 V to ±15 V		72	80		dB
–Input Current				0.3	0.7	µA/V
+Input Current				0.005	0.05	µA/V
DISABLE CHARACTERISTICS						
Off Isolation	f = 5 MHz	±5 V, ±15 V		–57		dB
Off Output Impedance	G = +1	±5 V, ±15 V		12.5		pF
Channel-to-Channel Isolation	2 or 3 Channels Mux, f = 5 MHz	±5 V, ±15 V		–65		dB
Turn-On Time		±5 V, ±15 V		100		ns
Turn-Off Time				80		ns

NOTES
[1]Slew rate measurement is based on 10% to 90% rise time in the specified closed-loop gain.
Specifications subject to change without notice.

AD813–SPECIFICATIONS

Single Supply (@ T_A = + 25°C, R_L = 150 Ω, unless otherwise noted)

Model	Conditions	V_S	AD813A Min	AD813A Typ	AD813A Max	Units
DYNAMIC PERFORMANCE						
–3 dB Bandwidth	G = +2, No Peaking	+5 V	35	50		MHz
		+3 V	25	40		MHz
Bandwidth for 0.1 dB Flatness	G = +2	+5 V	12	20		MHz
		+3 V	8	15		MHz
Slew Rate[1]	G = +2, R_L = 1 kΩ	+5 V		100		V/µs
		+3 V		50		V/µs
NOISE/HARMONIC PERFORMANCE						
Input Voltage Noise	f = 10 kHz	+5 V, +3 V		3.5		nV√Hz
Input Current Noise	f = 10 kHz, +In	+5 V, +3 V		1.5		pA√Hz
	–In	+5 V, +3 V		18		pA√Hz
Differential Gain Error[2]	NTSC, G = +2, R_L = 150 Ω	+5 V		0.05		%
	G = +1	+3 V		0.2		%
Differential Phase Error[2]	G = +2	+5 V		0.05		Degrees
	G = +1	+3 V		0.2		Degrees
DC PERFORMANCE						
Input Offset Voltage		+5 V, +3 V		1.5	3	mV
	T_{MIN}–T_{MAX}				10	mV
Offset Drift		+5 V, +3 V		7		µV/°C
–Input Bias Current		+5 V, +3 V		7	30	µA
	T_{MIN}–T_{MAX}				35	µA
+Input Bias Current		+5 V, +3 V		0.5	1.5	µA
	T_{MIN}–T_{MAX}				2	µA
Open-Loop Voltage Gain	V_O = +2.5 V p-p	+5 V	67	70		dB
	V_O = +0.7 V p-p	+3 V		69		dB
Open-Loop Transresistance	V_O = +3 V p-p	+5 V	200	300		kΩ
	V_O = +1 V p-p	+3 V		225		kΩ
INPUT CHARACTERISTICS						
Input Resistance	+Input	+5 V, +3 V		15		MΩ
	–Input	+5 V		90		Ω
Input Capacitance	+Input			2		pF
Input Common Mode		+5 V	1.0		4.0	V
Voltage Range		+3 V	1.0		2.0	V
Common-Mode Rejection Ratio						
Input Offset Voltage	V_{CM} = 1.25 V to 3.75 V	+5 V	54	58		dB
–Input Current				3	5	µA/V
+Input Current				0.1	0.2	µA/V
Input Offset Voltage	V_{CM} = 1 V to 2 V	+3 V		56		dB
–Input Current				3.5		µA/V
+Input Current				0.1		µA/V

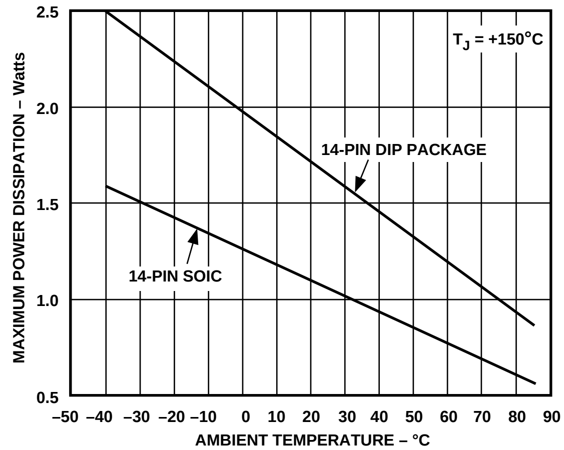
Model	Conditions	V_S	Min (AD813A)	Typ (AD813A)	Max (AD813A)	Units
OUTPUT CHARACTERISTICS						
Output Voltage Swing p-p	R_L = 150 Ω, T_{MIN}–T_{MAX}	+5 V	3.0	3.2		±V p-p
		+3 V	1.0	1.3		±V p-p
Output Current		+5 V	20	30		mA
		+3 V	15	25		mA
Short Circuit Current	G = +2, R_F = 715 Ω V_{IN} = 1 V	+5 V		40		mA
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	G = +2, f = 5 MHz	+5 V, +3 V		–65		dB
Gain Flatness Match	G = +2, f = 20 MHz	+5 V, +3 V		0.1		dB
DC						
Input Offset Voltage	T_{MIN}–T_{MAX}	+5 V, +3 V		0.5	2.5	mV
–Input Bias Current	T_{MIN}–T_{MAX}	+5 V, +3 V		2	10	µA
POWER SUPPLY						
Operating Range			2.4		36	V
Quiescent Current	Per Amplifier	+5 V		3.2	4.0	mA
		+3 V		3.0	3.5	mA
	T_{MIN}–T_{MAX}	+5 V			5.0	mA
Quiescent Current, Powered Down	Per Amplifier	+5 V		0.4	0.5	mA
		+3 V		0.4	0.5	mA
Power Supply Rejection Ratio						
Input Offset Voltage	V_S = +3.0 V to +30 V			76		dB
–Input Current				0.3		µA/V
+Input Current				0.005		µA/V
DISABLE CHARACTERISTICS						
Off Isolation	f = 5 MHz	+5 V, +3 V		–55		dB
Off Output Impedance	G = +1	+5 V, +3 V		13		pF
Channel-to-Channel Isolation	2 or 3 Channel Mux, f = 5 MHz	+5 V, +3 V		–65		dB

Maximum Power Dissipation

The maximum power that can be safely dissipated by the AD813 is limited by the associated rise in junction temperature. The maximum safe junction temperature for the plastic encapsulated parts is determined by the glass transition temperature of the plastic, about 150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD813 is internally short circuit protected, this may not be enough to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is important to observe the derating curves.

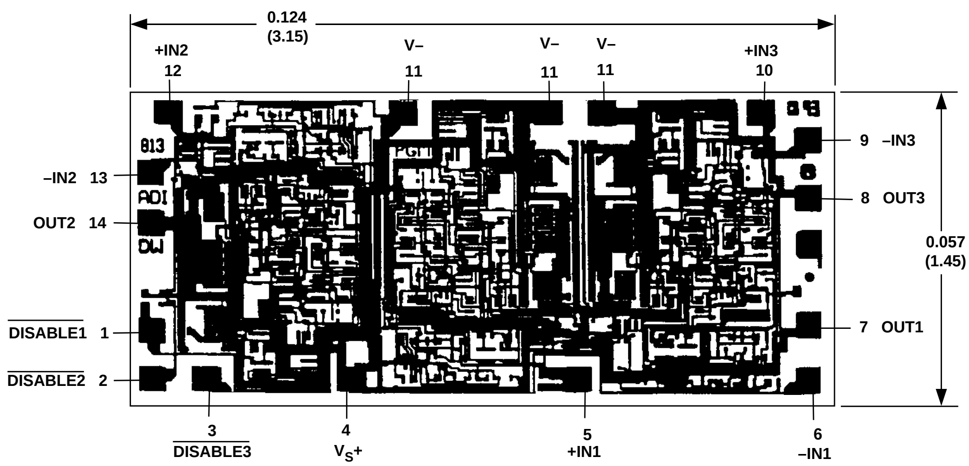
It must also be noted that in (noninverting) gain configurations (with low values of gain resistor), a high level of input overdrive can result in a large input error current, which may result in a significant power dissipation in the input stage. This power must be included when computing the junction temperature rise due to total internal power.



Maximum Power Dissipation vs. Ambient Temperature

METALIZATION PHOTO

Dimensions shown in inches and (mm).



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD813 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

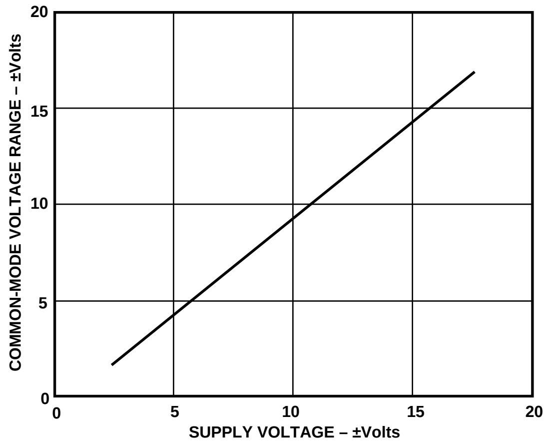


Figure 1. Input Common-Mode Voltage Range vs. Supply Voltage

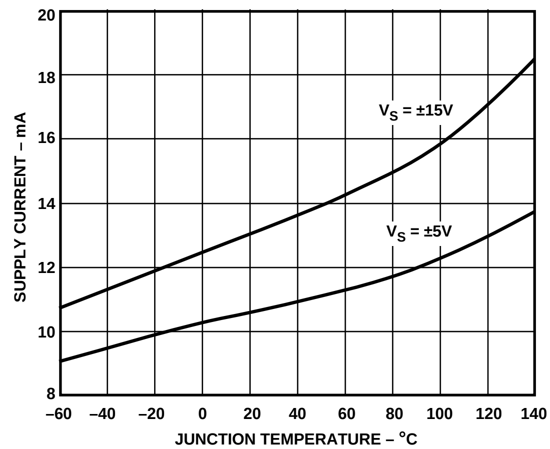


Figure 4. Supply Current vs. Junction Temperature

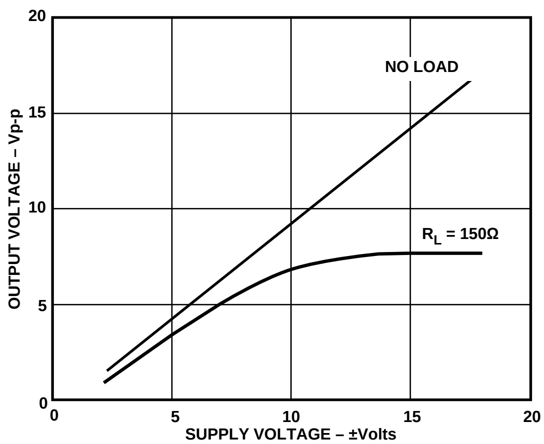


Figure 2. Output Voltage Swing vs. Supply

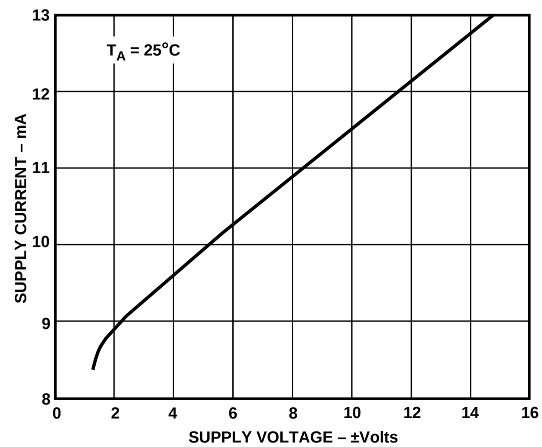


Figure 5. Supply Current vs. Supply Voltage at Low Voltages

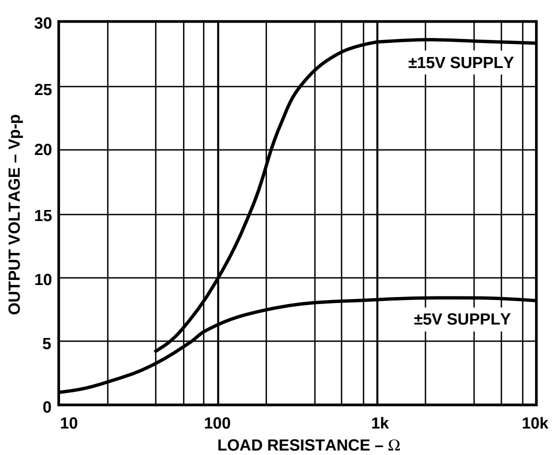


Figure 3. Output Voltage Swing vs. Load Resistance

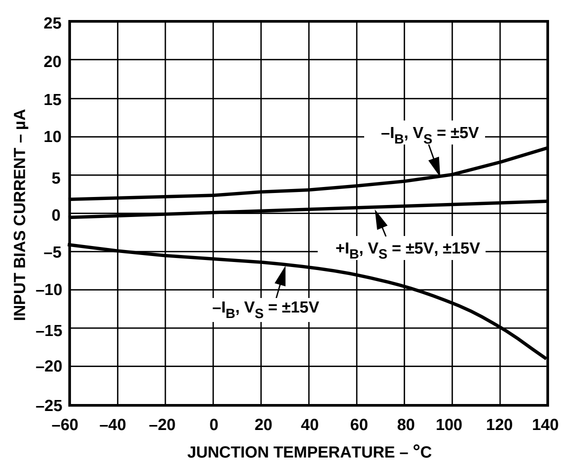


Figure 6. Input Bias Current vs. Junction Temperature

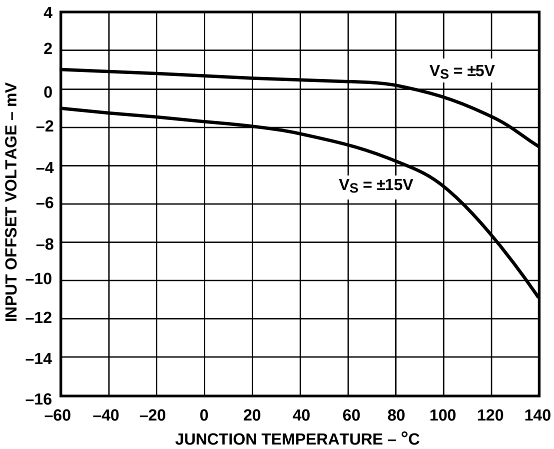


Figure 7. Input Offset Voltage vs. Junction Temperature

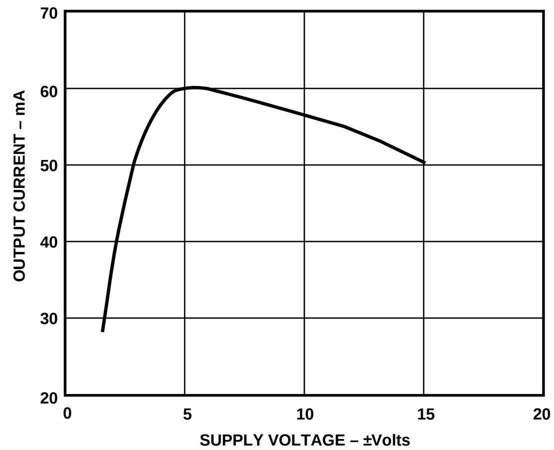


Figure 10. Linear Output Current vs. Supply Voltage

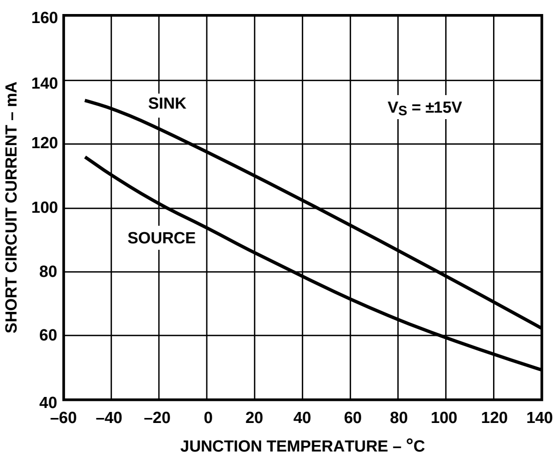


Figure 8. Short Circuit Current vs. Junction Temperature

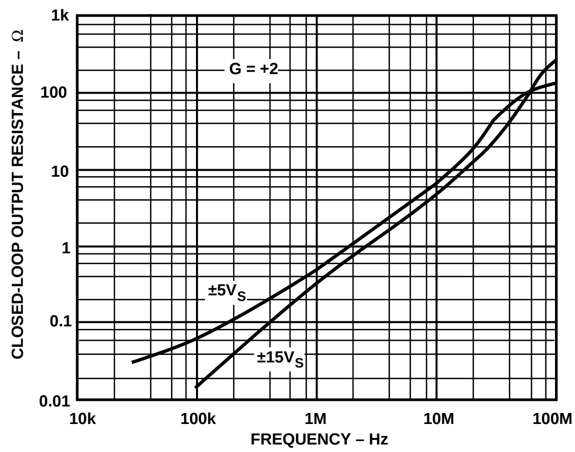


Figure 11. Closed-Loop Output Resistance vs. Frequency

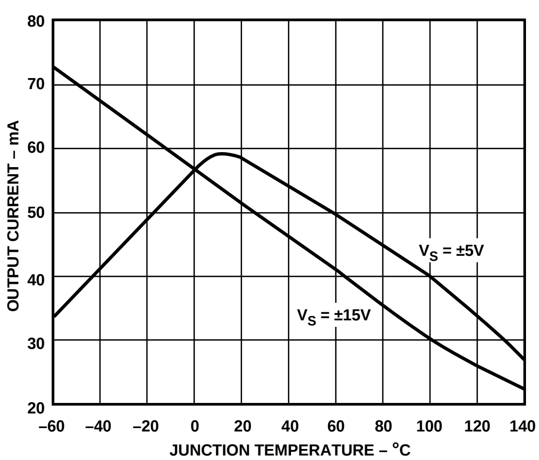


Figure 9. Linear Output Current vs. Junction Temperature

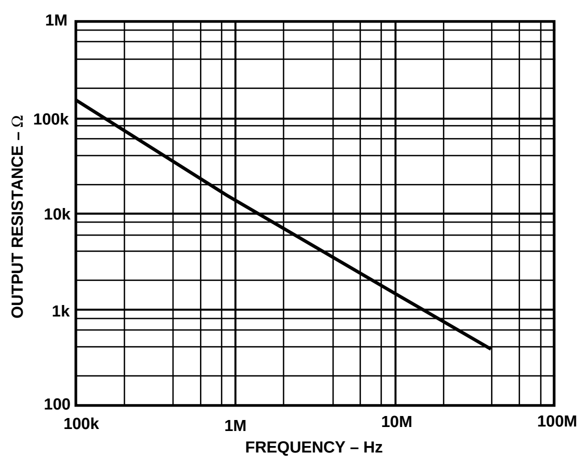


Figure 12. Output Resistance vs. Frequency, Disabled State

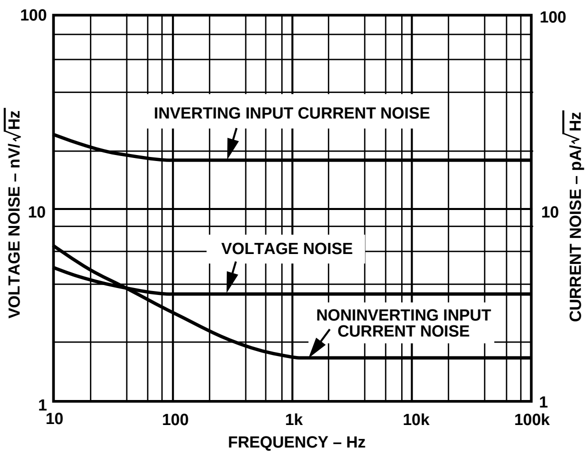


Figure 13. Input Current and Voltage Noise vs. Frequency

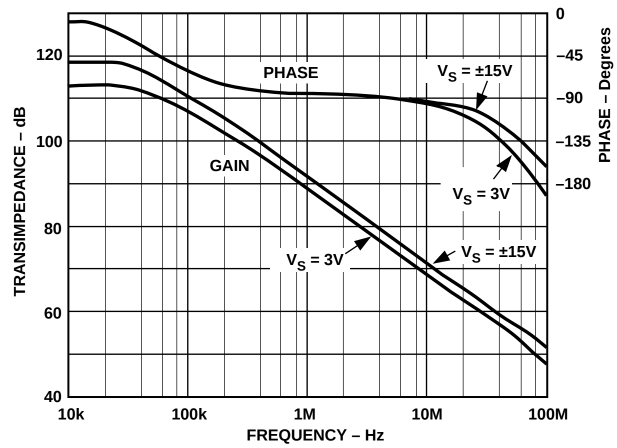


Figure 16. Open-Loop Transimpedance vs. Frequency (Relative to 1 Ω)

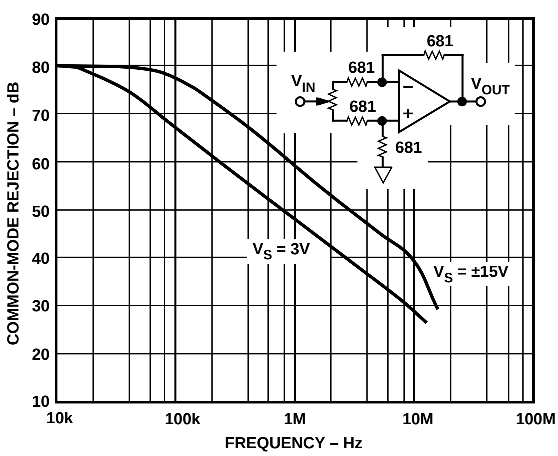


Figure 14. Common-Mode Rejection vs. Frequency

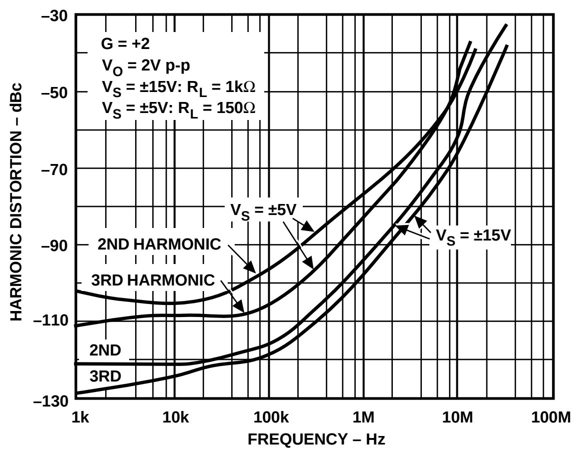


Figure 17. Harmonic Distortion vs. Frequency

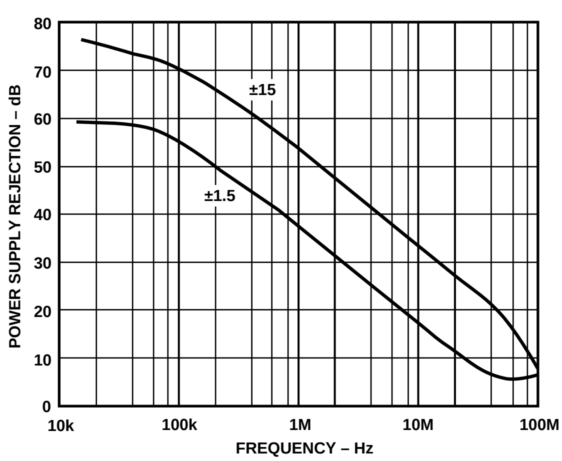


Figure 15. Power Supply Rejection vs. Frequency

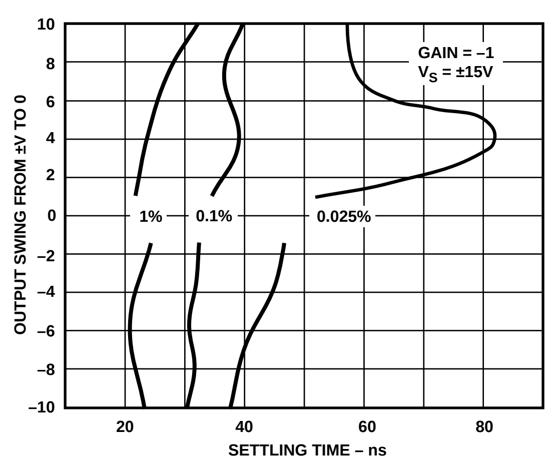


Figure 18. Output Swing and Error vs. Settling Time

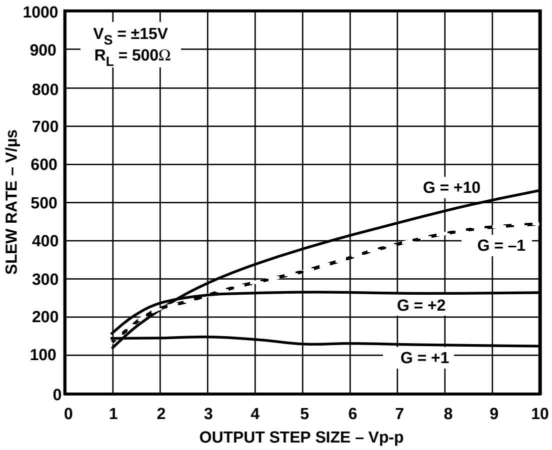


Figure 19. Slew Rate vs. Output Step Size

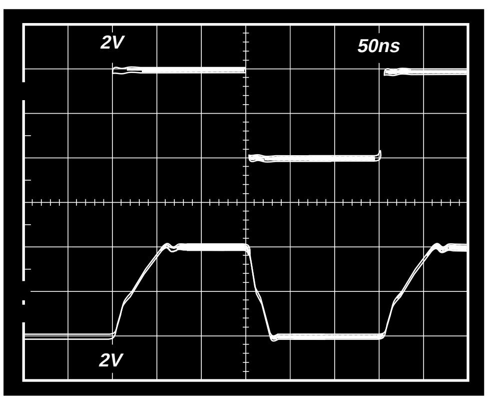


Figure 23. Small Signal Pulse Response, Gain = +1, (R_F = 750 Ω, R_L = 150 Ω, V_S = ±5 V)

Figure 21. Closed-Loop Gain and Phase vs. Frequency, G = +1

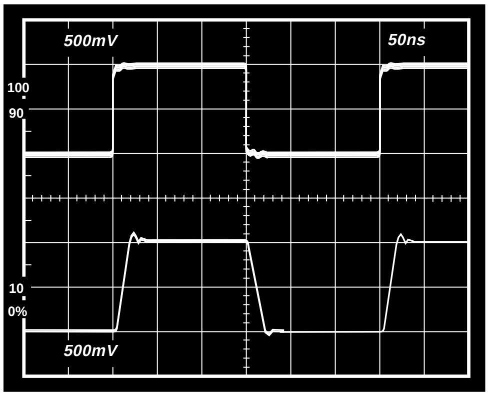


Figure 25. Large Signal Pulse Response, Gain = +10, (R_F = 357 Ω, R_L = 500 Ω, V_S = ±15 V)

Figure 28. Small Signal Pulse Response, Gain = +10, (R_F = 357 Ω, R_L = 150 Ω, V_S = ±5 V)

Figure 26. Closed-Loop Gain and Phase vs. Frequency, G = +10, R_L = 150 Ω

Figure 29. Closed-Loop Gain and Phase vs. Frequency, G = +10, R_L = 1 kΩ

Figure 27. –3 dB Bandwidth vs. Supply Voltage, G = +10, R_L = 150 Ω

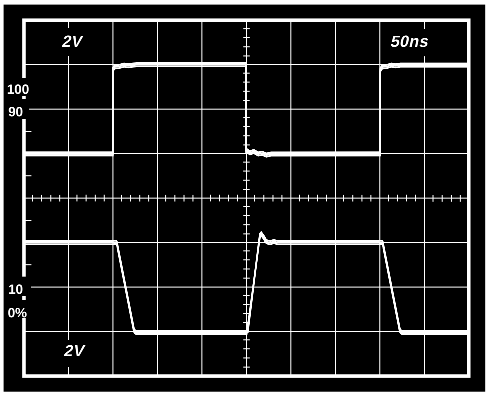


Figure 31. Large Signal Pulse Response, Gain = –1,

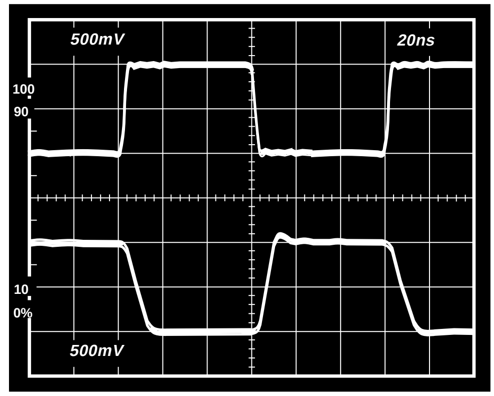


Figure 34. Small Signal Pulse Response, Gain = –1, (R_F = 750 Ω, R_L = 150 Ω, V_S = ±5 V)

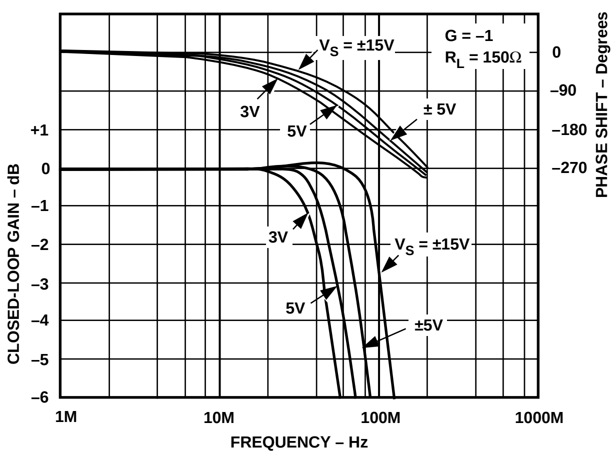


Figure 32. Closed-Loop Gain and Phase vs. Frequency, G = –1, R_L = 150 Ω

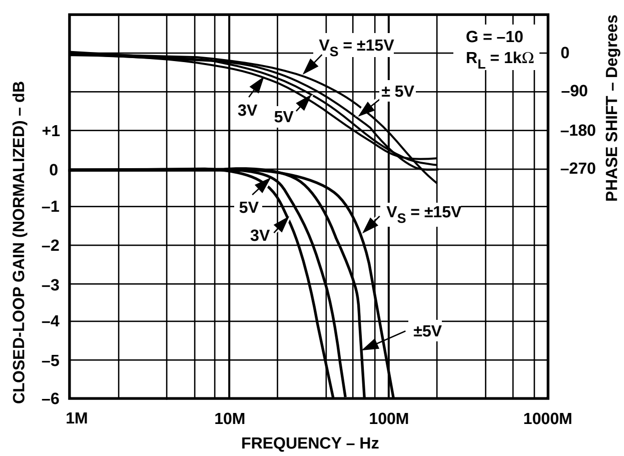


Figure 35. Closed-Loop Gain and Phase vs. Frequency, G = –10, R_L = 1 kΩ

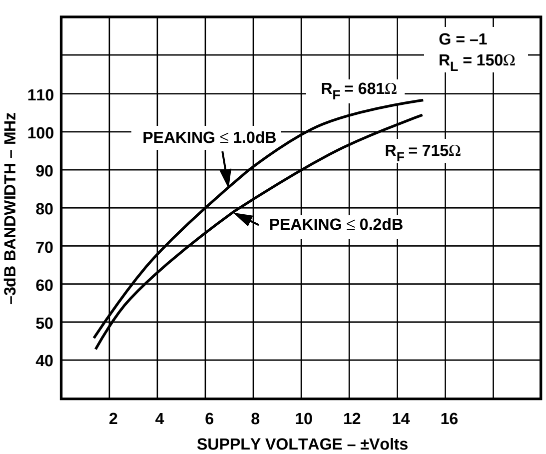


Figure 33. –3 dB Bandwidth vs. Supply Voltage, G = –1, R_L = 150 Ω

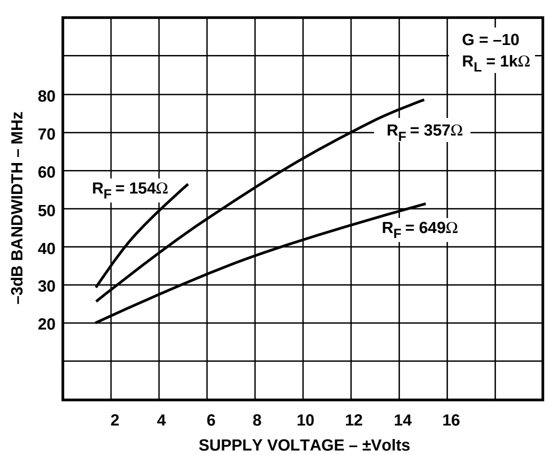


Figure 36. –3 dB Bandwidth vs. Supply Voltage, G = –10, R_L = 1 kΩ

General Consideration

The AD813 is a wide bandwidth, triple video amplifier that offers a high level of performance on less than 5.5 mA per amplifier of quiescent supply current. With its fast acting power down switch, it is designed to offer outstanding functionality and performance at closed-loop inverting or noninverting gains of one or greater.

Built on a low cost, complementary bipolar process, and achieving bandwidth in excess of 100 MHz, differential gain and phase errors of better than 0.1% and 0.1° (into 150 Ω), and output current greater than 40 mA, the AD813 is an exceptionally efficient video amplifier. Using a conventional current feedback architecture, its high performance is achieved through careful attention to design details.

Choice of Feedback & Gain Resistors

Because it is a current feedback amplifier, the closed-loop bandwidth of the AD813 depends on the value of the feedback resistor. The bandwidth also depends on the supply voltage. In addition, attenuation of the open-loop response when driving load resistors less than about 250 Ω will also affect the bandwidth. Table I contains data showing typical bandwidths at different supply voltages for some useful closed-loop gains when driving a load of 150 Ω. (Bandwidths will be about 20% greater for load resistances above a few hundred ohms.)

Table I. –3 dB Bandwidth vs. Closed-Loop Gain and Feedback Resistor, (R_L = 150 Ω)

V_S (V)	Gain	R_F (Ω)	BW (MHz)
±15	+1	866	125
	+2	681	100
	+10	357	60
	–1	681	100
	–10	357	55
±5	+1	750	75
	+2	649	65
	+10	154	40
	–1	649	70
	–10	154	40
+5	+1	715	60
	+2	619	50
	+10	154	30
	–1	619	50
	–10	154	30
+3	+1	681	50
	+2	619	40
	+10	154	25
	–1	619	40
	–10	154	20

The choice of feedback resistor is not critical unless it is important to maintain the widest, flattest frequency response. The resistors recommended in the table are those (metal film values) that will result in the widest 0.1 dB bandwidth. In those applications where the best control of the bandwidth is desired, 1% metal film resistors are adequate. Wider bandwidths can be attained by reducing the magnitude of the feedback resistor (at the expense of increased peaking), while peaking can be reduced by increasing the magnitude of the feedback resistor.

To estimate the –3 dB bandwidth for closed-loop gains or feedback resistors not listed in the above table, the following two pole model for the AD813 may be used:

$$A_{CL} = \frac{G}{S^2\left[\dfrac{(R_F + Gr_{IN})C_T}{2\ \pi\ f_2}\right] + S\ (R_F + Gr_{IN})\ C_T + 1}$$

Where: A_{CL} = closed-loop gain from "transcapacitance"
G = $1 + R_F/R_G$
r_{IN} = input resistance of the inverting input
C_T = "transcapacitance," which forms the open-loop dominant pole with the transresistance
R_F = feedback resistor
R_G = gain resistor
f_2 = frequency of second (nondominant) pole
s = $2\ \pi j\ f$

Appropriate values for the model parameters at different supply voltages are listed in Table II. Reasonable approximations for these values at supply voltages not found in the table can be obtained by a simple linear interpolation between those tabulated values which 'bracket' the desired condition.

Table II. Two Pole Model Parameters at Various Supplies

V_S (V)	r_{IN} (Ω)	C_T (pF)	f_2 (MHz)
±15	85	2.5	150
±5	90	3.8	125
+5	105	4.8	105
+3	115	5.5	95

As discussed in many amplifier and electronics textbooks (such as Roberge's *Operational Amplifiers: Theory and Practice*), the –3 dB bandwidth for the 2-pole model can be obtained as:

$$f_3 = f_n\left[1 - 2d^2 + (2 - 4d^2 + 4d^4)^{1/2}\right]^{1/2}$$

where:

$$f_n = \left[\frac{f_2}{(R_F + Gr_{IN})\,C_T}\right]^{1/2}$$

and:

$$d = \frac{1}{2}\left[f_2(R_F + Gr_{IN})\,C_T\right]^{1/2}$$

This model will predict –3 dB bandwidth within about 10% to 15% of the correct value when the load is 150 Ω. However, it is not accurate enough to predict either the phase behavior or the frequency response peaking of the AD813.

Printed Circuit Board Layout Guidelines

As with all wideband amplifiers, printed circuit board parasitics can affect the overall closed-loop performance. Most important for controlling the 0.1 dB bandwidth are stray capacitances at the output and inverting input nodes. Increasing the space between signal lines and ground plane will minimize the coupling. Also, signal lines connecting the feedback and gain resistors should be kept short enough that their associated inductance does not cause high frequency gain errors.

Power Supply Bypassing

Adequate power supply bypassing can be very important when optimizing the performance of high speed circuits. Inductance in the supply leads can (for example) contribute to resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to a load, then large (greater than 1 µF) bypass capacitors are required to produce the best settling time and lowest distortion. Although 0.1 µF capacitors may be adequate in some applications, more elaborate bypassing is required in other cases.

When multiple bypass capacitors are connected in parallel, it is important to be sure that the capacitors themselves do not form resonant circuits. A small (say 5 Ω) resistor may be required in series with one of the capacitors to minimize this possibility.

As discussed below, power supply bypassing can have a significant impact on crosstalk performance.

Achieving Low Crosstalk

Measured crosstalk from the output of Amplifier 2 to the input of Amplifier 1 of the AD813 is shown in Figure 37. All other crosstalk combinations, (from the output of one amplifier to the input of another), are a few dB better than this due to the additional distance between critical signal nodes.

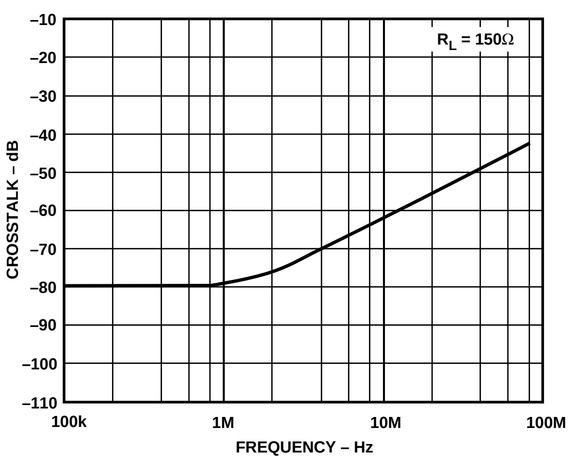


Figure 37. Worst Case Crosstalk vs. Frequency

A carefully laid-out PC board should be able to achieve the level of crosstalk shown in the figure. The most significant contributors to difficulty in achieving low crosstalk are inadequate power supply bypassing, overlapped input and/or output signal paths, and capacitive coupling between critical nodes.

The bypass capacitors must be connected to the ground plane at a point close to and between the ground reference points for the loads. (The bypass of the negative power supply is particularly important in this regard.) This requires careful planning as there are three amplifiers in the package, and low impedance signal return paths must be provided for each load. (Using a parallel combination of 1 µF, 0.1 µF, and 0.01 µF bypass capacitors will help to achieve optimal crosstalk.)

The input and output signal return paths (to the bypass caps) must also be kept from overlapping. Since ground connections are not of perfectly zero impedance, current in one ground return path can produce a voltage drop in another ground return path if they are allowed to overlap.

Electric field coupling external to (and across) the package can be reduced by arranging for a narrow strip of ground plane to be run between the pins (parallel to the pin rows). Doing this on both sides of the board can reduce the high frequency crosstalk by about 5 dB or 6 dB.

Driving Capacitive Loads

When used with the appropriate output series resistor, any load capacitance can be driven without peaking or oscillation. In most cases, less than 50 Ω is all that is needed to achieve an extremely flat frequency response. As illustrated in Figure 41, the AD813 can be very attractive for driving large capacitive loads. In this case, the AD813's high output short circuit current allows for a 150 V/µs slew rate when driving a 510 pF capacitor.

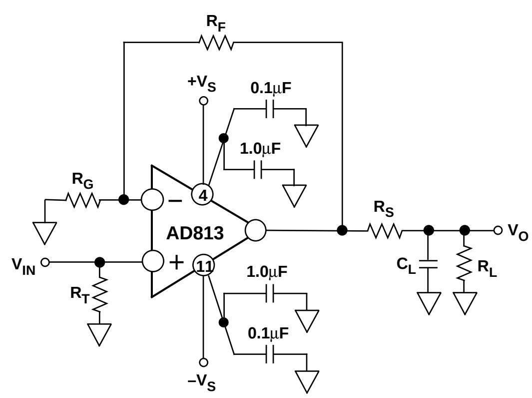


Figure 38. Circuit for Driving a Capacitive Load

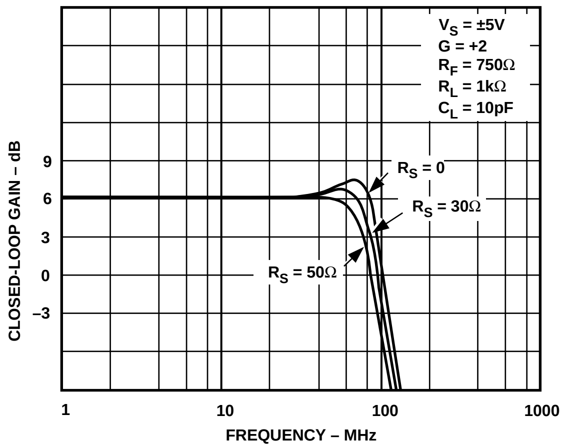


Figure 39. Response to a Small Load Capacitor at $V_S = \pm 5$ V

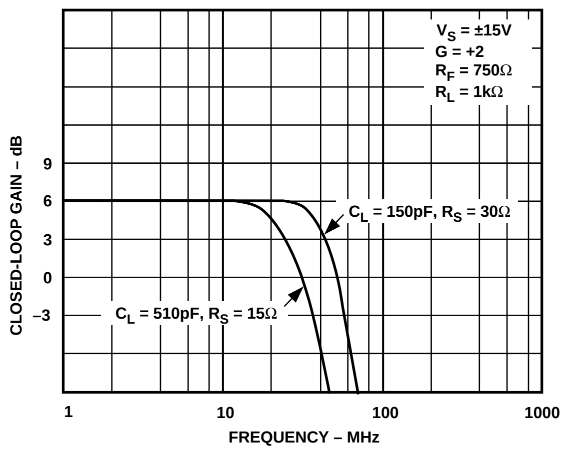


Figure 40. Response to a Large Load Capacitor at $V_S = \pm 15$ V

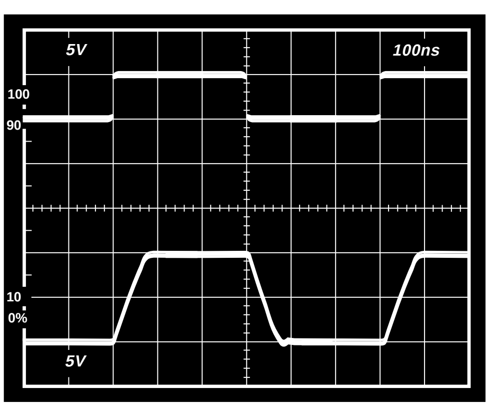


Figure 41. Circuit of Figure 38 Driving a 510 pF Load Capacitor, $V_S = \pm 15$ V (R_L = 1 kΩ, $R_F = R_G$ = 750 Ω, R_S =15 Ω)

Overload Recovery

There are three important overload conditions to consider. They are due to: input common-mode voltage overdrive, output voltage overdrive, and input current overdrive. When the amplifier is configured for low closed-loop gains, and the input common-mode voltage range is exceeded, the recovery time will be very fast, typically under 30 ns. When configured for a higher gain, and overloaded at the output, the recovery time will also be short. For example, in a gain of +10, with 6 dB of input overdrive, the recovery time of the AD813 is about 25 ns (see Figure 42).

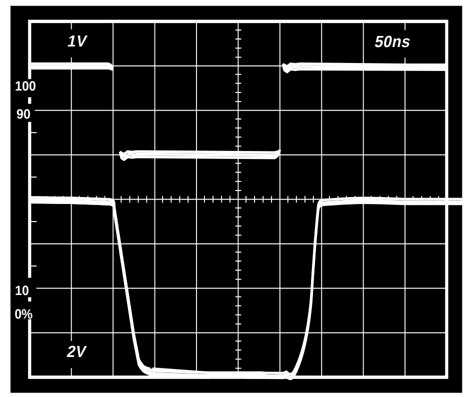


Figure 42. 6 dB Overload Recovery, G = +10, (R_L = 500 Ω, R_F = 357 Ω, V_S = ±5 V)

In the case of high gains with very high levels of input overdrive, a longer recovery time will occur. For example, if the input common-mode voltage range is exceeded in the gain of +10, the recovery time will be on the order of 100 ns. This is primarily due to current overloading of the input stage.

As noted in the warning under "Maximum Power Dissipation," a high level of input overdrive in a high noninverting gain circuit can result in a large current flow in the input stage. Though this current is internally limited to about 40 mA, its effect on the total power dissipation may be significant.

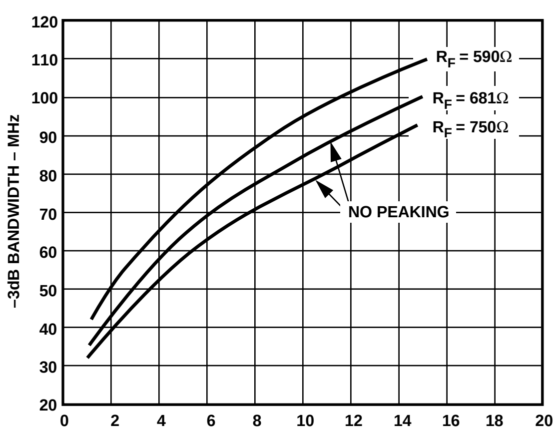


Figure 45. –3 dB Bandwidth vs. Supply Voltage for Gain = +2, R_L = 150 Ω

Operation Using a Single Supply

The AD813 will operate with total supply voltages from 36 V down to 2.4 V. With proper biasing (see Figure 49) it can make an outstanding single supply video amplifier. Since the input and output voltage ranges extend to within 1 V of the supply rails, it will handle a 1.3 V peak-to-peak signal on a single 3.3 V supply, or a 3 V peak-to-peak signal on a single 5 V supply. The small signal 0.1 dB bandwidths will exceed 10 MHz in either case, and the large signal bandwidths will exceed 6 MHz.

The capacitively coupled cable driver in Figure 49 will achieve outstanding differential gain and phase errors of 0.05% and 0.05 degrees respectively on a single 5 V supply. Resistor R2, in this circuit, is selected to optimize the differential gain and phase by biasing the amplifier in its most linear region.

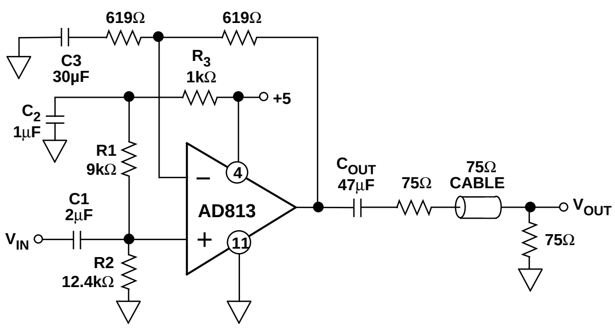


Figure 49. Biasing for Single Supply Operation

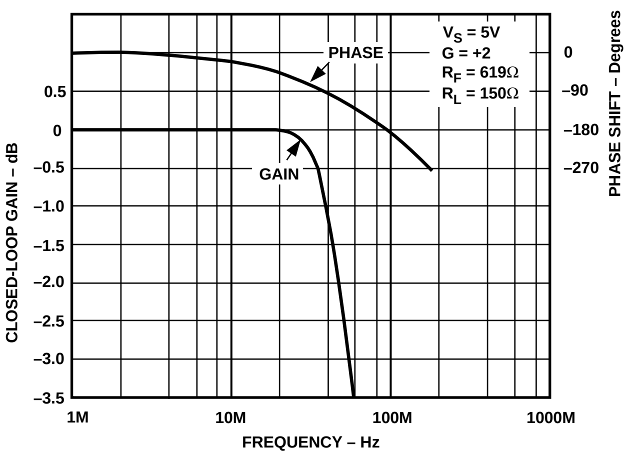


Figure 50. Closed-Loop Gain and Phase vs. Frequency, Circuit of Figure 49

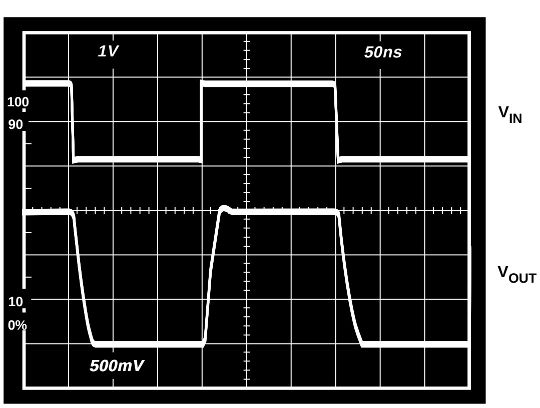


Figure 51. Pulse Response for the Circuit of Figure 49 with $+V_S = 5$ V

Disable Mode Operation

Pulling the voltage on any one of the Disable pins about 2.5 V down from the positive supply will put the corresponding amplifier into a disabled, powered down, state. In this condition, the amplifier's quiescent supply current drops to about 0.5 mA, its output becomes a high impedance, and there is a high level of isolation from input to output. In the case of the gain of two line driver for example, the impedance at the output node will be about the same as for a 1.4 kΩ resistor (the feedback plus gain resistors) in parallel with a 12.5 pF capacitor and the input to output isolation will be about 65 dB at 1 MHz.

Leaving the Disable pin disconnected (floating) will leave the corresponding amplifier operational, in the enabled state. The input impedance of the disable pins is about 35 kΩ in parallel with a few pF. When grounded, about 50 µA flows out of a disable pin on ±5 V supplies.

Input voltages greater than about 1.5 V peak-to-peak will defeat the isolation. In addition, large signals (greater than 3 V peak-to-peak) applied to the output node will cause the output impedance to drop significantly.

When the Disable pins are driven by complementary output CMOS logic (such as the 74HC04), the disable time is about 80 ns (until the output goes high impedance) and the enable time is about 100 ns (to low impedance output) on ±15 V supplies. When operated on ±15 V supplies, the disable pins should be driven by open drain logic. In this case, pull-up resistors from the disable pins to the plus supply will ensure minimum switching time.

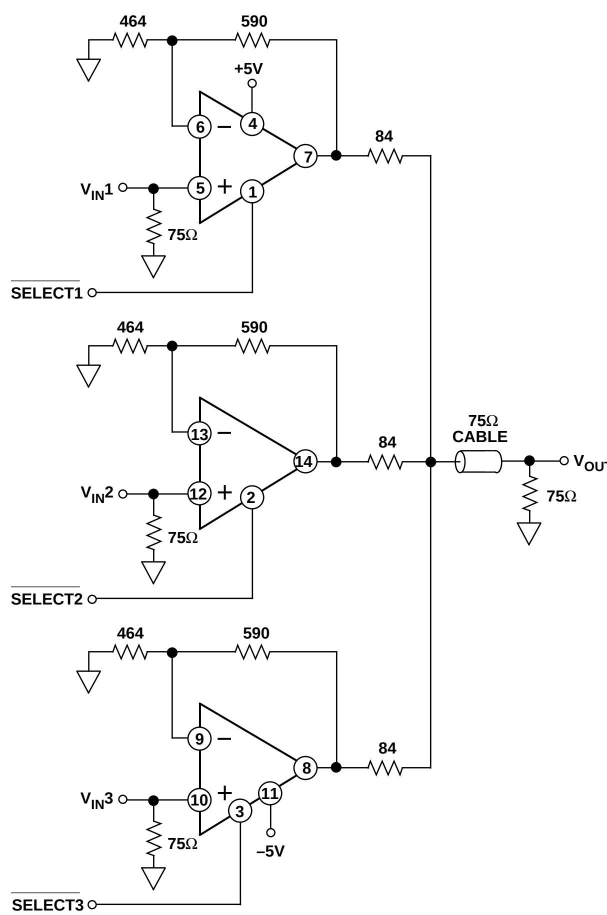


Figure 52. A Fast Switching 3:1 Video Mux (Supply Bypassing Not Shown)

3:1 Video Multiplexer

Wiring the amplifier outputs together will form a 3:1 mux with outstanding gain flatness. Figure 52 shows a recommended configuration which results in –0.1 dB bandwidth of 20 MHz and OFF channel isolation of 60 dB at 10 MHz on ±5 V supplies. The time to switch between channels is about 180 ns. Switching time is only slightly affected by signal level.

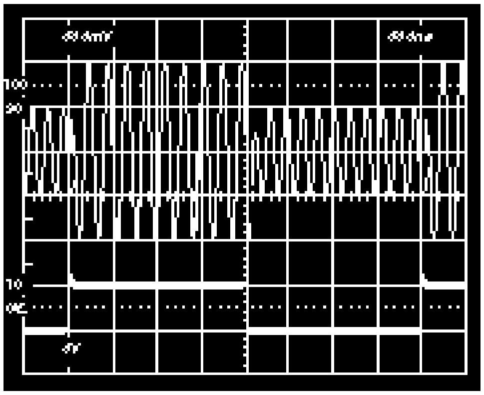


Figure 53. Channel Switching Characteristic for the 3:1 Mux

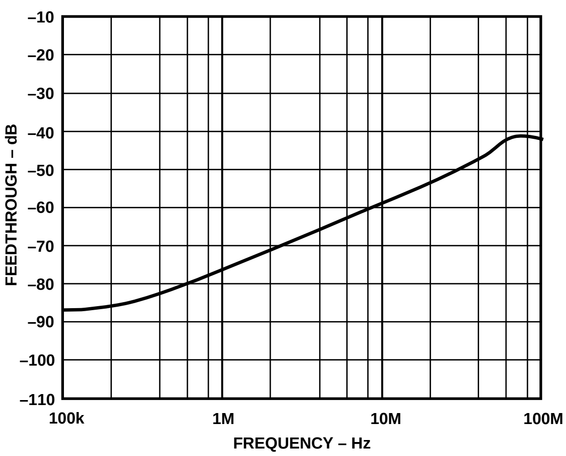


Figure 54. 3:1 Mux OFF Channel Feedthrough vs. Frequency

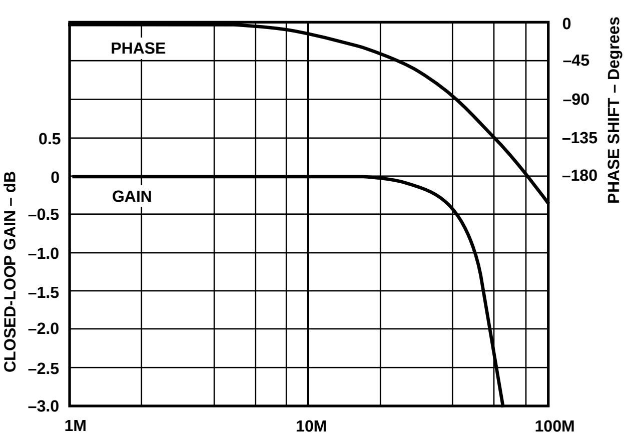


Figure 55. 3:1 Mux ON Channel Gain and Phase vs. Frequency

Single Supply Differential Line Driver

Due to its outstanding overall performance on low supply voltages, the AD813 makes possible exceptional differential transmission on very low power. The circuit of Figure 56 will convert a single-ended, ground referenced signal to a differential signal whose common-mode reference is set to one half the supply voltage. This allows for a greater than 2 V peak-to-peak signal swing on a single 3 V power supply. A bandwidth over 30 MHz is achieved with 20 mA of output drive on only 30 mW of quiescent power (excluding load current).

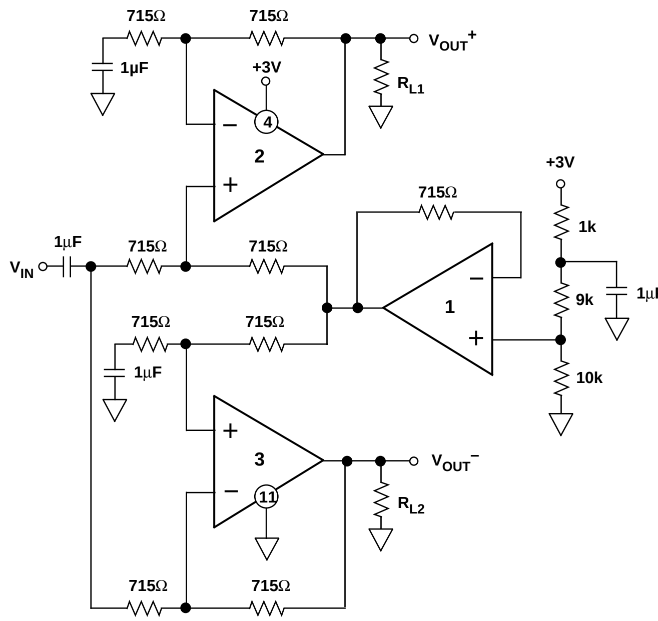


Figure 56. Single 3 V Supply Differential Line Driver with 2 V Swing

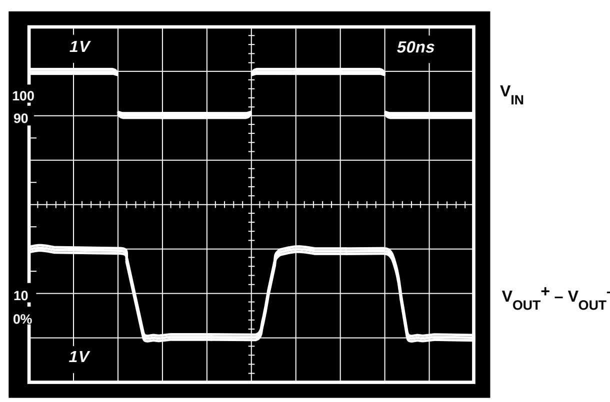
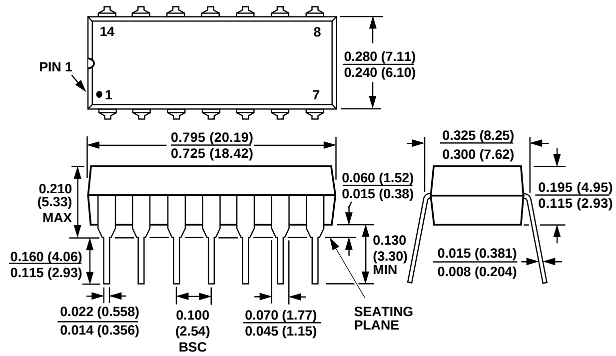


Figure 57. Differential Driver Pulse Response (V_S = 3 V, $R_{L1} = R_{L2}$ = 200 Ω)

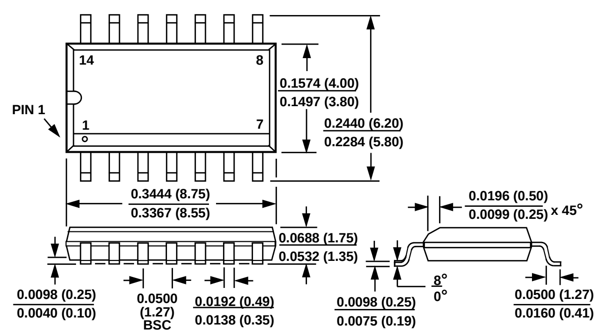
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead Plastic DIP (N-14)



14-Lead SOIC (R-14)



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