



1.1 Scope.

This specification covers the detail requirements for a 14-bit resolution A/D converter with complete microprocessor interface and an on-chip sample-hold amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD679SX/883B
-2	AD679TX/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

Appendix 1 of General Specification ADI-M-1000: package outline:

Type	Package	Description
D	D-28	28-Pin DIP
J	J-44	44-Pin JLCC

1.3 Absolute Maximum Ratings. ($T_A = -25^\circ\text{C}$ unless otherwise noted)

V_{CC} to AGND	+18 V to -0.3 V
V_{EE} to AGND	-18 V to +0.3 V
V_{DD} to DGND	0 V to +7 V
AGND to DGND	-1 V to +1 V
V_{CC} to V_{EE}	+26.4 V to -0.3 V
A_{IN} , REF_{IN} to AGND	V_{EE} to V_{CC}
Digital Inputs to DGND	-0.5 V to +7 V
Digital Outputs to DGND	-0.5 V to $V_{DD} + 0.3$ V
Power Dissipation	1000 mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 4^\circ\text{C/W}$ for J-44; 25°C/W for D-28
 $\theta_{JA} = 80^\circ\text{C/W}$ for J-44; 60°C/W for D-28

Tested in accordance with MIL-STD-750C in still air freely suspended under natural convection conditions.

REV. A

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Table 1.

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Power Dissipation	P_D	-1, 2	745	745	745	Converting	mW max
Internal Reference Output Voltage	V_{REF}	-1, 2	4.98	4.98	4.98	Bipolar 0.5 mA External Load	+V min
			5.02	5.02	5.02		+V max
Internal Reference Output Current	I_{REF}	-1, 2	1.5	1.5	1.5	Unipolar	mA max
			0.5	0.5	0.5	Bipolar	
High Level Input Voltage	V_{IH}	-1, 2	2.0	2.0	2.0		-V min
Low Level Input Voltage	V_{IL}	-1, 2	0.8	0.8	0.8		-V max
Logic Input Current	I_{IH}	-1, 2	10	10	10	$V_{IH} = 5.0$ V $V_{IL} = 0.0$ V	μ A max
High Level Output Voltage	V_{OH}	-1, 2	2.4	2.4	2.4	$I_{OH} = 0.5$ mA	-V min
Low Level Output Voltage	V_{OL}	-1, 2	0.4	0.4	0.4	$I_{OL} = 1.6$ mA	-V max
High Z Leakage Current	I_{OZ}	-1, 2	10	10	10	$V_{IN} = 0, V_{DD}$	μ A max
Power Supply Current	I_{CC}	1, 2	20	20	20	$V_{CC} = 12.6$ V	mA max
	I_{EE}	-1, 2	-34	-34	-34	$V_{EE} = -12.6$ V	
	I_{DD}	-1, 2	12	12	12	$V_{DD} = +5.5$ V	
Integral Nonlinearity	INL	-2	2	2	2	Unipolar	\pm LSB max
Differential Nonlinearity ²	DNL	-1, 2	14	14	14	All Codes Tested	Bits min
Unipolar Zero Error	ZE_U	-2	11.5	11.5			\pm LSB max
Bipolar Zero Error	ZE_B	-2	11.5	11.5			\pm LSB max
Unipolar Zero Error Drift	ZE_{UTC}	-2			16.4	w/Internal Reference	\pm LSB max
Bipolar Zero Error Drift	ZE_{BTC}	2			14.7	w/Internal Reference	\pm LSB max
Gain Error	GE	2	18	18		Unipolar & Bipolar Modes	+LSB max
Gain Error Drift	GETC	-2			16.4	Unipolar Mode w/External Reference	+LSB max
Gain Error Drift	GETC	-2			41	Unipolar & Bipolar Mode w/Internal Reference	± 1 LSB max
Power Supply Rejection Ratio	PSRR	-2	6	6	6	Unipolar Mode ³	\pm LSB max
Signal-to-Noise and Distortion	S/(N+D)	-1	78	78	78	Bipolar, $f_{IN} = 10.06$ kHz	dB min
		-2	78	78	78	Bipolar, $f_{IN} = 10.06$ kHz	
Total Harmonic Distortion	THD	-1, 2	-84	82	-82	Bipolar, $f_{IN} = 10.6$ kHz	dB max
Intermodulation Distortion Second-Order Products	IMD_2	-1, 2	-84	-84	-84	Bipolar, $f_A = 9.09$ kHz; $f_B = 9.58$	dB max
Intermodulation Distortion Third-Order Products	IMD_3	-1, 2	-84	84	-84	Bipolar, $f_A = 9.09$ kHz; $f_B = 9.58$	dB max
SC Delay	t_{SC}	-1, 2	50	50	50	See Figure 1	ns min
Conversion Rate	t_{CR}	1, 2	7.8	7.8	7.8	See Figure 1	μ s max
Convert Pulse Width	t_{CP}	-1, 2	97	97	97	See Figure 1	ns min
Conversion Time	t_C	-1, 2	6.3	6.3	6.3	See Figure 1	μ s max
Status Delay	t_{SD}	-1, 2	0	0	0	See Figure 1	ns min
			400	400	400		ns max
Access Time	t_{BA}	-1, 2	100	100	100	See Figures 2, 3, 4	ns max
Float Delay	t_{FD}	-1, 2	10	10	10	See Figures 2, 3, 4	ns min
		-1, 2	80	80	80		ns max
Format Setup	t_{FS}	-1, 2	100	100	100	See Figure 3	ns min
OE Delay	t_{OE}	-1, 2	20	20	20	See Figure 3	ns min
Read Pulse Width	t_{RP}	-1, 2	195	195	195	See Figure 3	ns min
Conversion Delay	t_{CD}	-1, 2	400	400	400	See Figures 1, 3	ns min
EOCEN Delay	t_{EO}	-1, 2	50	50	50	See Figure 2	ns min

NOTES

¹ $V_{REF} = +12\text{ V} \pm 5\%$, $V_{EE} = -12\text{ V} \pm 5\%$, $V_{DD} = 5\text{ V} \pm 10\%$. See Figures 1, 2, 3, and 4 for timing information.

²Minimum resolution for which no missing codes are guaranteed.

³Test condition for PSRR, with limit shown as the change from nominal value to each extreme:

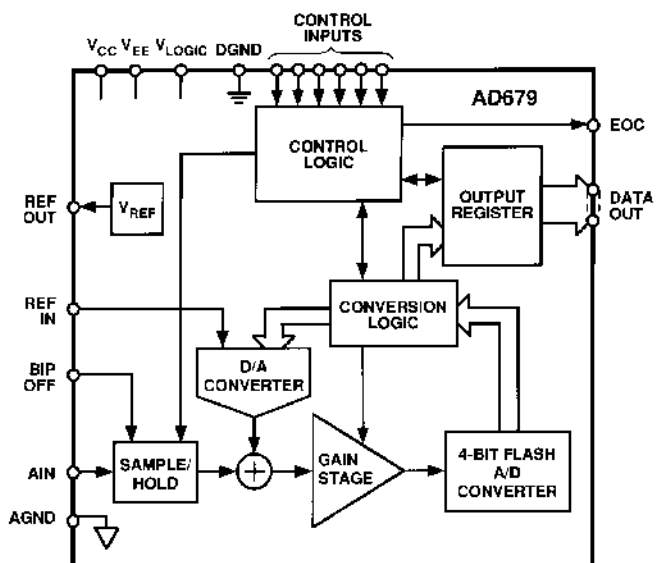
+11.4 V $\leq V_{CC} \leq$ -12.6 V; $V_{EE} = -12\text{ V}$; $V_{DD} = +5\text{ V}$

-12.6 V $\leq V_{EE} \leq$ 11.4 V; $V_{CC} = +12\text{ V}$; $V_{DD} = +5\text{ V}$

+4.5 V $\leq V_{DD} \leq$ +5.5 V; $V_{CC} = -12\text{ V}$; $V_{EE} = -12\text{ V}$

3.2.1 Functional Block Diagram and Terminal Assignments.

Description	D-Pin Description	J-44 Pin Description
$\overline{\text{EOCEN}}$	1	1
$\overline{\text{OE}}$	2	3
$\overline{\text{SC}}$	3	5
$\overline{\text{CS}}$	4	6
V_{EE}	5	8
AIN	6	10
AGND	7	11
REFOUT	8	12
REFIN	9	14
BIPOFF	10	15
V_{CC}	11	17
DGND	12	19
SYNC	13	21
DGND	14	23
$\overline{\text{HBE}}$	15	25
V_{DD}	16	26
V_{DD}	17, 18	27, 30
DB0	19	31
DB1	20	33
DB2	21	34
DB3	22	35
DB4	23	36
DB5	24	37
DB6	25	39
DB7	26	40
EOC	27	42
V_{DD}	28	43



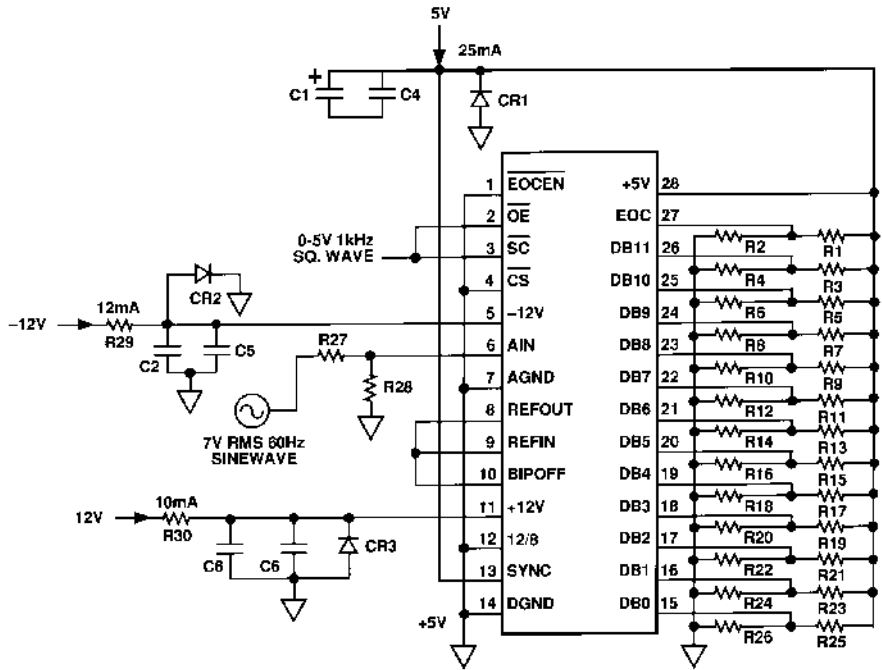
3.2.4 Microcircuit Technology Group.

This circuit is covered by technology group (57).

AD679

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



- NOTES**
1. C1, C2, C3 ARE 47µF CAPACITORS RATED AT 35V, 125°C.
 2. C4, C5, C6 ARE 0.1µF CAPACITORS RATED AT 50V, 125°C.
 3. CR1, CR2, CR3 ARE MRB20 DIODES.
 4. R1-R26 ARE 3kΩ RESISTOR PACKS.
 5. ALL CURRENTS SHOWN ARE MAXIMUM PER DEVICE.
 6. R27, R28 ARE 10kΩ 1% 1/4 WATT METAL FILM RESISTORS.
 7. R29 AND R30 ARE 1Ω 2 WATT GLASS RESISTORS.

Burn-In Circuit

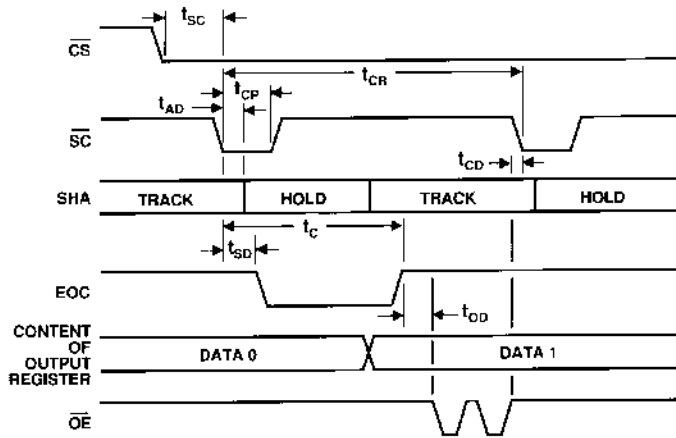


Figure 1. Conversion Timing

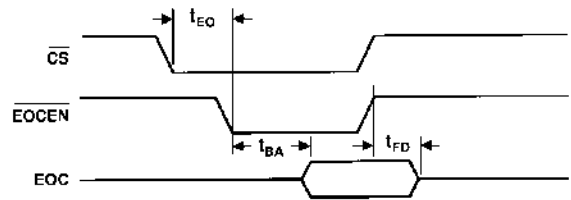
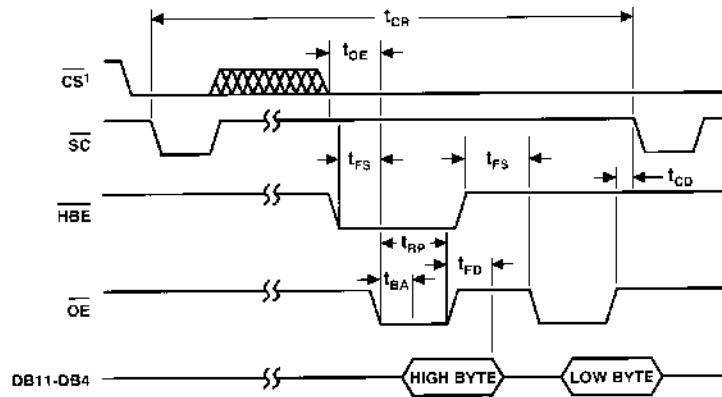


Figure 2. EOC Timing



NOTE
¹ IN ASYNCHRONOUS MODE, \overline{SC} IS INDEPENDENT OF \overline{CS} .

Figure 3. Output Timing

TIME	V_{CP}	C_{OUT}
ACCESS TIME HIGH Z TO LOGIC LOW	5V	100pF
FLOAT TIME LOGIC HIGH TO HIGH Z	0V	10pF
ACCESS TIME HIGH Z TO LOGIC HIGH	0V	100pF
FLOAT TIME LOGIC LOW TO HIGH Z	5V	10pF

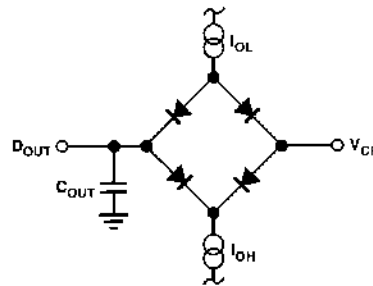
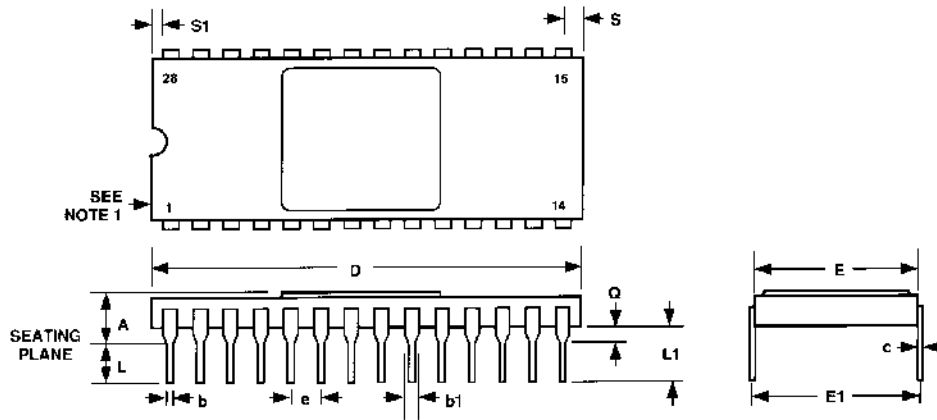


Figure 4. Load Circuit for Bus Timing Specifications

D-28 28-Pin Side Brazed Ceramic DIP

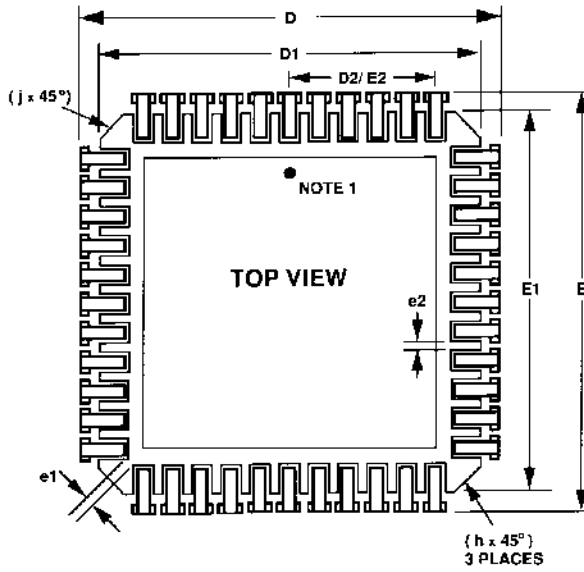


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.232	—	5.84	6
b	0.014	0.023	0.36	0.58	6
b1	0.038	0.065	0.96	1.65	2,6
c	0.008	0.015	0.20	0.38	6
D	—	1.490	—	37.85	4
E	0.500	0.610	12.70	15.49	4
E1	0.590	0.620	14.99	15.75	—
e	0.100	BSC	2.54	BSC	7
L	0.125	0.200	3.18	5.08	—
L1	0.150	—	3.81	—	—
Q	0.015	0.060	3.38	1.52	3
S	—	0.100	—	2.54	5
S1	0.005	—	0.13	—	5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to the lead one.
2. The minimum limit for dimension b may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads - increase maximum limit by 0.003" (0.008 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twenty-six spaces.

J-44
44-Pin JLCC



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.100	0.135	2.54	3.43	2
A1	0.054	0.078	1.37	1.98	
A2	0.025	-	0.64	-	
B	0.013	0.023	0.33	0.58	3
B1	0.020	0.032	0.51	0.81	3
C	0.008	0.013	0.15	0.33	3
D / E	0.680	0.700	17.27	17.78	
D1 / E1	0.628	0.662	15.95	16.82	
D2 / E2	0.250	BSC	6.35	BSC	
D3 / E3	0.500	BSC	12.70	BSC	
D4 / E4	0.610	0.650	15.49	16.51	
e	0.050	BSC	1.27	BSC	
e1 / e2	0.012	-	0.30	-	
L	0.030	-	0.76	-	
L1	0.005	-	0.12	-	
L2	0.025	-	0.76	-	
Q	0.003	-	0.08	-	
R	0.015	-	0.38	-	
R1	0.025	0.040	0.76	1.02	
h	0.040	REF	1.02	REF	
i	0.020	REF	0.52	REF	

NOTES

1. Pin 1 indicator is on the bottom of the package.
2. Dimension A controls the overall package thickness.
3. All Leads - increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.

